

RZ Ecosystem Partner Solution

Aurora System PCB Verification Services



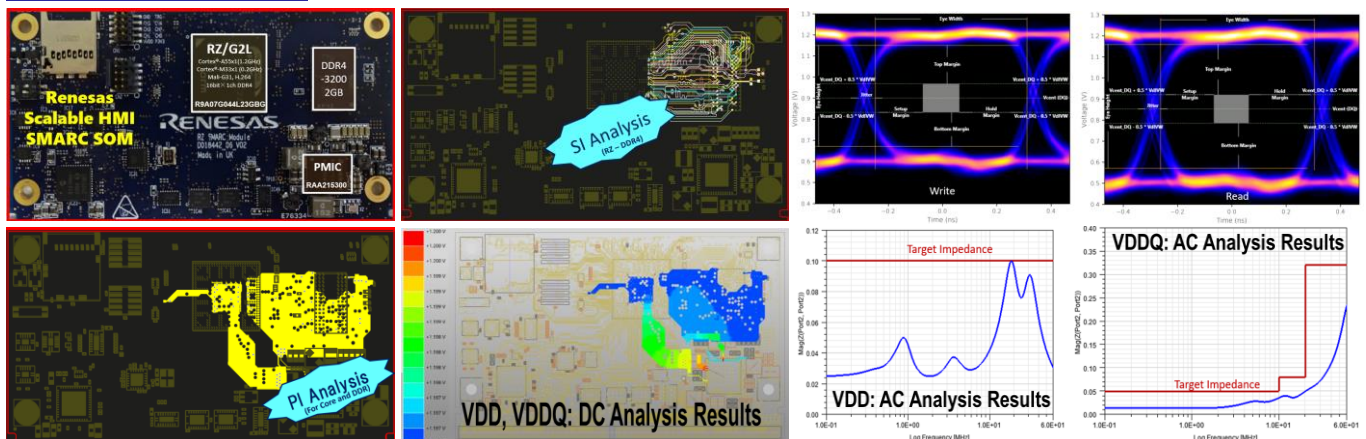
Solution Summary

Based on Aurora's proprietary SI/PI verification platform that incorporates the industrial leading-edge simulation software, our service ensures simulation accuracy and fast turn-around time for the [RZ Family of MPUs](#) in which some RZ MPUs have high-speed parallel memory interfaces(DDR4/LPDDR4). Aurora's Signal Integrity (SI) simulation services ensure your PCB design meets the RZ PCB verification guide as well as each interface's specifications. Aurora's Power Integrity (PI) simulation services verify your PCB design meets based on the RZ power verification guide.

Features/Benefits

- High-Speed Parallel Interface Analysis – DDR3/DDR4/DDR5/LPDDR4/LPDDR5/ONFI
- High-Speed Serial Interface Analysis – PCI Express/HDMI/MIPI/USB/Ethernet etc
- Low-Speed General Purpose I/F Analysis – I2C/SPI/I2S etc
- Power Integrity Analysis – AC/DC/Transient Analysis, Decap Optimization
- Thermal Analysis / EMI Analysis

Diagrams/Graphics



Target Markets and Applications

- IoT applications
- Consumer electronics
- Artificial intelligence
- Computing infrastructure
- Industrial controls
- Smart buildings
- HMI
- Communication

Aurora System Inc.

➤ Company Information

- Established : 2016
- Headquarter: San Jose, CA, USA
- Development Office : USA, China
- Sales, Support Office: USA, Japan, China
Taiwan, Singapore



➤ Aurora System Business

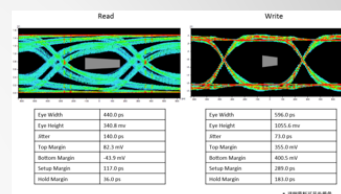
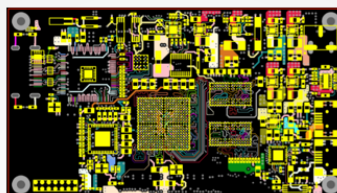
- LSI, Package, PCB Co-simulation Service, Consulting Service, Verification Platform Development
 - High-Speed Parallel Interface Signal Integrity Analysis(DDR3/4/5, LPDDR4/4X/5)
 - High-Speed Serial Interface Signal Integrity Analysis (PCIe, MIPI, HDMI, USB, ...)
 - General I/O Signal Integrity Analysis (I2C, I2S, I3C, ...)
 - Power Integrity Analysis (AC/DC/Transient Analysis)
 - Thermal / EMI Analysis



Simulation Service Process

Information Required	Format	Comments
1. PCB layout file	PDF, Gerber, ODB++	Required for simulation
2. BOM file	CSV	Required for component parameters
3. Package model	CSV	Required for package parameters
4. Clock signal	CSV	Required for clock signal

Sample 6-layer Stackup File
Layer 1: 1.5mm FR4
Layer 2: 0.1mm Cu
Layer 3: 0.1mm Cu
Layer 4: 0.1mm Cu
Layer 5: 0.1mm Cu
Layer 6: 1.5mm FR4



Customer Submit
Design Data to Aurora

Aurora Perform Simulation
And Verification Analysis

Return Verification Report
To Customer

- Support most of PCB and package design format (Cadence, Mentor, Altium, ANSYS, ...)
- BOM and stack-up
- IBIS, IBIA-AMI, SPICE, Package..

- DDR: DDR3/4/5, LPDDR4/5/4x/5x
- SerDes: PCIe, MIPI, HDMI, USB
- GPIO: I²C, SPI, SPMI, I²S, ...
- PDN PI analysis, Optimization
- Extract SI/PI package model

- SI report
 - Impedance, Delay, Skew, Eyediagram
- PI report
 - DC/AC analysis, broadband model
- Package model
 - RLCG and broadband model

