Application Note

Power Solutions for Xilinx® Spartan®-7 Devices

AN-PM-096

Abstract

This application note provides information on powering the Xilinx Spartan-7 family of devices.

Power Solutions for Xilinx® Spartan®-7 Devices

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1 Terms and Definitions

GUI	Graphical User Interface
PMIC	Power Management Integrated Circuit
DA906x	Dialog DA9061, DA9062, DA9063, and DA9063L
DVC	Dynamic Voltage Control
DVS	Dynamic Voltage Scaling, analogous to DVC
MPSoC	Multiprocessor System-on-Chip
OTP	One-Time Programmable (memory)
RTC	Real-Time Clock
SoC	System-on-Chip

2 References

[1] Xilinx Power Estimator (XPE), http://www.xilinx.com/products/technology/power/xpe.html [Accessed 4th Oct 2016]

[2] Philofsky, B., 'Seven Steps to an Accurate Worst-Case Power Analysis Using Xilinx Power Estimator (XPE)', WP353, v1.0, Xilinx Inc., 2008.

[3] DA9061, Datasheet, Dialog Semiconductor, Dialog Website Link

[4] DA9062, Datasheet, Dialog Semiconductor, Dialog Website Link

[5] DA9063, Datasheet, Dialog Semiconductor, Dialog Website Link

[6] DA9063L, Datasheet, Dialog Semiconductor, Dialog Website Link

[7] AN-PM-080, 'In-Circuit Programming of DA9061/2/3', Dialog Semiconductor, 2016, Dialog Website Link

[8] UM-PM-008, SmartCanvas™ DA9061/2 User Manual, Dialog Semiconductor, Dialog Website Link

[9] UG583, UltraScale Architecture PCB Design User Guide (ver1.10)

[10] Spartan-7 FPGAs Data Sheet: DC and AC Switching Characteristics, Xilinx, Link

[11] DA9062 Performance Board Schematic, Dialog Semiconductor, Dialog Website Link

3 Introduction

The Xilinx Spartan-7 family of FPGA devices is part of the Xilinx All Programmable Cost-Optimized Portfolio. To fully realize the performance of a Spartan-7 device requires an optimized power management solution. The Dialog DA9062 PMIC provides flexibility to match the requirements of most FPGA designs while maximizing performance and integration, and minimizing the PCB footprint.

4 Getting Started

The following sections introduce the basic power rail requirements of the Spartan-7 devices along with the capabilities of the Dialog DA9062 PMIC, and show why they are the perfect partners.

4.1 The Spartan-7

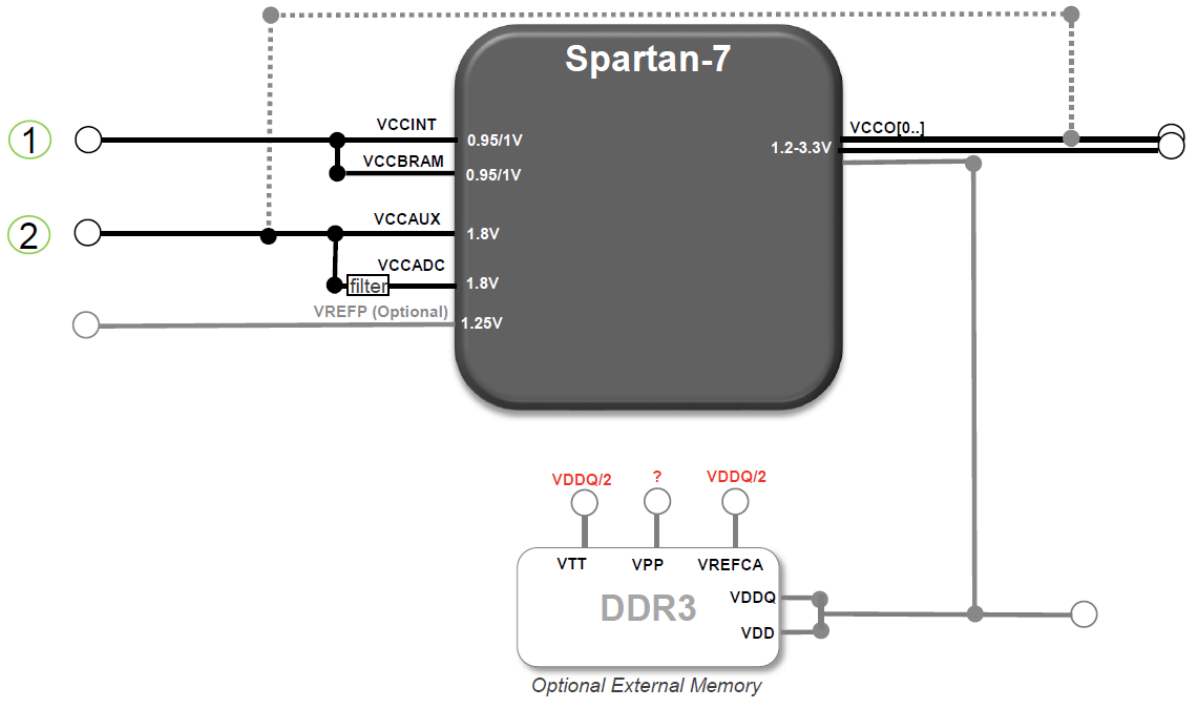

Figure 1: The Spartan-7 Power Rail Requirements

Table 1: Spartan-7 Power Rail Requirements

Rail	Voltage (V)	Load (A)
VCCINT	0.95 or 1	**0.3 to 2.5**
VCCBRAM	0.95 or 1	0.1
VCCAUX	1.8	0.15 to 0.35
VCCADC	1.8	
VREFP	1.25	
VCCIO	1.2 to 3.3	**0.2 to 2.5**
VDDQ	1.35 to 1.5	**2**

Rail	Voltage (V)	Load (A)
VREFCA		0.01
VTT		**1**

4.2 The Dialog DA9062

The Dialog DA9062 flexible power management IC integrates four bucks and four LDOs capable of supplying individual rails of up to 2.5 A. This device ideally matches the requirements of the Spartan-7 family of devices.

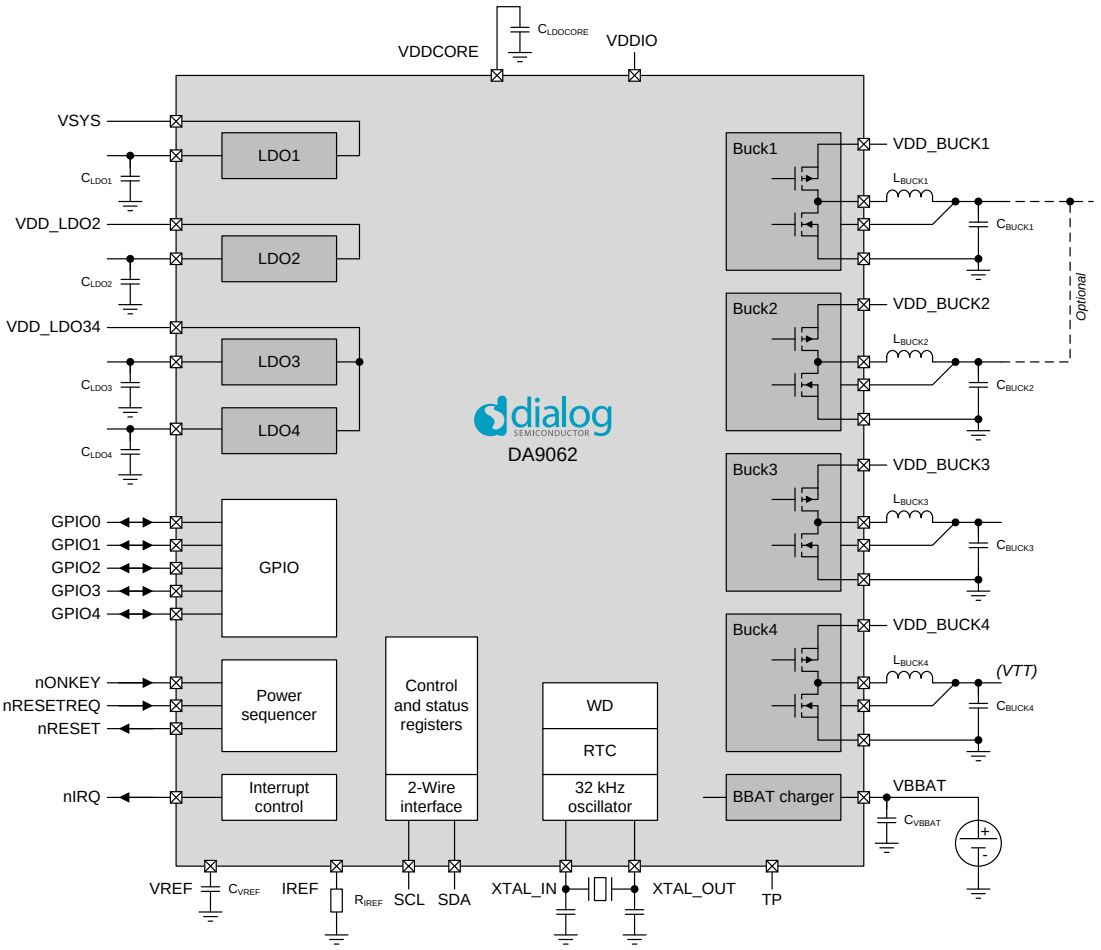

Figure 2: DA9062 Block Diagram

4.2.1 The DA9062 Regulators

Table 2: DA9062 Regulator Summary

Regulator	Supplied Voltage (V)	Supplied Max. Current (A)	External Component	Notes
Buck1	0.3 to 1.57	2.5	1.0 µH / 2 x 47 µF	3 MHz, DVS with variable slew rate, 10 mV steps
Buck2	0.3 to 1.57	2.5	1.0 µH / 2 x 47 µF	3 MHz, DVS with variable slew rate, 10 mV steps, can be combined with Buck1 as a 5 A dual-phase buck
Buck3	0.8 to 3.34	2.0	1.0 µH / 2 x 22 µF or 2 x 47 µF	3 MHz, DVS with variable slew rate, 20 mV steps
Buck4	0.53 to 1.8	1.5	1.0 µH / 2 x 22 µF or 2 x 47 µF	3 MHz, DVS with variable slew rate, 10 mV steps, can be used as a DDR VTT supply
LDO1	0.9 to 3.6	0.1	1.0 µF	Programmable in 50 mV steps, can be configured as an ‘always-on’ supply
LDO2	0.9 to 3.6	0.3	2.2 µF	Programmable in 50 mV steps
LDO3	0.9 to 3.6	0.3	2.2 µF	Programmable in 50 mV steps
LDO4	0.9 to 3.6	0.3	2.2 µF	Programmable in 50 mV steps

4.2.2 The DA9062 PCB Footprint

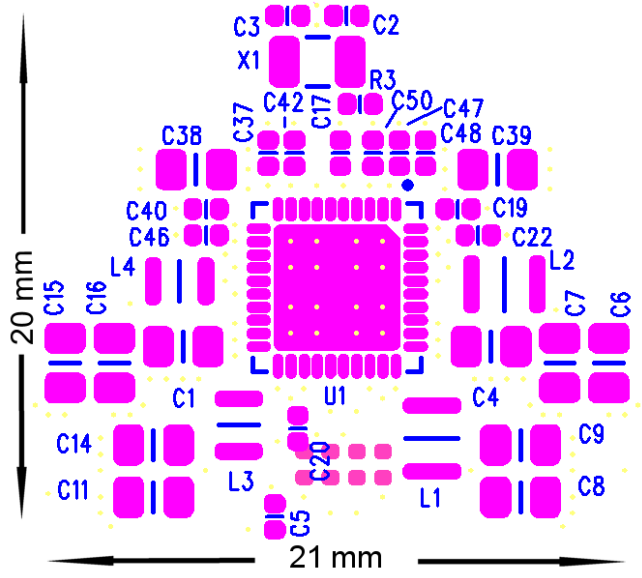

Figure 3: DA9062 Solution Footprint

The high level of integration along with the 3 MHz switching frequency results in a compact footprint. Figure 3 is an example footprint including all of the required passive components. The total area is less than 420 mm^2. This is achieved with all of the components on the top side of the PCB and without the use of over-aggressive placement. This area could be further reduced by placing some of the capacitors on the reverse of the PCB and by more aggressive spacing rules. As shown, there is significant unused space in the calculated area, possibly up to 25 %. See the DA9062 Performance board data pack for more details [11].

4.2.3 Typical Bill of Materials

Table 3: DA9062 Bill of Materials

Qty	Description	Value	Tol.	Rating	Dielectric	Manufacturer	Manufacturer Part Number
1	DA9062 QFN40	DA9062				Dialog	DA9062
2	TFM252010 Series SMD Inductor	1 µH	±20 %	Isat=3.5 A		TDK	TFM252010A-1R0M
2	TFM201610 Series SMD Inductor	1 µH	±20 %	Isat=2.9 A		TDK	TFM201610A-1R0M
4	0402 (1005 Metric) SMD Resistor	100 kΩ	±1 %	0.063 W		Yageo	RC0402FR-07100KL
1	0402 (1005 Metric) SMD Resistor	200 kΩ	±1 %	0.063 W		Yageo	RC0402FR-07200KL
2	0402 (1005 Metric) SMD Capacitor	15 pF	±5 %	50 V	COG/NPO	Murata	GRM1555C1H150JZ01D
2	0402 (1005 Metric) SMD Capacitor	100 nF	±10 %	10 V	X5R	Murata	GRM155R61A104KA01D
1	0402 (1005 Metric) SMD Capacitor	470 nF	±10 %	10 V	X5R	Murata	GRM155R61A474KE15D
4	0402 (1005 Metric) SMD Capacitor	1 µF	±10 %	10 V	X5R	Murata	GRM155R61A105KE15D
4	0805 (2012 Metric) SMD Capacitor	22 µF	±20 %	10 V	X5R	Taiyo Yuden	LMK212BJ226MG-T
5	0402 (1005 Metric) SMD Capacitor	2.2 µF	±20 %	6.3 V	X5R	Murata	GRM155R60J225ME95
8	0805 (2012 Metric) SMD Capacitor	47 µF	±20 %	4 V	X5R	Murata	GRM219R60G476M

NOTE

The BoM does not include the 32 kHz crystal or the backup battery cell as these are optional components dependent on the application requirements.

4.3 Mapping to the DA9062

Comparing the Spartan-7 power rail requirements from Table 1 with the DA9062 available regulators in Table 2, it is clear to see that the DA9062 is a good match for designs using the Spartan-7.

Mapping the Spartan-7 on to the DA9062 rails is shown in Table 4.

Table 4: DA9062 Mapping for Spartan-7

Spartan-7			DA9062	
Rail	**Voltage (V)**	**Load (A)**	**Rail**	**Max. (A)**
VCCINT	0.95/1	**0.3 to 2.5**	VBuck1	2.5
VCCBRAM	0.95/1	0.1	VBuck1	0.1
VCCAUX	1.8	0.15 to 0.35	LDO2*	0.3
VCCADC	1.8			
VREFP	1.25			
VCCIO	1.2 to 3.3	**0.2 to 2.5**	Buck3	2.0
VDDQ	1.35 to 1.5	**2**	Buck2	2.5
VREFCA		0.01	VTTREF	0.01
VTT		**1**	Buck4	

4.3.1 Flexibility

The DA9062 has four LDO regulators, so there are three spare regulators that can be used to provide power to additional parts of the system, or to supply additional voltage IO domains.

The voltage required to supply the VCCINT rail is either 0.95 V or 1.0 V.

The voltage required to supply the VDDQ rail is either 1.35 V or 1.5 V.

The DA9062 can be configured to provide two different output voltages depending on the state of a GPIO. A single configuration of the DA9062 can therefore easily fulfil the requirements of many Spartan-7 designs.

For designs not using DDR memory, or not requiring DDR termination, Buck4 can be configured as a normal buck to provide an extra supply rail for IO or any other requirement of the system. In applications where the additional rail is not required, the Dialog DA9061 should be considered.

For more demanding designs, Dialog has a range of System and Sub PMICS that can be used to build a power tree that will meet your needs, see http://www.dialog-semiconductor.com/power-management for more information.

4.3.2 DA9062 Additional Features

Along with the buck and LDO regulators, the DA9062 also includes a range of additional features that are vital to most systems.

- Supply rail qualification: The DA9062 can monitor the incoming supply to prevent the system starting if a suitable supply is not available. A warning will be generated if the supply falls below a programmed level.
- Low power RTC with alarm function and 32 kHz output.
- System RESET control: The DA9062 provides a system RESET signal that is used to hold the system in RESET until all supply rails are available.
- System Watchdog: The watchdog can be used to reset the system in the case that the system becomes unresponsive.

4.3.3 Working with the DA9062

The DA9062 Evaluation kit includes a flexible evaluation board to allow access to all of the key features of the part. The evaluation kit also includes the Dialog SmartCanvas™ GUI which simplifies the control and configuration of the DA9062.

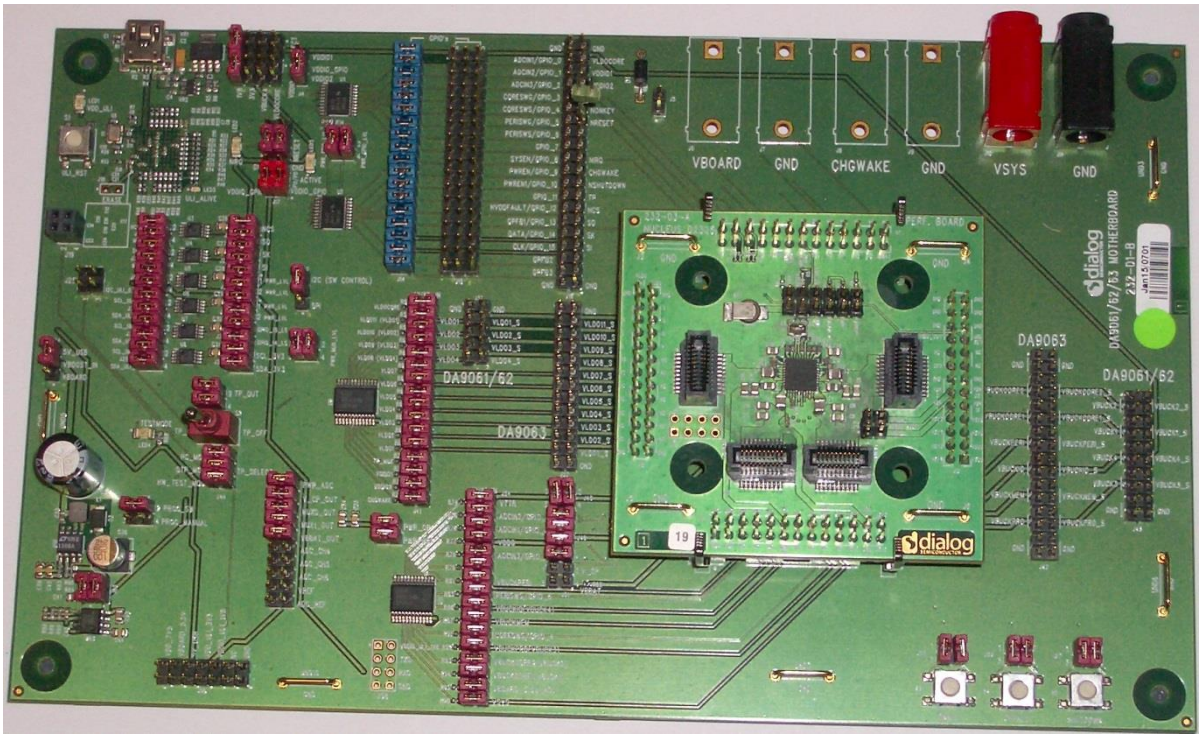

Figure 4: The DA9062 Evaluation Board

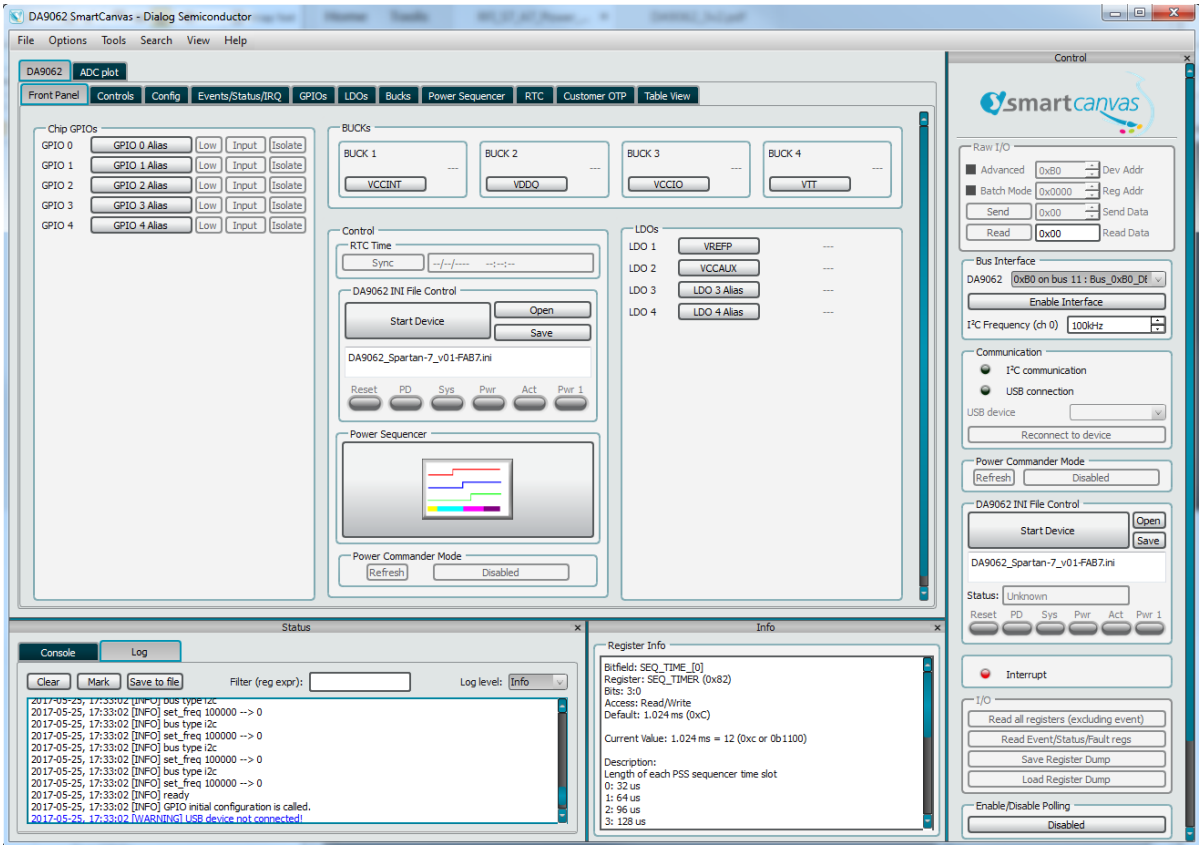

Figure 5: The DA9062 SmartCanvas GUI

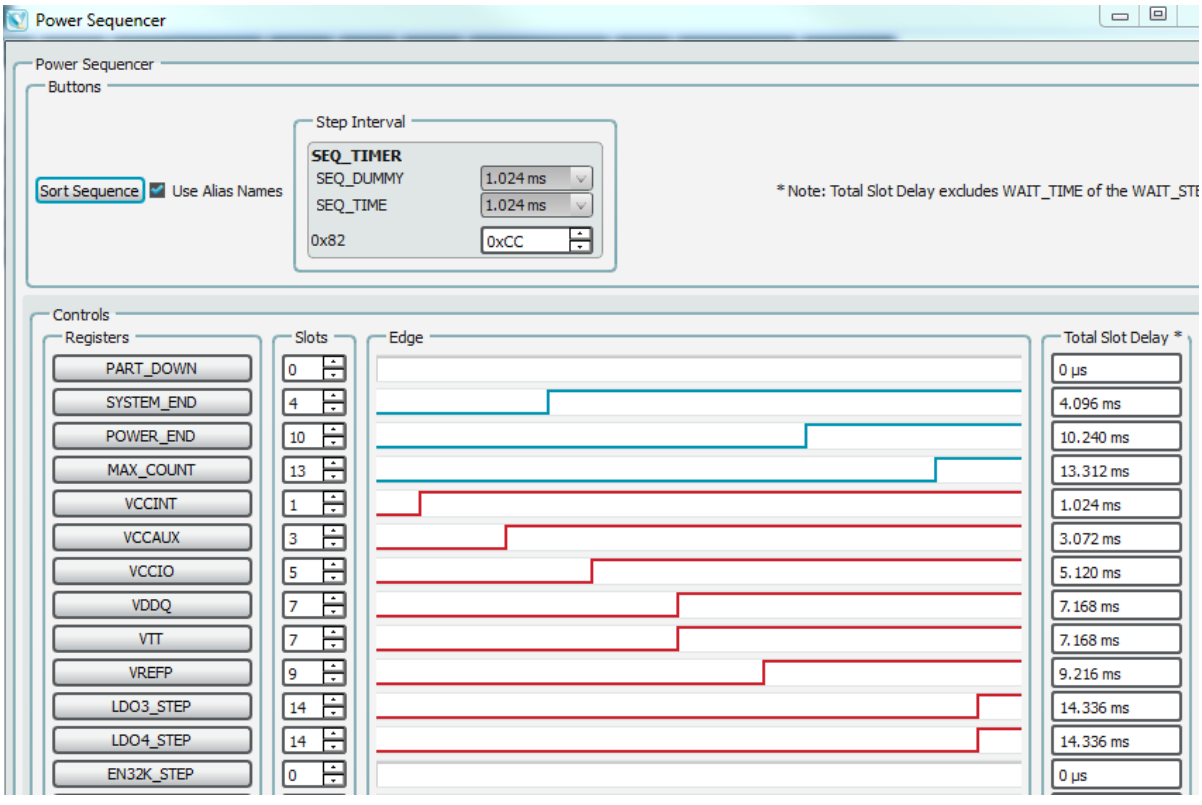

Figure 6: The SmartCanvas Drag and Drop Sequence Tool

4.4 Bench Measurements

This section provides some basic performance measurements made using the DA9062 Evaluation kit.

The following measurements are included:

- power-on sequence
- buck efficiency
- static load regulation.
- buck transient load regulation
- reference measurements

4.4.1 Power-On Sequence

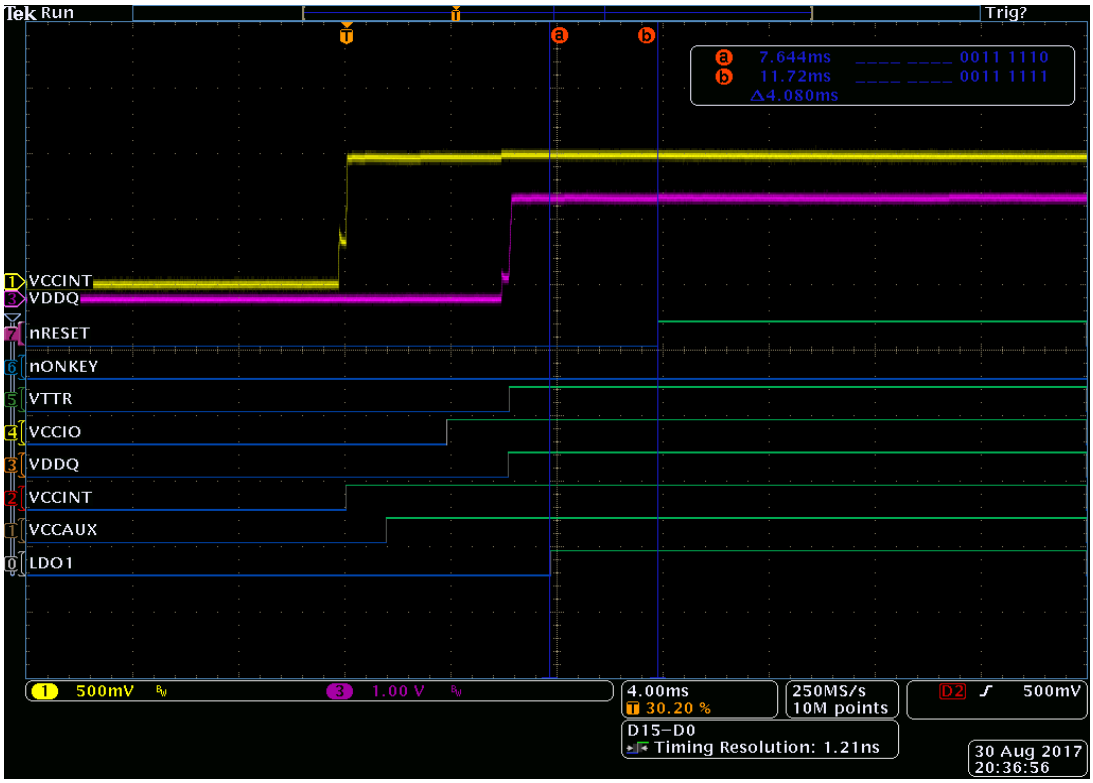

Figure 7: Spartan-7 Power-On Sequence

4.4.2 Buck Efficiency

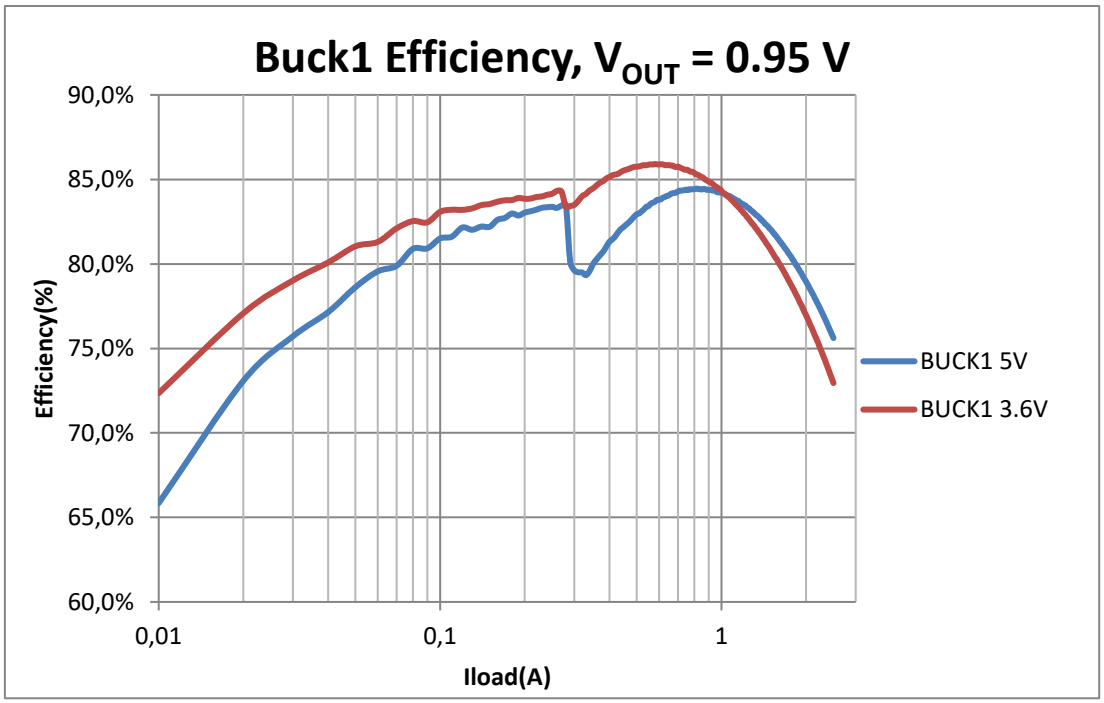

Figure 8: Buck1 Efficiency with V_{OUT} = 0.95 V and V_{IN} = 5 V and 3.6 V

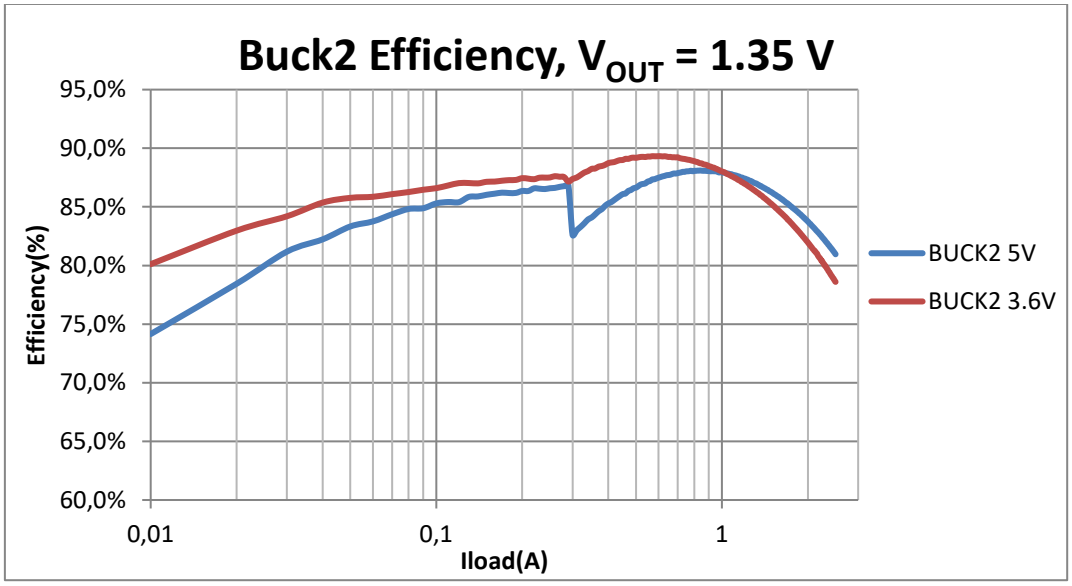

Figure 9: Buck2 Efficiency with V_{OUT} = 1.35 V and V_{IN} = 5 V and 3.6 V

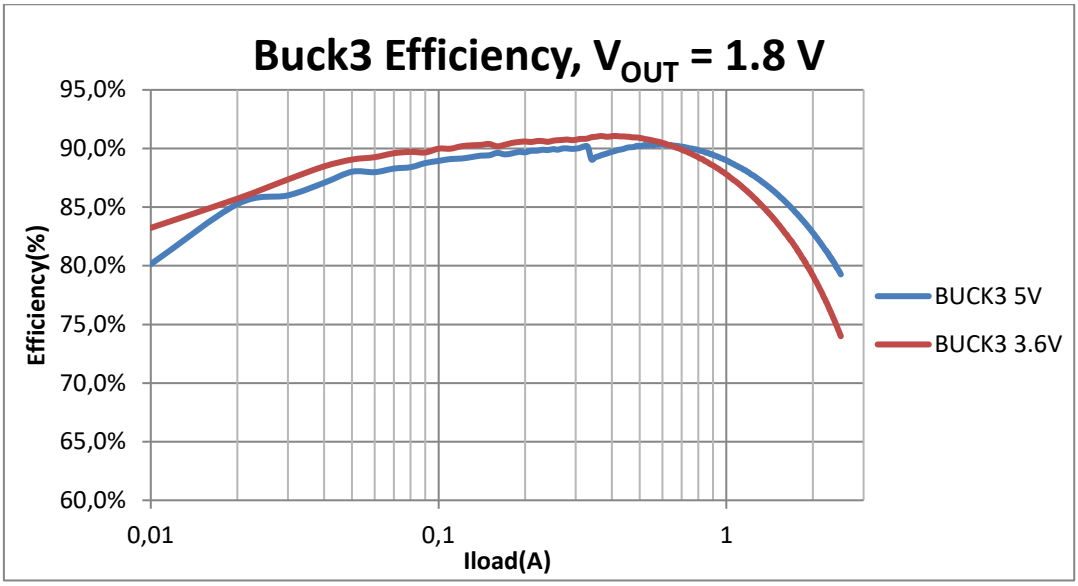

Figure 10: Buck3 Efficiency with V_{OUT} = 1.8 V and V_{IN} = 5 V and 3.6 V

4.4.3 Static Load Regulation

The following static load regulation plots show the variation on the output voltage over a sweep of the load. The buck regulators were running in Auto mode. The change in slope at approximately 300 mA is where the buck transitions from PFM to PWM.

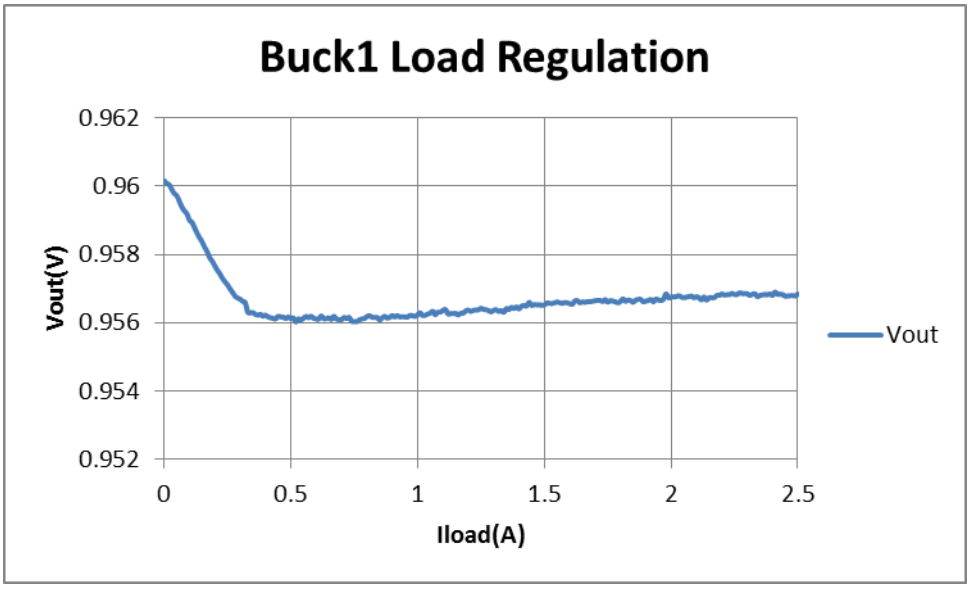

Figure 11: Buck1 Static Load Regulation

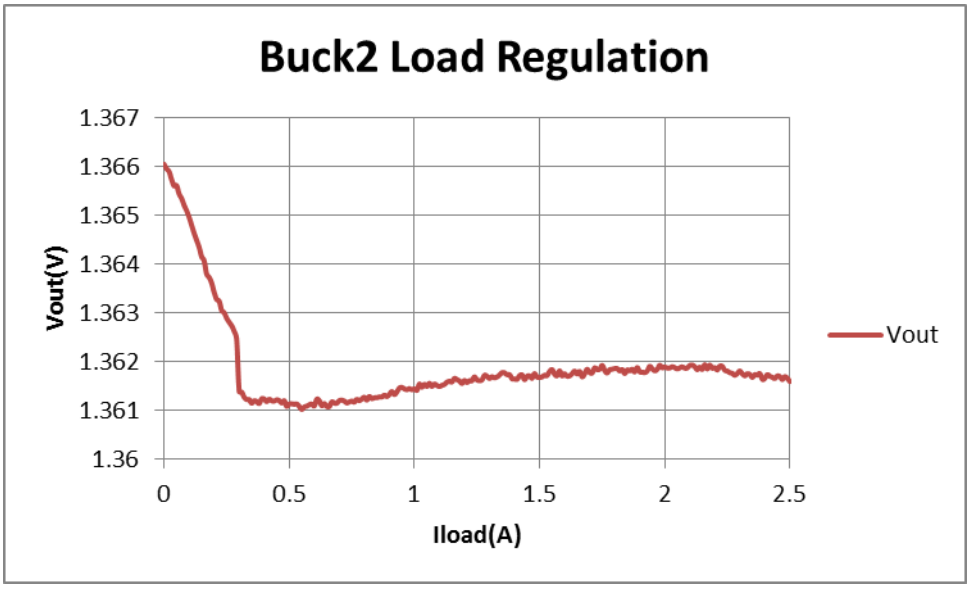

Figure 12: Buck2 Static Load Regulation

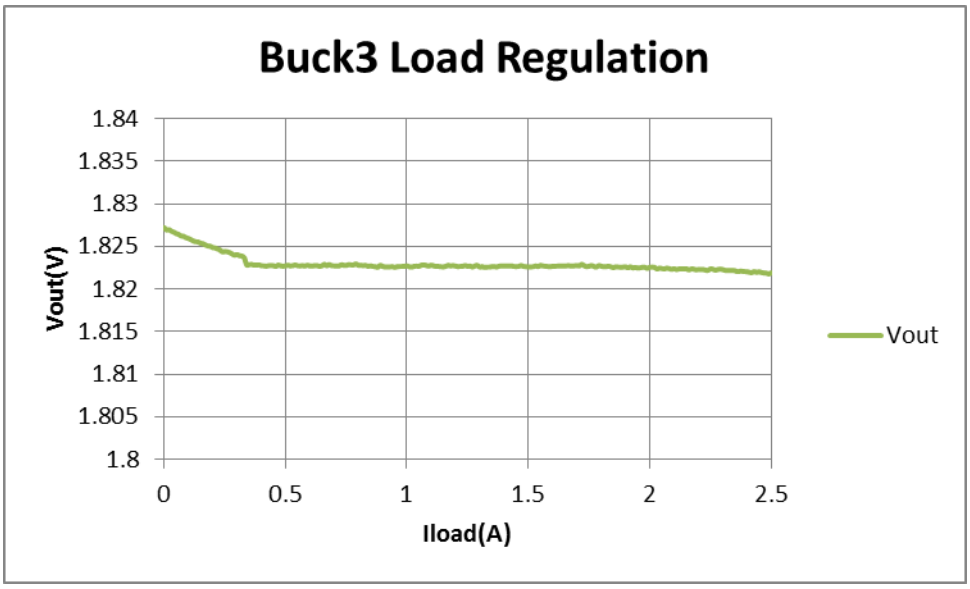

Figure 13: Buck3 Static Load Regulation

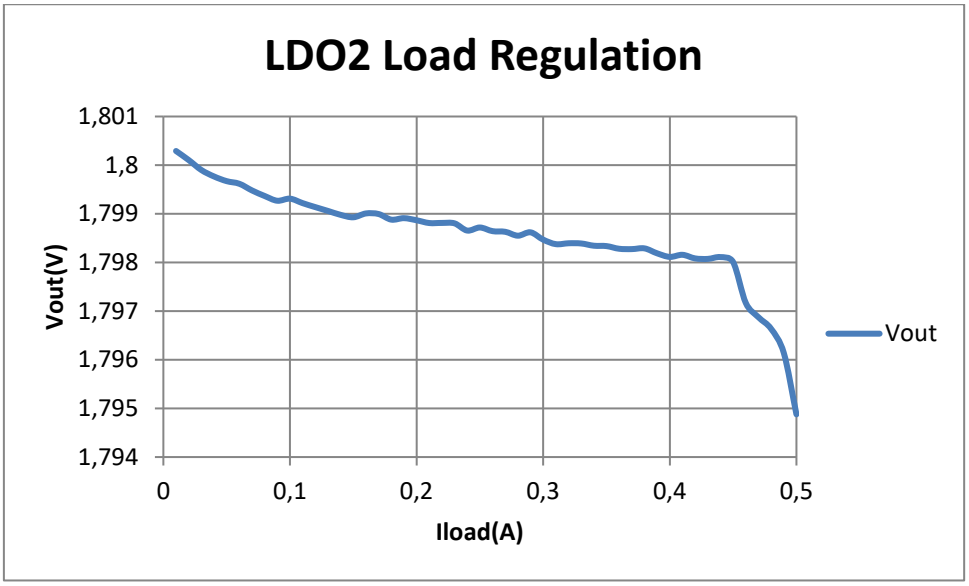

Figure 14: LDO2 Static Load Regulation

4.4.4 Buck Transient Load Regulation

For the transient measurements in this section, the oscilloscope is configured as follows:

- Channel1 (Yellow) shows the regulator output.
  The output was AC coupled, The buck was set to 0.95 V. The Min and Max measurements show the maximum excursion during the transient event.
- Channel 2 (Blue) shows the transient load being applied.
  The Low and High measurements were configured to show the levels of the current pulse waveform. The pulse duration was set to 10 µs.
- Channel 3 (Magenta), where shown, displays the DC coupled output voltage.
- The “a” and “b” horizontal cursors show the Xilinx specification limits for the specific voltage rail.

In Table 5, Table 6, and Table 7, the results are given for the transient as a percentage of the maximum load for the regulator. For example, 625 mA is 25 % of 2.5 A. The ±3 % specification is then calculated in mV for comparison against the measured result.

Table 5: VCCINT Transient Load Results

VCCINT (V)	Transient Load			Spec. Limit (mV)		Measured (mV)	
	Low (mA)	High (mA)	%	-3%	3%	Min	Max
0.95	310	990	25 %	-28.5	28.5	-14	13.2
0.95	310	1310	40 %	-28.5	28.5	-20.8	18.4

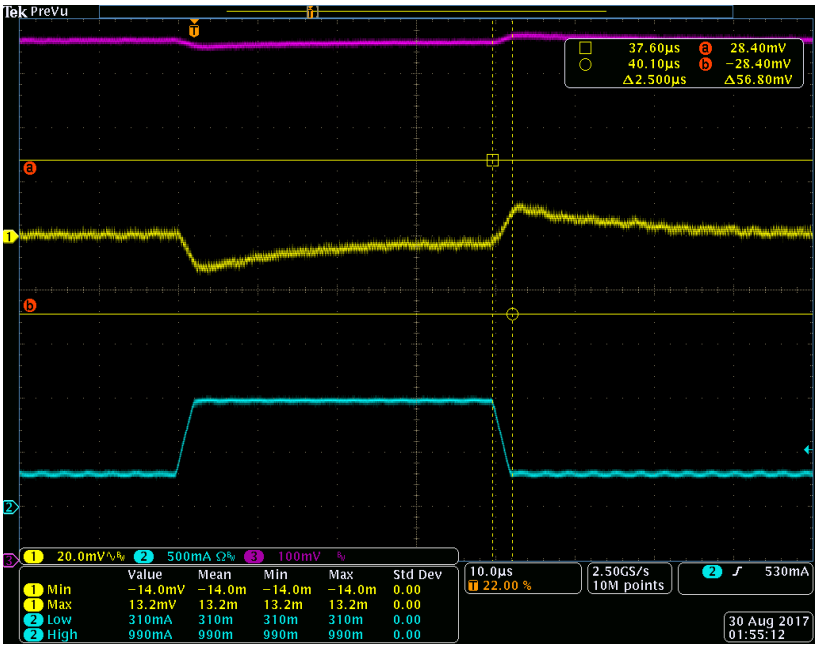

Figure 15: VCCINT (Buck1) Transient Response, 310 mA to 990 mA step

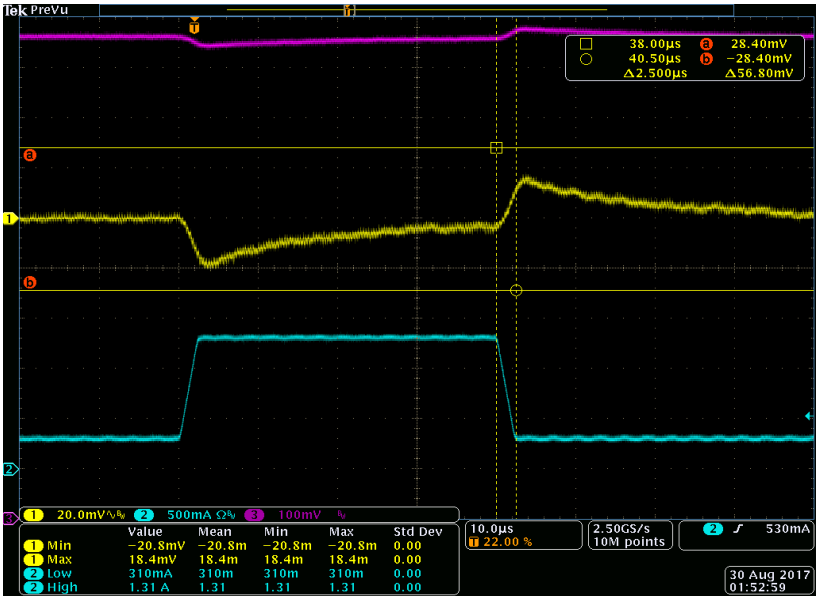

Figure 16: VCCINT (Buck1) Transient Response, 1 A Step

Table 6: VDDQ Transient Load Results

VDDQ (V)	Transient Load			Spec. Limit (mV)		Measured (mV)	
	Low (mA)	High (mA)	%	-3%	3%	Min	Max
1.35	310	1310	40 %	-40.5	40.5	21.2	20.4
1.5	310	1310	40 %	-45	45	-20.4	21.2

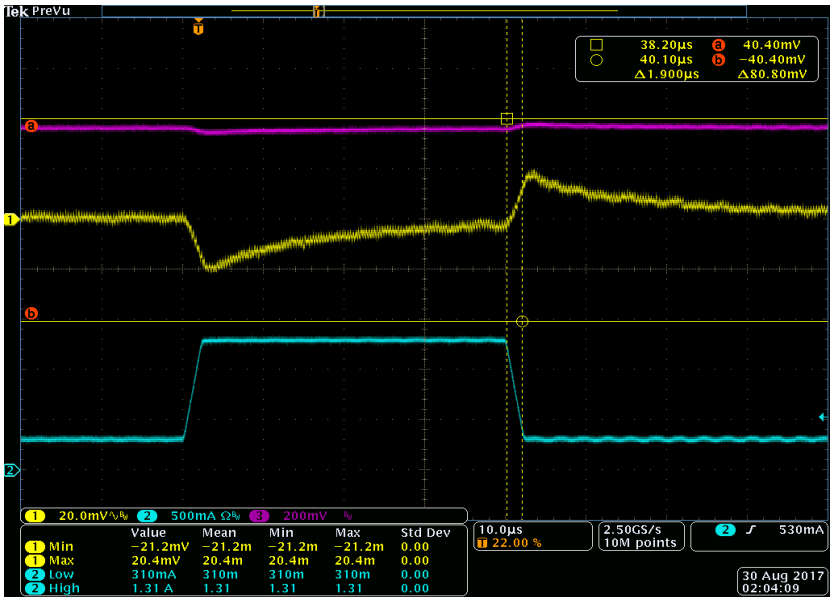

Figure 17: VDDQ (Buck2) Transient Response, V_{OUT} = 1.35 V, 1 A Step

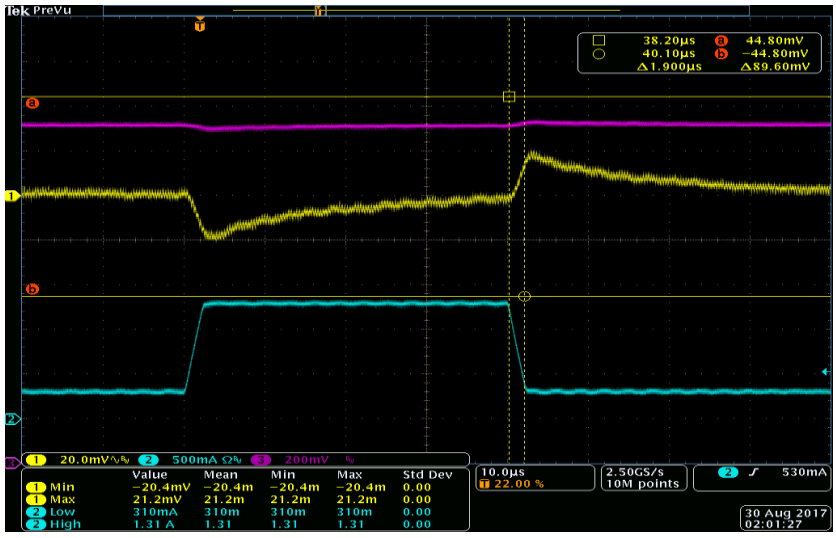

Figure 18: VDDQ (Buck2) Transient Response, V_{OUT} = 1.5 V, 1 A Step

Table 7: VCCIO Transient Load Results

VCCIO (V)	Transient Load			Spec. Limit (mV)		Measured (mV)	
	Low (mA)	High (mA)	%	-3%	3%	Min	Max
2.5	310	1310	40 %	-75	75	-41	35
2.5	310	1570	50 %	-75	75	-55	49
3.3	310	1310	40 %	-99	99	-45	37
3.3	310	1570	50 %	-99	99	-55	51

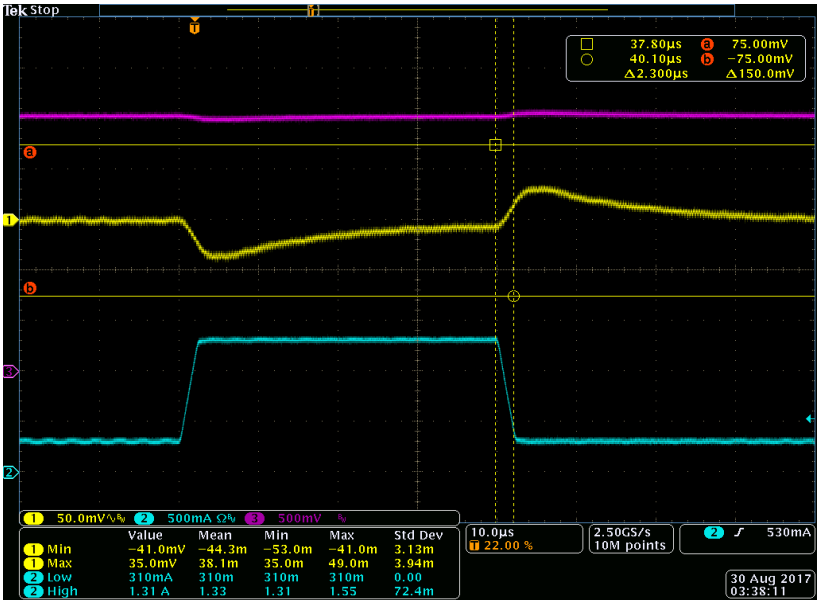

Figure 19: VCCIO (Buck3) Transient Response, V_{OUT} = 2.5 V, 1 A Step

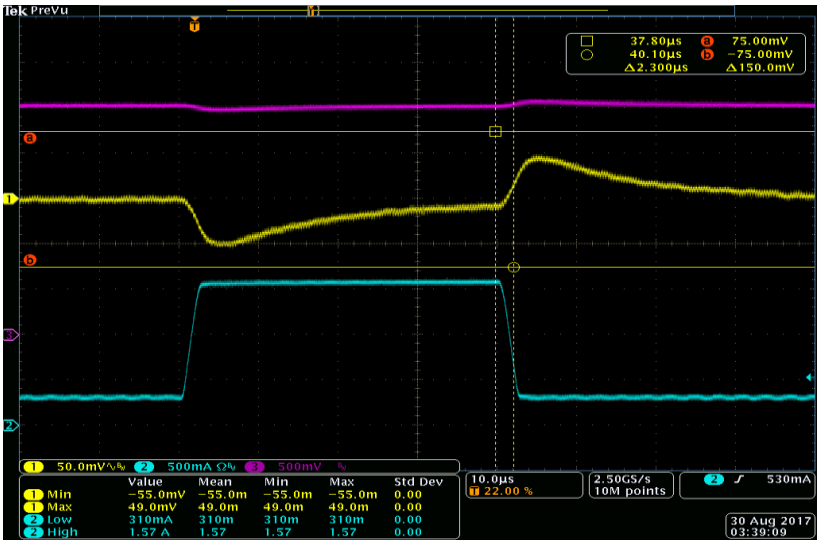

Figure 20: VCCIO (Buck3) Transient Response, V_{OUT} = 2.5 V, 1.25 A Step

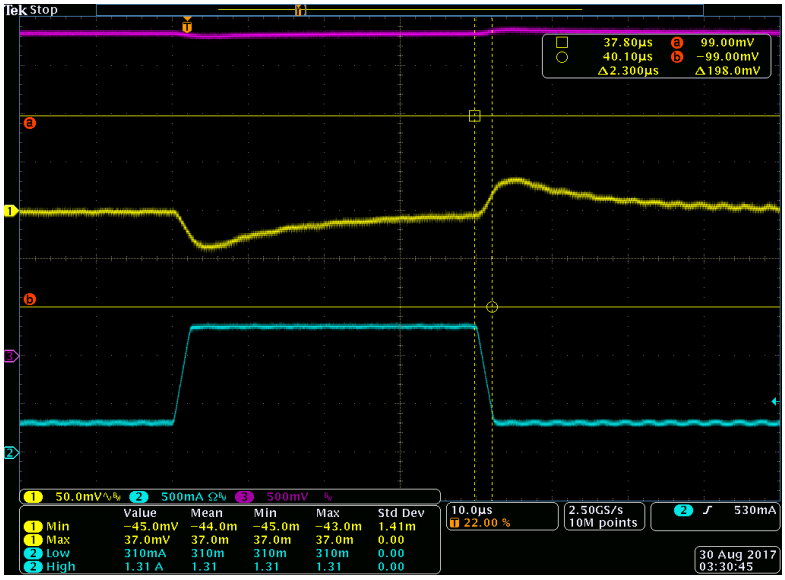

Figure 21: VCCIO (Buck3) Transient Response, V_{OUT} = 3.3 V, 1 A Step

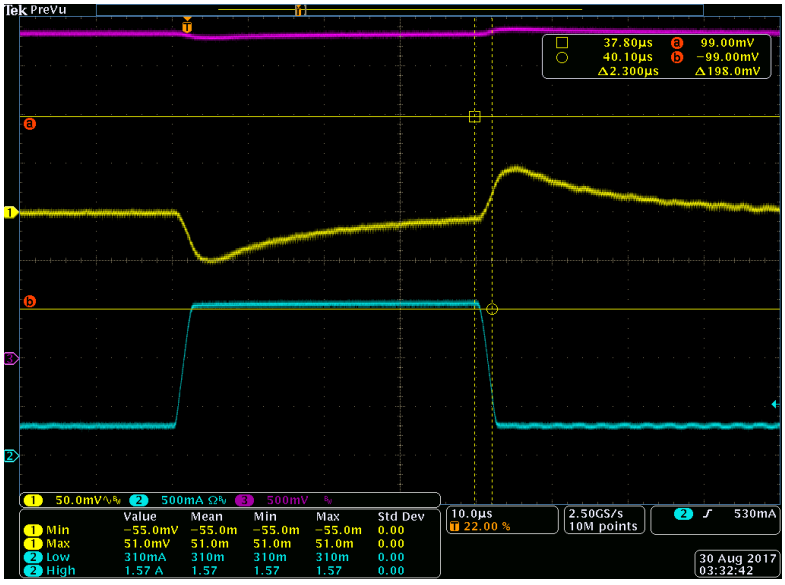

Figure 22: VCCIO (Buck3) Transient Response, V_{OUT} = 3.3 V, 1.25 A Step

4.4.5 Reference Measurements

The operating performance of the PMIC is affected by the performance of the voltage and current references. This section shows the performance of the voltage and current references over temperature.

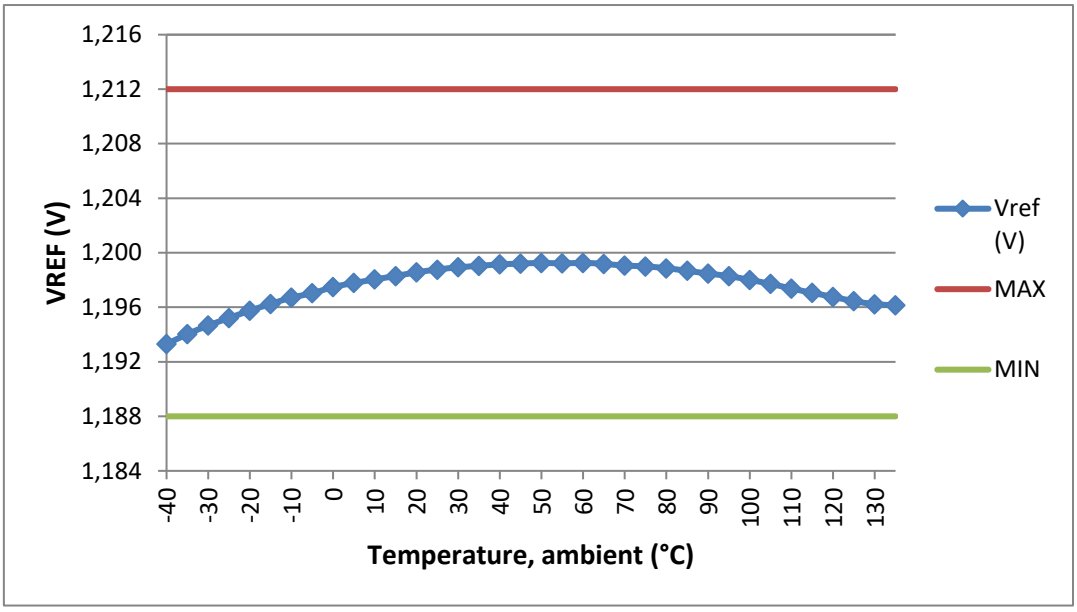

Figure 23: V_{REF} Over Temperature

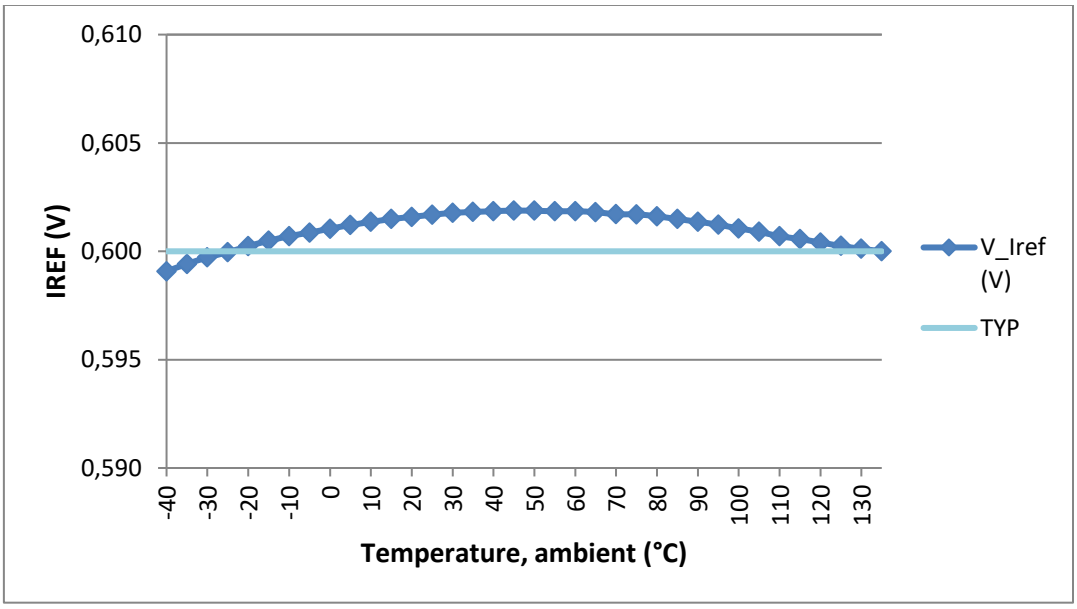

Figure 24: I_{REF} Over Temperature

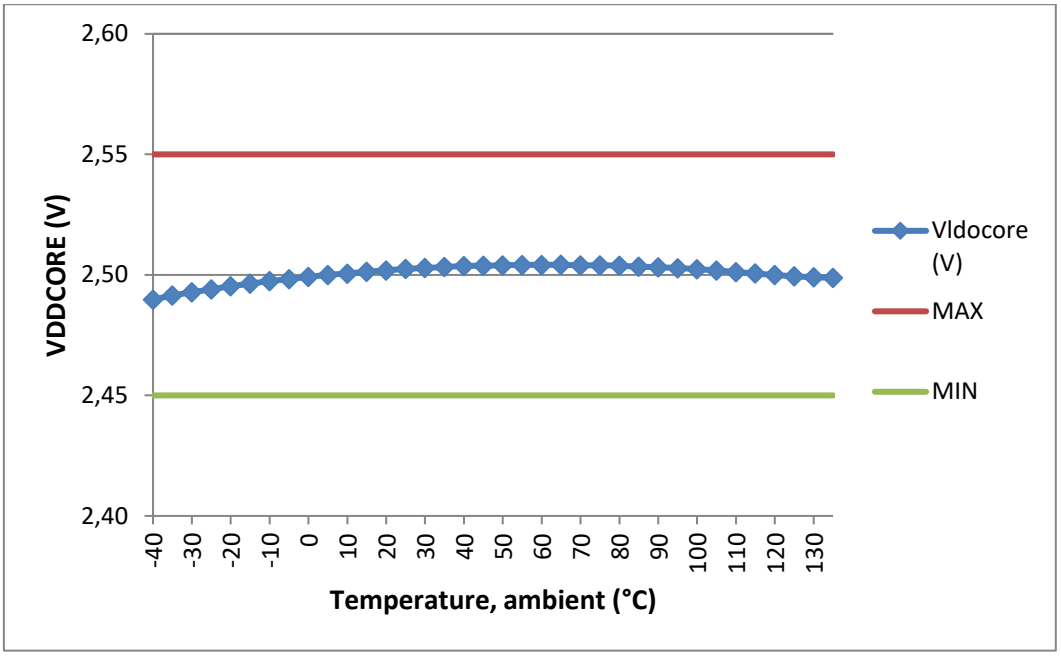

Figure 25: VDDCORE Over Temperature

5 Conclusions

By providing a high level of integration and high efficiency in a small PCB footprint, the Dialog DA9062 can be seen to be an ideal partner to the Xilinx Spartan-7 family of devices.

Revision History

Revision	Date	Description
1.0	01-Jun-2017	Initial version.
1.1	31-Aug-2017	Added Section: Bench Measurement.
1.2	10-Jan-2018	Corrected application note number.
1.3	18-Feb-2022	File was rebranded with new logo, copyright and disclaimer

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Status	Definition
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APPROVED or unmarked	The content of this document has been approved for publication.

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