



S-RIO Gen2 Switch Signal Quality Optimization Application Note

Formal Status
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About this Document

This document discusses when and how to change the SerDes parameters for IDT Gen2 S-RIO switches in order to optimize signal quality. Topics discussed include the following:

- [Signal Quality Measurement](#)
- [Signal Quality Optimization](#) using Fabric Embedded Tool's RapidFET JTAG (Enhanced) Diagnostic Tool

Revision History

October 14, 2011, Formal

Updated register references as per recent changes to the Gen2 user manuals.

August 4, 2011, Preliminary

Updated [Signal Quality Measurement](#) and [Figure 3](#).

February 19, 2011, Preliminary

First release of the document.

Introduction

Gigahertz signaling rates require multiple disciplines for successful operation, including careful attention to board layout, clocking, and power. IDT Gen2 S-RIO switches can achieve bit error rates of 1 in 10^{15} using default settings over short- and medium-reach channels, as defined by the *RapidIO Specification (Rev. 2.1)*, Part 6.

When the channel characteristics exceed medium reach, it may be necessary to improve the signal quality by altering the transmit and/or receive Serializer/Deserializer (SerDes) coefficients. The first step in determining if optimization is necessary is to measure the signal quality of the channel, and if it does not meet application requirements, to perform signal quality optimization.

Note that signal quality optimization is intended to overcome inter-symbol interference (ISI) within a compliant channel. Signal quality optimization may be able to overcome signal degradation caused by design defects (cross talk, excessive reflection, or attenuation) in some cases, but is not intended for this purpose. Signal quality optimization is not a substitute for good workmanship.

Signal Quality Measurement

There are several indicators of the aggregate signal quality for all lanes of a RapidIO port. If the following three conditions are true, the signal quality of all lanes of a port is acceptable:

- Port n Error and Status CSR[PORT_OK] remains 1, referred to as "PORT_OK" in the remainder of this document.
- Port n Error and Status CSR[OUTPUT_ERR] remains 0 when cleared
- Port n Error and Status CSR[INPUT_ERR] remains 0 when cleared

If PORT_OK is not asserted, or if either OUTPUT_ERR or INPUT_ERR becomes 1 after being cleared, this indicates a signal quality issue exists for at least one direction of the link.

A RapidIO port is composed of one or more lanes. It is possible to determine the signal quality for a port, and for each lane connected to the port. A functional measure of the signal quality of a port or lane is the bit error rate (BER). A bit error is the inversion of a single transmitted bit from its intended value. The BER is the probability that any one bit will be received inverted from its intended value. The *RapidIO Specification (Rev. 2.1)* requires processing elements to demonstrate a BER of 10^{-12} , and to be capable of a BER of 10^{-15} .

Bit errors are detected in the following ways in the IDT Gen2 SRIO switches:

- Invalid 10-bit code group – RapidIO encodes each 8 bits of data sent using a 10-bit code with excellent electrical and fault detection properties. Single-bit transmission errors always result in detection of at least one invalid 10-bit code group. Note that this invalid 10-bit code group may not be the one that experienced the single bit error. Invalid code-groups may result from a prior error which altered the running disparity of the bit stream but which did not result in a detectable error at the code-group in which the error occurred. Invalid 10-bit code groups are counted for each lane in the Lane n Status 0 CSR[ERR_8B10B] field.
- Invalid Cyclic Redundancy Code (CRC) – The correctness of RapidIO control symbols and packets can be checked using the standard CRC codes. CRC code failures are detected by the port receiving the packet or control symbol. Due to lane striping, it is not possible to determine which lane of a multi-lane port is responsible for the transmission error that caused the CRC check to fail. CRC code failures can be counted using the Port n Error Rate CSR[ERR_RATE_CNTR] field.
- Protocol Error – A valid 10-bit code group or control symbol was received at a time that is not compliant with the RapidIO protocol. An example of a protocol error is reception of a 10-bit data code group within the IDLE1 sequence. Protocol failures are detected by the port that receives the packet or control symbol. It is not possible to determine which lane of a multi-lane port is responsible for the transmission error that caused the protocol error. Protocol errors can be counted using the Port n Error Rate CSR[ERR_RATE_CNTR] field.

To determine the rate of invalid 10-bit code group reception, read the Lane n Status 0 CSR[ERR_8B10B] field repeatedly for a time period that corresponds to the bit error rate expected. For example, if the expected BER is 10^{-12} for a 6.25 Gbaud link, it is necessary to read the Lane n Status 0 CSR[ERR_8B10B] after at least 160 seconds has passed. The more often the register is read in this interval, the higher the maximum bit error rate that can be measured.

Counting invalid CRC and protocol errors requires the RapidIO Error Management Extension per-port error counters to be used. To count CRC and protocol errors for a port, update the registers as listed in [Table 1](#).

Table 1: Port Configuration to Count Physical Layer Errors

Register	Address	Value	Comments
Port n Error Rate Enable CSR	0x1044 + (0x40*port)	0x004E8015	Enable all events that indicate reception of a transmission error by this end of the link.
Port n Error Rate CSR	0x1068 + (0x40*port)	0x00030000	Maximum value of error counter is 0xFF, leak rate is 0, clear error counter value.
Port n Error Rate Threshold CSR	0x106C + (0x40*port)	0x00000000	Disable notification thresholds for physical layer error counts.

Update the registers as listed in [Table 2](#) to determine the current per-port error count. The current value of the register is bit-wise ANDed with the Mask, and bit-wise ORed with the Value. Note that the per-port error count is not cleared when read.

Table 2: Per-Port Error Measurement Programming Model

Register	Mask	Value	Comments
Port n Error Rate CSR	0x000000FF	N/A	Read the Port n Error Rate CSR and extract the ERR_RATE_CNTR field.
Port n Error Rate CSR	0xFFFFFFFF00	0x00000000	Clear the ERR_RATE_CNTR field to 0.

The per-lane invalid 10-bit code group counter, ERR_8B10B, is the preferred method for measuring signal quality when the system is being used by a customer. The reason is that this counter is not linked to the switches' event notification or fault isolation mechanisms.

The ERR_8B10B field must always be used to diagnose signal quality for multi-lane (2x, 4x) ports. The lane that caused a per-port error cannot be determined from the port level, so per-lane error detection mechanisms must be used. The ERR_RATE_CNTR field can be used to determine the aggregate signal quality for a multi-lane port. The ERR_RATE_CNTR can be used to diagnose signal quality for single-lane (1x) ports, as long as the event notification and fault isolation mechanisms are not required for system operation.

Signal Quality Optimization

Signal quality optimization involves changing Serializer/Deserializer (SerDes) coefficients and using signal quality measurements to determine which coefficients result in optimal signal quality.

This section is organized as an overview of the SerDes coefficient programming model implemented in the RapidFET JTAG (Enhanced), followed by step-by-step instructions for optimizing signal quality using the RapidFET JTAG (Enhanced).

It must be pointed out that there is no magic coefficient value that works for all topologies. Though variations eye diagrams taken of the signal at the receiver end of a link might not be visible when examined, it is quite normal that similar topologies may yield different coefficients. However, board to board variations of the same topology should still yield the same coefficients.

SerDes Programming Model

Signal quality optimization requires configuration of two sets of coefficients: the far-end link partner SerDes transmission coefficients, and the local receiver SerDes DFE coefficients. This section of the application note discusses what needs to take place in order to optimize the transmit and receive coefficients of a lane and port. These processes are embedded into the RapidFET JTAG (Enhanced) tool so specific register accesses are performed transparently to the user.

Transmitter Coefficients

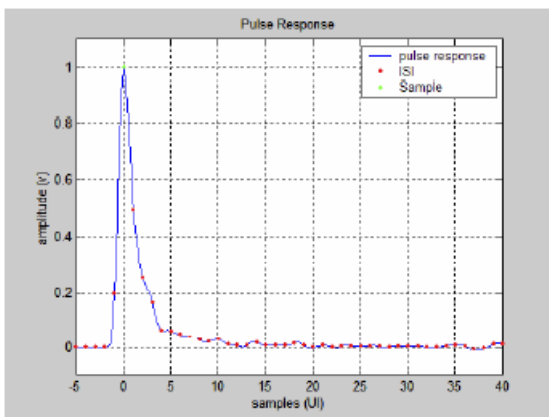
IDT Gen2 switch SerDes transmission coefficients are listed in [Table 3](#). Note that these coefficients must be set for each lane of a multi-lane port.

Table 3: IDT Gen2 Switch SerDes Transmission Coefficients

Coefficient Name	Register	Field	Comments
Transmission Strength	Lane n Control Register	TX_AMP_CTRL	-
Transmit Pre-Cursor Emphasis	Lane n Status 3 CSR	NEG1_TAP	Only has effect when AMP_PROG_EN is 1.
Transmit Post-Cursor Emphasis	Lane n Status 3 CSR	POS1_TAP	Only has effect when AMP_PROG_EN is 1.

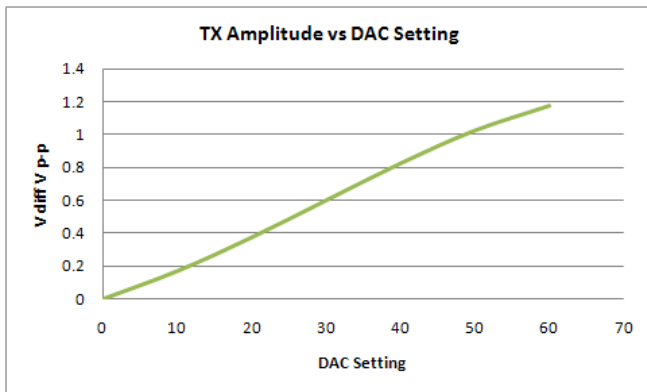
The effects on a bit imposed onto a transmission line can be seen in the transient response shown below. The goal of optimizing the transmitter coefficients is to maximize the signal amplitude at 0UI and minimize the tail that extends beyond 1UI.

Figure 1: Example Transient Response of a PCB Trace Showing Signal Spread into Subsequent Bit Times



Signal amplitude losses are the greatest visible effect when conducting a 6.25 Gbps signal through PCBs, connectors and cables. Figure 2 shows the range of amplitude values to which the transmitter can be programmed.

Figure 2: Graph of Transmitter Amplitude DAC Setting versus Differential Voltage



In compensating specifically for high frequency losses in the topology, the application of post-emphasis in the waveform can be used to improve the signal quality being received. Figure 3 demonstrates the changes that take place on the waveform when the post-emphasis is applied.

The PRE and POST emphasis settings affect bit sequences of the same value only when there are two or more bits of the same value in sequence. In a sequence of three bits of the same value, the PRE coefficient would affect bits one and two, but not the third or last bit. The POST coefficient would affect bits two and three of the sequence but not the first bit. The amplitude control affects all three bits equally. When dealing with signal losses in a topology, the amplitude control is the primary variable which is increased. The POST coefficient has the next greatest effect on the signal, while the PRE coefficient has the least amount of perceptible effect.

Figure 3: Simulation Output Showing the Effect on the Waveform by Changes in Post-Emphasis Coefficient

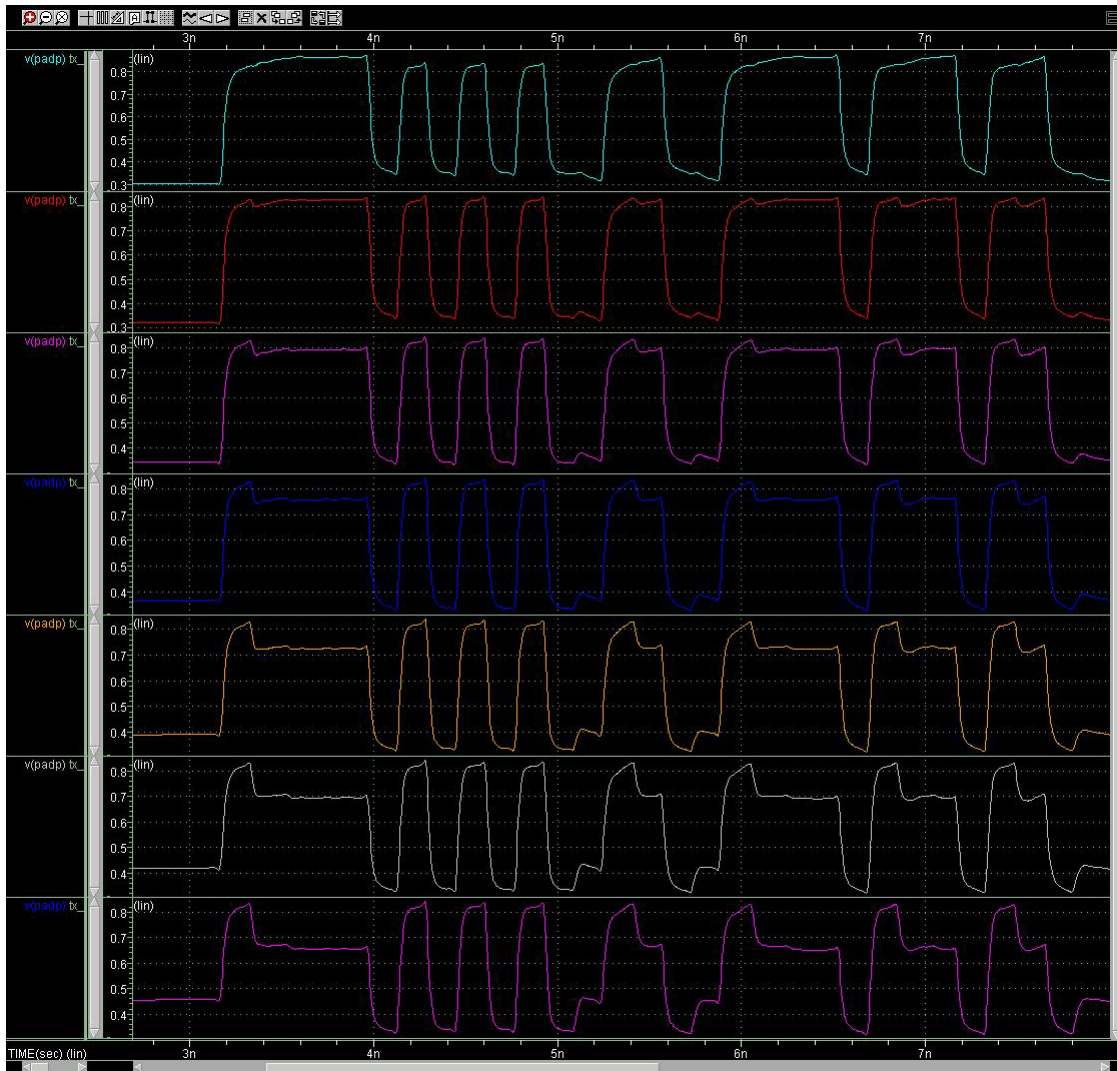
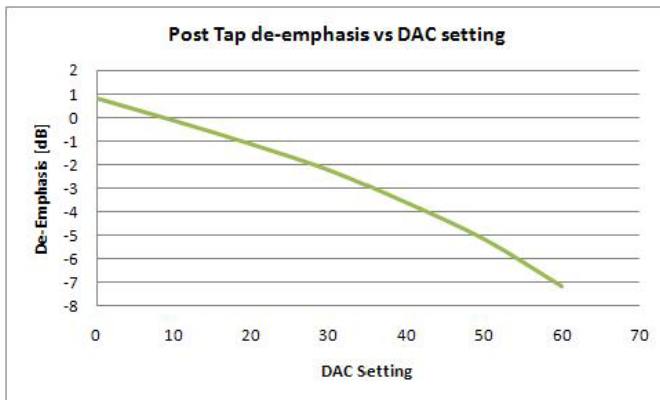


Figure 4 documents the effect on the signal amplitude in dB when the POST coefficient is varied.

Figure 4: Transmitter Post-Emphasis DAC Setting versus Effect in dB on Nominal Amplitude



The third transmitter coefficient controls the PRE- emphasis of the waveform. This coefficient varies the leading edge of a multi-bit sequence. Figure 5 shows the effect on the waveform shape when the pre-emphasis coefficient is varied.

Figure 5: Simulation Output Showing the Effect on the Waveform by Changes in Pre-Emphasis Coefficient

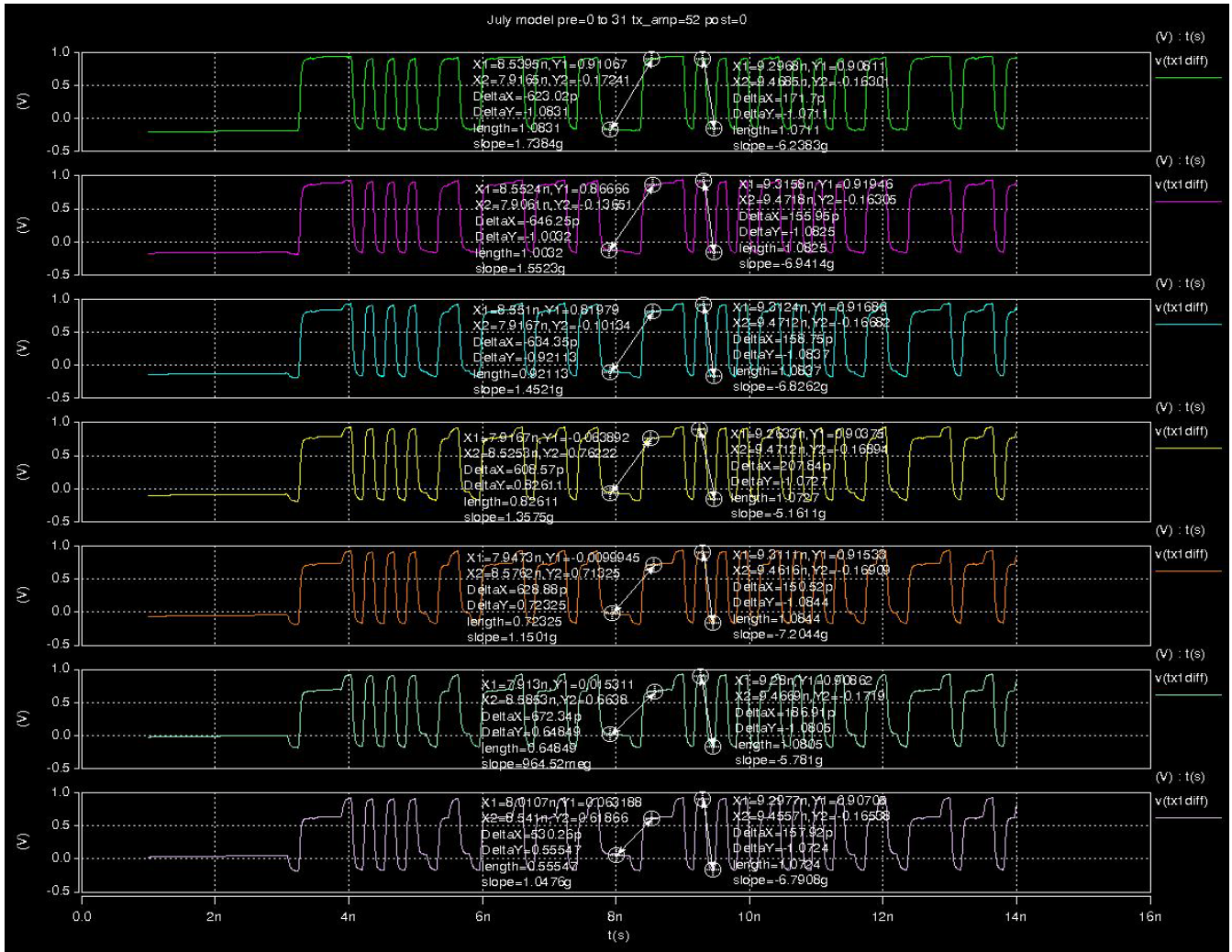
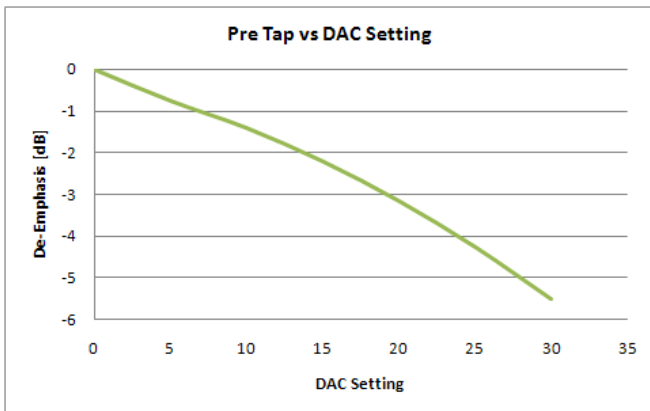


Figure 6 shows the effect in amplitude in dB of the pre-emphasis coefficient.

Figure 6: Transmitter Pre-Emphasis DAC Setting versus Effect on Nominal Amplitude in dB



Receiver Coefficients

IDT Gen2 switch SerDes receiver DFE coefficients and their names are listed in Table 4. Note that these coefficients are lane specific and must be configured for each lane of a multi-lane port.

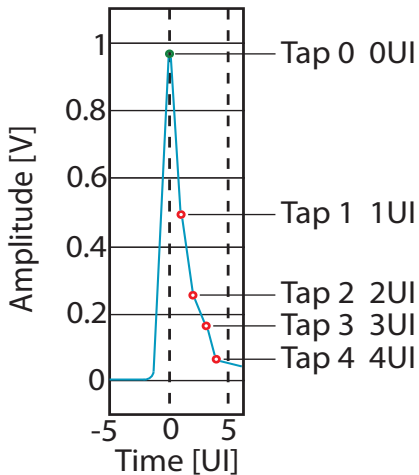
Table 4: IDT Gen2 Switch SerDes Receiver DFE Coefficients

Coefficient Name	Register	Field	Comments
Tap 0	Lane n DFE 2 Register	TAP_0_CFG	Input amplifier gain setting
Tap 1	Lane n DFE 2 Register	TAP_1_CFG	Coefficient for 1UI
Tap 2	Lane n DFE 2 Register	TAP_2_CFG	Coefficient for 2UI
Tap 3	Lane n DFE 2 Register	TAP_3_CFG	Coefficient for 3UI
Tap 4	Lane n DFE 2 Register	TAP_4_CFG	Coefficient for 4UI

The goal of the receiver coefficients is to aid in extracting the correct data from the received signal which can be represented by the transient response shown in Figure 7. In the Gen2 switch SerDes, coefficient 0 is a variable gain amplifier (VGA). It's purpose is to increase the signal amplitude to be above the detection thresholds of the slicer (data sampler). Increasing the VGA gain has both desired and undesired effects. The desired effect is that it increases the signal amplitude. The undesired effect is that it also increases the amplitude of the noise received along with the signal. This noise may be partially removed by the application of a linear equalizer, at the expense of some signal amplitude. The Gen2 switch SerDes receiver does not contain a linear equalizer so it is imperative that only enough gain be applied to the signal that will support a BER approaching 10E-15.

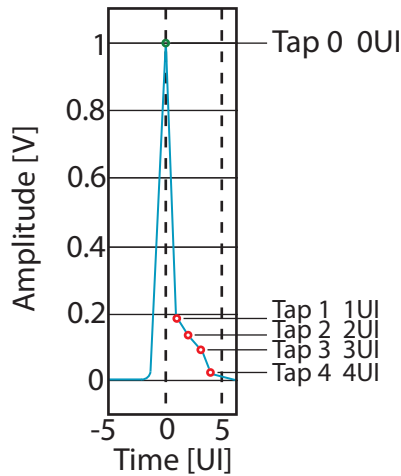
Figure 7 shows the positions on the waveform where the coefficients will have an effect. The desired effect is to lower the amplitude of the tail in the transient response that spans one to four UI and bring that part of the waveform down below the detection threshold of the slicer (data sampler).

Figure 7: Position of Taps on Impulse Response Relative to Time



In this example the detection threshold of the slicer is 200mV. In order to correctly sample bits that follow after the initial data bit, the tap coefficients apply a voltage that forces the tail down below the detection voltage. The further the tail can be brought down towards zero, the higher probability of obtaining the correct bit value when the sample is taken. Figure 8 graphically demonstrates the effect of the applied tap coefficients.

Figure 8: Effect of Taps on Impulse Response after Application



Control of the Coefficients

In order to obtain full manual control of receiver DFE coefficients, configure the following registers and fields as specified in [Table 5](#). The current value of the register is bit-wise ANDed with the Mask, and bit-wise ORed with the Value. In the Lane n DFE 2 Register, the adaptive DFE function must be turned off and the ability of the adaptive DFE to access the coefficients must be disabled. In the Lane n DFE 2 Register, the ability to enter coefficients through register writes must be enabled.

Please note that the RapidFET JTAG (Enhanced) tool takes care of these bit operations for you in the background but that we want you to know what's taking place.

Also note that the SerDes DFE coefficients must be programmed for each lane of a multi-lane port.

Table 5: Programming Model for IDT Gen2 Switch SerDes DFE Coefficients

Register	Address	Mask	Value	Comments
Lane n DFE 1 Register	0xFF8028 + (0x100*lane)	0xFFFF80FFF	0x0007F000 or 0x0003F000	If Device Information CAR[MINOR_REV] is 0, then the value should be 0x0007F000. If MINOR_REV is not 0, then the value should be 0x0003F000.
Lane n DFE 2 Register	0xFF802C + (0x100*lane)	0xFFFFFFFFE	0x00000001	Ensure that CFG_EN bit is set for consistent programming.

To change the SerDes receiver DFE coefficients, perform the following register writes:

1. Set the desired Tap0–4 values into the Lane n DFE 2 Register, with the CFG_EN field cleared to 0.
2. Set the Lane n DFE 2 Register[CFG_EN] field to 1 while keeping the Tap 0–4 values constant to latch in the values.

Signal Quality Optimization Procedures

The process of optimizing the link signal quality is very repetitive and time consuming. The processes and algorithms have been implemented into the RapidFET JTAG (Enhanced) product to relieve users from the burden of writing their own optimization tools. The following sections describe how to use the RapidFET JTAG (Enhanced) tool in order to optimize the signal quality of the links.

Signal quality optimization is a two-step procedure:

1. Determine the SerDes transmission coefficients, which allow the link to operate correctly
2. Search SerDes DFE coefficients for those that provide optimal signal quality

The first step is a manual process of selecting and installing the transmit strength and Post emphasis tap settings. Typically the two coefficients are progressively increased until either a PORT_OK status appears on the ports or until the coefficients are at their maximum values.

The second step utilizes the DFE Scan command button in the SerDes Configuration window. This is a fast search that tries to find coefficients that offer the lowest BER that will allow a port to train and achieve a PORT_OK status.

The second step also utilizes the DFE Adjust button which launches a long running search algorithm that tries to optimize the coefficients determined by the DFE Scan performed earlier.

It should be noted that transmit and DFE coefficients can be determined through simulation of the channel using various modelling technologies (HSPICE, IBIS-AMI). Modelling can be used to guide the search for optimal transmit and DFE coefficients.

SerDes Transmission Coefficient Optimization

When optimizing SerDes transmission coefficients, the link partner's DFE should be disabled by setting registers and values as described in [Table 6](#). The RapidFET JTAG (Enhanced) tool takes care of this for you in the background but it is necessary for the user to understand what is happening when a scan is launched.

Table 6: Programming Model to Disable IDT Gen2 Switch SerDes DFE

Register	Address	Mask	Value	Comments
Lane n DFE 1 Register	0xFF8028 + (0x100*lane)	0xFFFF FFFF	0x00000000 or 0x00040000	If Device Information CAR[MINOR_REV] is 0, then the value should be 0x00000000. If MINOR_REV is not 0, then the value should be 0x00040000.

The default SerDes transmission coefficients support successful link initialization for channels that are compliant to the RapidIO short-reach specifications. Medium-reach channels can operate successfully with the default SerDes settings but may require increasing the post-cursor emphasis to achieve target bit error rates.

RapidIO long-reach channels may require increasing the SerDes transmission strength to its maximum value (0x3F), and then increasing the post-cursor emphasis setting until the link partner's PORT_OK bit is asserted. The available signal drive is maximized when the signal amplitude and post-cursor emphasis settings are at their maximum (0x3F) values.

In the Transmitter section of the SerDes Configuration window, see [Figure 12](#), the user is required to increase the Strength and Post coefficients manually in order to help the DFE Scan seek and find receiver tap coefficients that allow a PORT_OK to be established.

While it is possible that varying the pre-cursor emphasis settings can yield improved signal quality, signal quality is usually optimal when the pre-cursor emphasis setting remains 0. For transmission coefficients, see [Table 3](#).

Using the RapidFET JTAG (Enhanced) Tool to change the transmitter coefficients

After launching the RapidFET JTAG (Enhanced) tool and connecting to a target device, see [Figure 9](#), right click on the device to bring up the menu and select "Port/Lane Mapping and Control...", see [Figure 10](#).

Figure 9: RapidFET JTAG (Enhanced) Connected to a Device

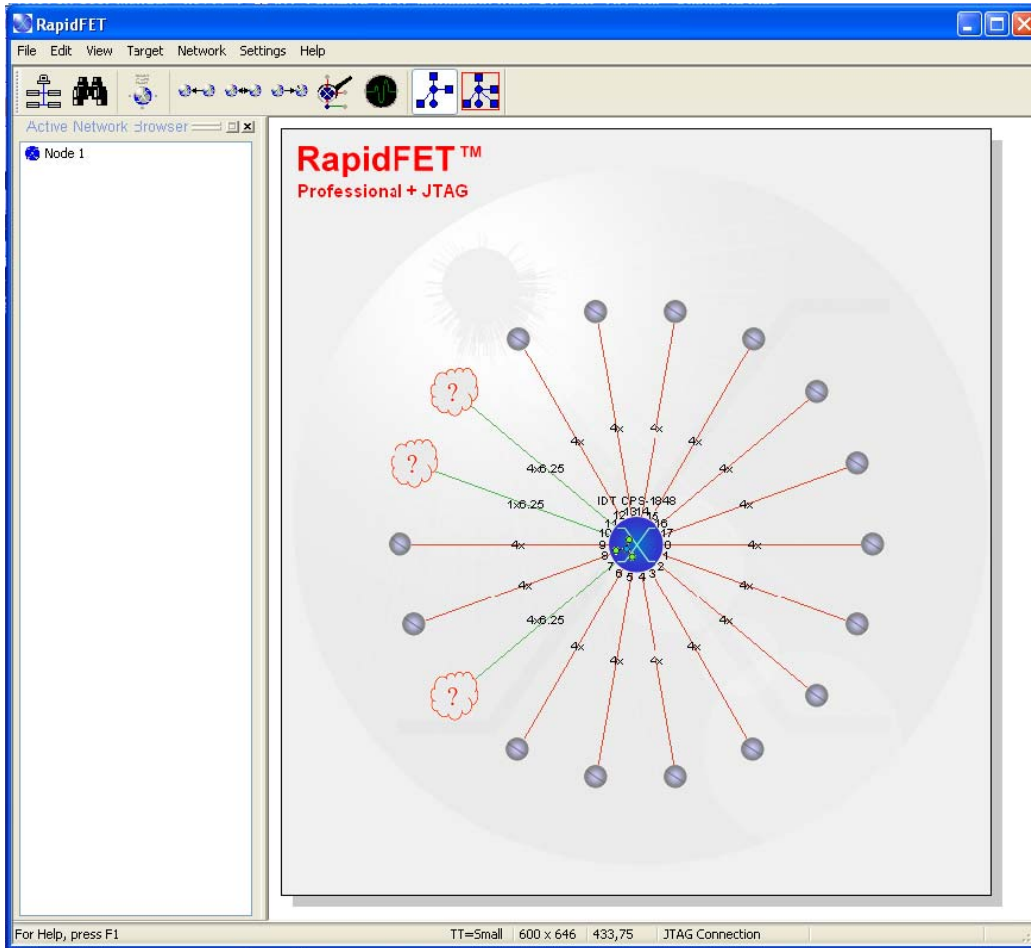
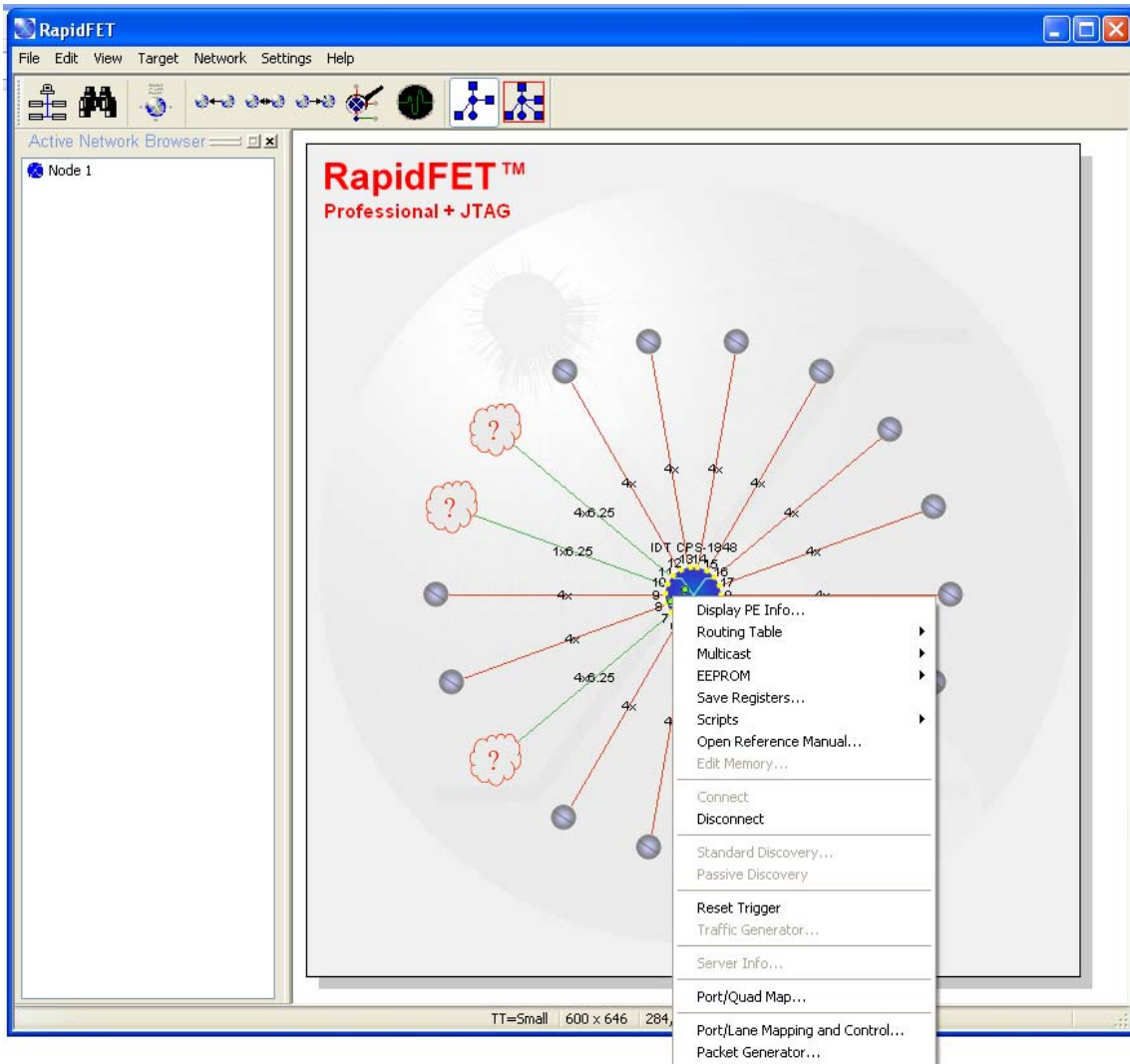


Figure 10: Target Device Pop-Up Menu



The Port/Lane Mapping and Control window that looks like the example in [Figure 11](#) will open showing the list of ports and lanes on the device as well as the PORT_OK status of the ports.

In the case of this example, ports 7 and 11 are looped together and show a PORT_OK status.

Figure 11: Port/Lane Mapping and Control Dialogue Window

Quad#	Quad Config	Port#	Port Width	Port Width Override	Port Status	Port Enable	Port Lockout	Input Enable	Output Enable	IDLE2 Enable	Enable TxFlowCtrl	Flow Control Mode	Idle Seq In Use	PLL#	Lane(s)	Port Speed
0	0	0	x4	No override	Uninit	Y	N	N	N	Y	Y	Tx	IDLE2	0	0-3	6.25
		4	x4	No override	Uninit	Y	N	N	N	Y	Y	Tx	IDLE2	4	16-19	6.25
		8	x4	No override	Uninit	Y	N	N	N	Y	Y	Tx	IDLE2	8	32-35	6.25
1	0	1	x4	No override	Uninit	Y	N	N	N	Y	Y	Tx	IDLE2	1	4-7	6.25
		5	x4	No override	Uninit	Y	N	N	N	Y	Y	Tx	IDLE2	5	20-23	6.25
		9	x4	No override	Uninit	Y	N	N	N	Y	Y	Tx	IDLE2	9	36-39	6.25
2	0	2	x4	No override	Uninit	Y	N	N	N	Y	Y	Tx	IDLE2	2	8-11	6.25
		6	x4	No override	Uninit	Y	N	N	N	Y	Y	Tx	IDLE2	6	24-27	6.25
		10	x4	No override	x1	Y	N	N	N	Y	Y	Tx	IDLE2	10	40-43	6.25
3	1	3	x2	No override	Uninit	Y	N	N	N	Y	Y	Tx	IDLE2	3	12-13	6.25
		7	x4	No override	x4	Y	N	N	N	Y	Y	Tx	IDLE2	7	28-31	6.25
		11	x4	No override	x4	Y	N	N	N	Y	Y	Tx	IDLE2	11	44-47	6.25
		15	x2	No override	Uninit	Y	N	N	N	Y	Y	Tx	IDLE2	3	14-15	6.25

Double clicking on the Lane(s) 28–31 field and Lane(s) 44–47 field will bring up two new windows as displayed Figure 12. These configuration windows show the coefficients contained in each of the lane transmitters and receivers. The buttons you will use most frequently are the REFRESH, DFE SCAN, and ERROR COUNT ENABLE. The REFRESH button is used to update both the device and the window each time a change or set of changes are made to any settings in the windows. Changes can be made to all of the settings and uploaded as a batch.

Figure 12: RapidFET JTAG (Enhanced) SerDes Configuration Windows

Lane	Port Speed	Transmitter				Receiver								10b Loopback Enable	Error Count Enable	Error Count	Error Rate
		Strength	Pre	Post	DFE ON/OFF	DFE Tap 0	DFE Tap 1	DFE Tap 2	DFE Tap 3	DFE Tap 4	DFE Scan	DFE Monitor	DFE Adjust				
28	6.25	52	0	0	ON	8	0	0	0	0	Run	Run	Run	Disabled	Disabled		
29		52	0	0	ON	8	0	0	0	0	Run	Run	Run				
30		52	0	0	ON	8	0	0	0	0	Run	Run	Run				
31		52	0	0	ON	8	0	0	0	0	Run	Run	Run				

Lane	Port Speed	Transmitter				Receiver								10b Loopback Enable	Error Count Enable	Error Count	Error Rate
		Strength	Pre	Post	DFE ON/OFF	DFE Tap 0	DFE Tap 1	DFE Tap 2	DFE Tap 3	DFE Tap 4	DFE Scan	DFE Monitor	DFE Adjust				
44	6.25	52	0	0	ON	8	0	0	0	0	Run	Run	Run	Disabled	Disabled		
45		52	0	0	ON	8	0	0	0	0	Run	Run	Run				
46		52	0	0	ON	8	0	0	0	0	Run	Run	Run				
47		52	0	0	ON	8	0	0	0	0	Run	Run	Run				

If you have a PORT_OK status showing (green background in the Port Status field in the Port/Lane Mapping and Control window) when you open the window, you can check the quality of the link by enabling counting in the “Error Count Enable” selection. If a count accumulates fairly rapidly, greater than one error in one minute of elapsed time, it is recommended that the receiver DFE coefficients be changed. To begin, first increase the Transmitter POST coefficient in order to present a larger signal to the receiver. A value between 40 and 60 would be chosen, 40 for a medium reach scenario, 60 for a long reach scenario. This example is along reach scenario so the Strength parameter also needs to be increased from 52 to 60.

SerDes DFE Coefficient Optimization - What happens when a Scan is launched

DFE coefficients can be used to optimize signal quality when transmission coefficients alone are insufficient to achieve the required signal quality. The process of searching the DFE coefficients is known as “scanning.” A number of different scan methods can be used to search the DFE coefficients, as described in the following sections. See [Figure 13](#) to view the RapidFET JTAG (Enhanced) window that pertains to the following scan methods. These methods all depend on the following points:

- Tap 0 is an amplifier, and so increases noise as well as signal strength.
- Tap number corresponds to the received bit number. Tap 0 is acting on the bit currently being received, Tap 1 values are applied based on the previous bit received, Tap 2 values are applied based on the second last bit received, and so on.
- Tap 0, Tap 1, and Tap 2 have the largest impact on signal quality.

Each of the following scan methods depends on finding a Tap 0 value that is sufficient to achieve PORT_OK.

“Ratio” Scan Method

When using this method, for each Tap 0 value to be scanned, Tap 1, 2, 3, and 4 values are attempted where Tap 2 is 1/2 of Tap 1, Tap 3 is 1/2 of Tap 2, and Tap 4 is 1/2 of Tap 3. Note that ratios other than 1/2 can be used. Typically, Tap 1 values cover the entire allowed range for Tap 1 (0–31). Once the tap values are programmed, a BER measurement is taken for the lane. If the BER is below a selected threshold, this is a “good” tap combination; otherwise, this is not an acceptable tap combination. The optimal tap value is the middle of the largest contiguous range of “good” tap combinations.

The Ratio method is a fast way to approximate tap settings. RapidIO traffic, however, cannot be exchanged while the Ratio method is being executed.

“One-at-a-Time” Scan Method

When using this method, Tap 0 is held constant at an expected good value. All Tap 1 values are then programmed and a BER measurement is taken for each one. Again, tap combinations are determined to be “good” or “bad” based on comparison to a BER threshold. The Tap 1 value selected is the middle of the largest contiguous range of “good” Tap 1 values. This procedure is repeated for Tap 2, 3, and 4 while all other taps are held constant.

There are a couple of variations on the “One at a Time” scan method:

- Perform “One at a Time” scanning with Tap 1–4 values initialized to 0, then perform “One at a Time” scanning with the Tap 1–4 values held to their previously selected values.
- Perform “Ratio” scanning, then perform “One at a Time” scanning with Tap 1–4 values held to their previously selected values.

The One-at-a-time method can be used to approximate tap settings. It can also be used repeatedly to refine tap settings. RapidIO traffic, however, cannot be exchanged while the One-at-a-time method is being executed.

“Adjustment” Scan Method

When using this method, a sequence of taps and delta values is selected. Each tap has the delta value added and subtracted from it. The bit error rate is measured for each tap value. A tap value is permanently changed if the bit error rate has improved. Once all tap values have been tried, if at least one tap value has been changed then all tap values are again tested using the same delta values. If no tap values have been changed, then the delta values are decreased by 1. Adjustment continues until the delta values for all taps are 0, a bit error rate of 0 has been measured, or if the maximum number of adjustment attempts has been performed.

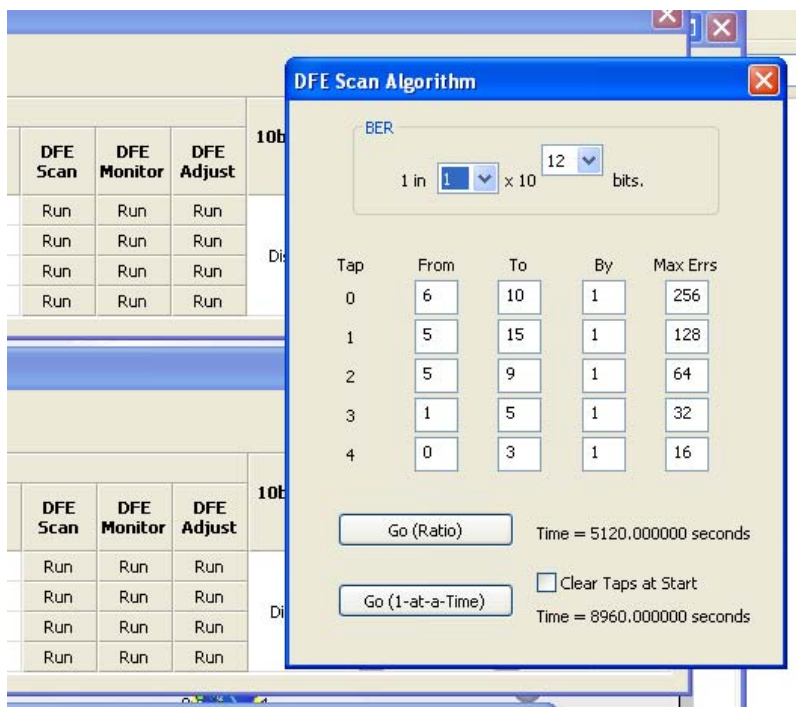
“Adjustment” can be thought of as a version of the “One-at-a-time” method which restricts the range of tap values examined. Typically, adjustment should only be used when good tap values have been found using the “Ratio” or “One-at-a-time” methods.

Adjustment coefficients can be constrained to allow RapidIO traffic be exchanged while the Adjustment method is being executed. Tap 0, 1, and 2 can be excluded from adjustment, and/or the delta amount can be reduced to 1.

The RapidFET JTAG (Enhanced) DFE Scan Algorithm Window

To start a coefficient scan, click the “RUN” button of one of the lanes to be optimized. This will bring up the DFE Scan Algorithm window as shown in Figure 13. In most cases the default settings are sufficient for either scan method, ratio or 1-at-a-time. The minimum desired BER for RapidIO is 10^{-12} , however the lower the BER chosen the longer the scan session will take to run. As can be seen opposite the “Go (Ratio)” button, the estimated run time for the shown settings will be around 5120 seconds (1 hour 25 minutes).

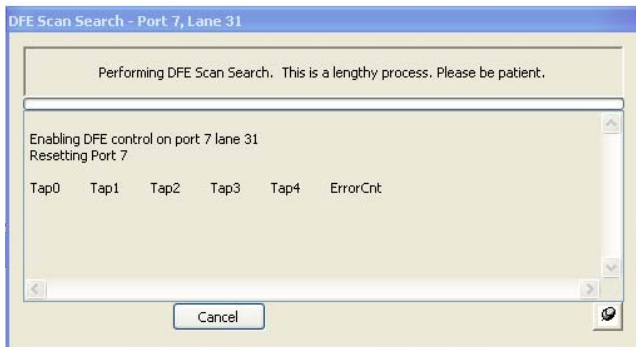
Figure 13: DFE Scan Algorithm Window



Pressing either “Go” choice opens a new window that looks like Figure 14. At this point the RapidFET JTAG (Enhanced) tool is completely under algorithm control and only the DFE Scan Search window is active. Other RapidFET JTAG (Enhanced) windows may grey over while the DFE Scan Search is active. The progress bar indicates the progress made in the scanning process. Once the scan is complete and new tap settings are available, pressing the Copy to Clipboard button will write the coefficients into the SerDes Configuration window for the respective lane. Closing the DFE Scan Search window returns control to the SerDes Configuration window to permit selection of another lane.

In this example, the two ports connected together are on the same device and therefore visible to the same instance of the RapidFET JTAG (Enhanced) tool. If the linked ports are on different devices, the tool will have to be connected to each device separately for transmitter coefficient changes and then the connections repeated to scan for receiver DFE coefficients.

Figure 14: DFE Scan Search Running Window



Signal Quality Optimization for Multi-Lane Ports

The procedure for optimizing the signal quality of multi-lane ports must account for the operation of the link-initialization state machines. The easiest method is to set the transmit strength to 0 for the transmitter on the near link and the link partner for all lanes. This has the effect of halting operation of the link-initialization state machines since no lane can train.

Signal quality can then be optimized for one lane at a time by optimizing the transmit coefficients for one lane in one direction, and then optimizing the DFE coefficients for that same lane in the same direction. Once a lane and direction have been optimized, the transmitter strength should be set back to zero.

The lane sequence that has been found to be the most effective is to work from lane D to lane A, sequentially setting the desired lane's transmitter amplitude to the correct setting while clearing all others to zero.

Once all lanes have been optimized in each direction as described above, the transmit and DFE coefficients can be programmed to enable correct operation for the RapidIO port.

All of the Coefficients have been Determined – Now What?

Once all of the coefficients have been determined by the tool to yield a BER of at least 10^{-12} , it is then necessary to perform a BER soak which should run overnight. Referring back to [Figure 11](#), Port/Lane Mapping and Control, refresh the window to ensure that the port status is green. If it is red, disable and re-enable the port using the "Port Enable" selection for the port in order to reset the port and all of its internal state machines.

Then proceed to the SerDes Configuration window, see [Figure 12](#), and enable error counting. If the scanning process has been successful, the error count should remain very low, less than one error per hour at 3.125Gbps for an error rate of better than 10^{-12} .

A bit error rate higher than 10^{-12} does not meet the minimum requirements for RapidIO and it would be prudent to repeat the coefficient search once again. It is possible that the channel characteristics are sufficiently poor that the degradation of the signal is beyond the capability of the SerDes. A simulation review of the channel using the IBIS-AMI model available for the SerDes can be used to determine if the topology and implementation of the channel is within or beyond the capability of the SerDes.

If a long term soak of the system indicates a BER that approaches the target of 10^{-15} , the performance approaches that desired for data rates of 5.0 and 6.25Gbps. System deployment can then be considered with the knowledge that the link is stable and sufficiently error free to support a high throughput bandwidth.

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