SRDP2 User Manual

Formal Status

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About this Document

Topics discussed include the following:

Overview

This document discusses the architecture, specifications, and functional characteristics of the *Serial RapidIO Development Platform Gen2 (SRDP2) User Manual*. The platform's main purpose is to provide a design reference for board designers who are implementing the SRDP2 schematic design. It can also be used to evaluate the key features of the SRDP2.

Revision History

June 12, 2012

- Added a new chapter, Recommended Cables
- Updated the Ordering Information

March 31, 2011

Updated Table 5 and the preceding paragraph.

February 15, 2011

Updated to support changes to SRDP2 Assembly Revision 3.

- Changed the default setting for J55 - I2C Master or Slave Mode (CPS-1848) to OUT
- Changed the default setting for J87 - I2C Master or Slave Mode (SPS-1616) to OUT

September 16, 2010

- Updated SRDP2 Block diagram with Connector Reference Designators
- Updated Default Configuration to reflect current board assembly.

August 12, 2010

Updated the Ordering Information and fixed the connector information for J45 - J62 - J66 - J67 InfiniBand Connectors.

June 18, 2010

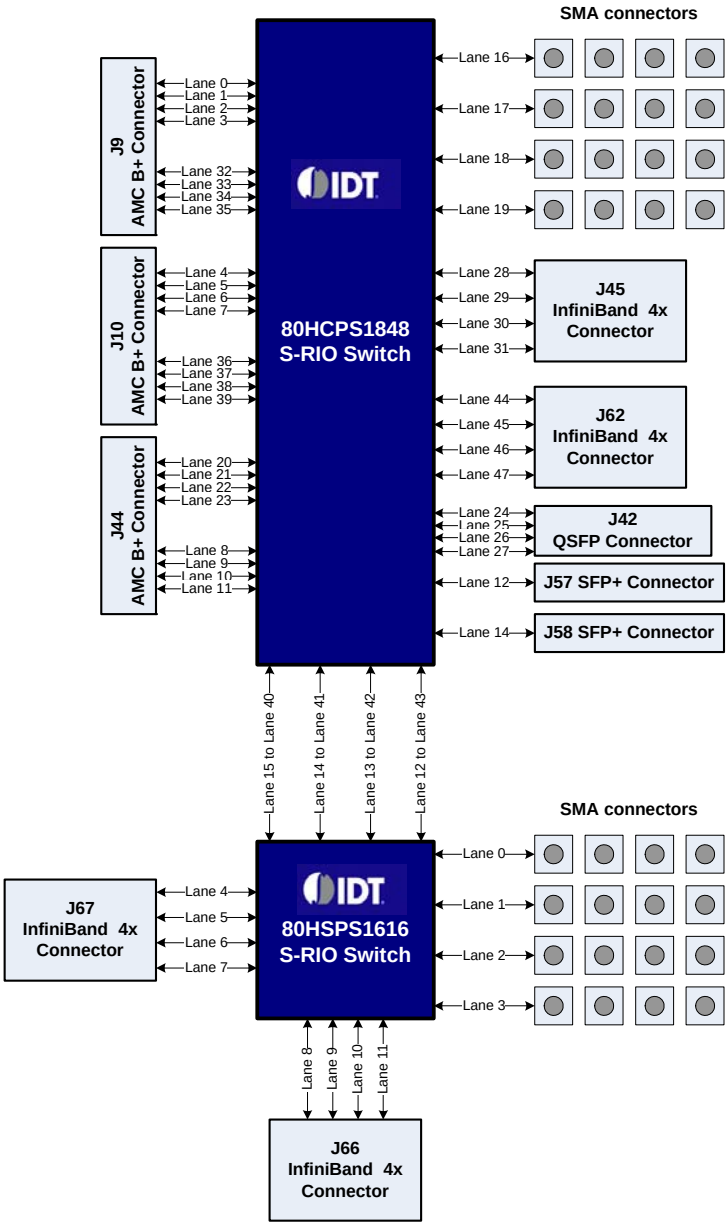
First release of the *Serial RapidIO Development Platform Gen2 User Manual*.

1. Overview

1.1 Introduction

The Serial RapidIO Development Platform Gen2 (SRDP2) provides a flexible test platform for S-RIO Gen2 switches. It is a stand-alone desktop platform powered by an ATX power supply. The SRDP2 is composed of two S-RIO Gen2 switches: the CPS-1848 (80HCPS1848) and the SPS-1616 (80HSPS1616), and several standard connectors. Figure 1 shows a block diagram of the SRDP2.

Figure 1: SRDP2 Block Diagram



1.2 Key Features

- S-RIO Switching Fabric
  - Device: IDT CPS-1848 and SPS-1616 S-RIO Gen2 switches
  - Link speed: 6.25, 5, 3.125, 2.5, 1.25 Gbaud
  - Protocol: S-RIO Gen1 (v1.3) or S-RIO Gen2 (v2.1)
  - LA probe: ½ Mid-bus footprint for all 58 S-RIO lanes
- Industry-standard system interconnect connectors
  - 3 AMC B+ connectors: 4x S-RIO link, Ports 4–7 and 8–11 (NO support on IPMC and JTAG)
  - 2 SFP+ connectors: 1x S-RIO link
  - 1 QSFP connector: 4x S-RIO link
  - 4 InfiniBand/CX4 connectors: 4x S-RIO link
  - SMA arrays
- Clock distribution
  - PLL synthesizer: IDT ICS841N254i, four outputs
  - Clock frequency: 156.25 MHz, differential HCSL
  - Reference Clock Out: SMA, differential LVDS, 156 MHz
  - Reference Clock In: SMA, LVTTL, 25 MHz
- JTAG and I2C
  - JTAG header: 0.1" 10-pin header, two S-RIO switches and JTAG header form a JTAG chain
  - I2C header: 0.1” 10-pin header, for both S-RIO switch I2C access
  - One I2C EEPROM per switch
  - USB connector: on-board JTAG/I2C to USB converter (FTDI FT2232HL)
- Power distribution
  - External power supply: ATX power supply with on-board, push-button ON/OFF control
  - Adjustable DC/DC regulators

2. Design Description

This chapter describes the design characteristics of the SRDP2. It is intended to provide an understanding of how the components are connected together and how they interact.

2.1 Switch Ports Assignment

The switch lanes to connector assignment is detailed in Table 1 and Table 2. The CPS-1848 and SPS-1616 are connected together using four lanes.

Table 1: Lane Assignment (CPS-1848)

CPS-1848 Lane	Connector	Assignment
0	AMC J9	Port 4
1		Port 5
2		Port 6
3		Port 7
4	AMC J10	Port 4
5		Port 5
6		Port 6
7		Port 7
8	AMC J44	Port 8
9		Port 9
10		Port 10
11		Port 11
12	SFP J57	SFP Tx/Rx
13		Not Connected
14	SFP J58	SFP Tx/Rx
15		Not Connected
16	SMAs	Tx: J16/J26, Rx J25/J24
17		Tx: J12/J11, Rx J23/J22
18		Tx: J17/J15, Rx J21/J20
19		Tx: J14/J13, Rx J19/J18

Table 1: Lane Assignment (CPS-1848) *(Continued)*

CPS-1848 Lane	Connector	Assignment
20	AMC J44	Port 4
21		Port 5
22		Port 6
23		Port 7
24	QSFP J42	Lane 1
25		Lane 2
26		Lane 3
27		Lane 4
28	InfiniBand J45	Lane 1
29		Lane 2
30		Lane 3
31		Lane 4
32	AMC J9	Port 8
33		Port 9
34		Port 10
35		Port 11
36	AMC J10	Port 8
37		Port 9
38		Port 10
39		Port 11
40	-	Lane 15 of SPS1616
41		Lane 14 of SPS1616
42		Lane 13 of SPS1616
43		Lane 12 of SPS1616
44	InfiniBand J62	Lane 1
45		Lane 2
46		Lane 3
47		Lane 4

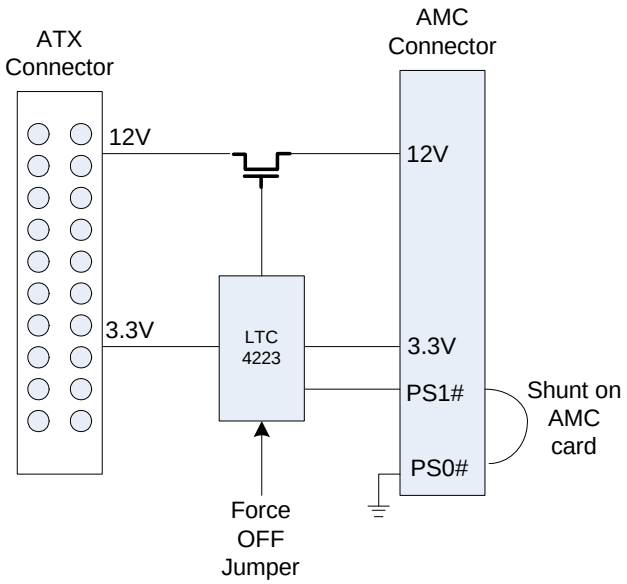
Table 2: Port Assignment (SPS-1616)

SPS-1616 Lane	Connector	Assignment
0	SMAs	Tx: J83/J82, Rx J75/J74
1		Tx: J81/J80, Rx J73/J72
2		Tx: J79/J78, Rx J71/J70
3		Tx: J77/J76, Rx J69/J68
4	InfiniBand J67	Lane 1
5		Lane 2
6		Lane 3
7		Lane 4
8	InfiniBand J66	Lane 1
9		Lane 2
10		Lane 3
11		Lane 4
12	-	Lane 43 of CPS-1848
13		Lane 42 of CPS-1848
14		Lane 41 of CPS-1848
15		Lane 40 of CPS-1848

2.2 AMC Connector Power Distribution

The AMC connector provides 12V and 3.3V power to the plug-in AMC modules. The 12V supply is gated with a high current Field Effect Transistor (FET). When inserted, the AMC module shunts the presence signals (PS1# connects to PS0#). When this connection is established, a hot swap controller turns the FET ON in a controlled fashion. In-rush current is limited and high current faults are detected. The hot swap controller can be used to manually keep AMC power OFF. A jumper is provided to force a power-down condition.

Figure 2: AMC Power Controller



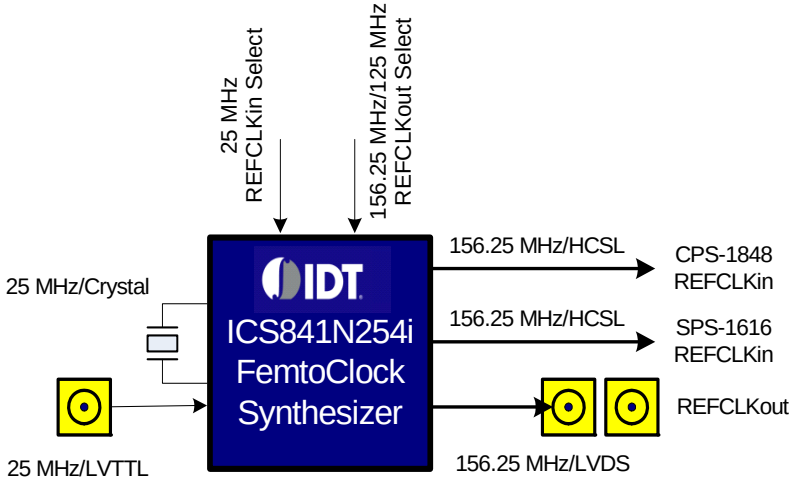
2.2.1 AMC Module Current Limit

The hot swap controller provides short circuit protection. The current limit is programmed with a sense resistor in series in the 12V supply. The current limit is set to 6.25A per connector. The 3.3V supply should be used for management power only on the module and is limited to 165 mA.

2.3 Clocking

The FemtoClock synthesizer, ICS841N254i, is designed for S-RIO 1.3 and 2.1 applications. The synthesizer's sourcing clock can be supplied from either the on-board 25-MHz crystal, or from an external 25-MHz LVTTL reference clock. The synthesizer generates 156.25-MHz or 125-MHz reference clock outputs. There are four clock outputs, two of which are HCSL and two LVDS. The HCSL output is used to drive the CPS-1848 and SPS-1616 reference clock inputs through AC coupling, and LVDS reference clock output are available on SMA connectors. The ICS841N254i has excellent phase jitter performance at 0.5 ps RMS specified for the 1–20 MHz frequency range, in compliance with S-RIO Gen2 switch reference clock requirement.

Figure 3: Clock Generation and Distribution Chip



2.4 Reset

Board-level reset is activated two different ways: power-up and manual reset. These options are discussed below.

2.4.1 Power-up Reset

On power-up, the CPS-1848 and SPS-1616 are held in reset by voltage supervisors/reset timers.

There are three open-drain voltage supervisor “OR wired” together, each monitoring a specific voltage supply. When all three supplies are within good operating range, a reset delay timer counter is started. After the delay, reset is de-asserted.

Since the power supply of the two switches are separate, each S-RIO switch has its own voltage supervisor circuit as described above.

2.4.2 Manual Reset

The voltage supervisors (TPS3808) provide a manual reset input for push-button resets (see Figure 4). The reset assertion time is the same as the power-up time. The reset push-button actives the CPS-1848 and SPS-1616 reset circuit concurrently.

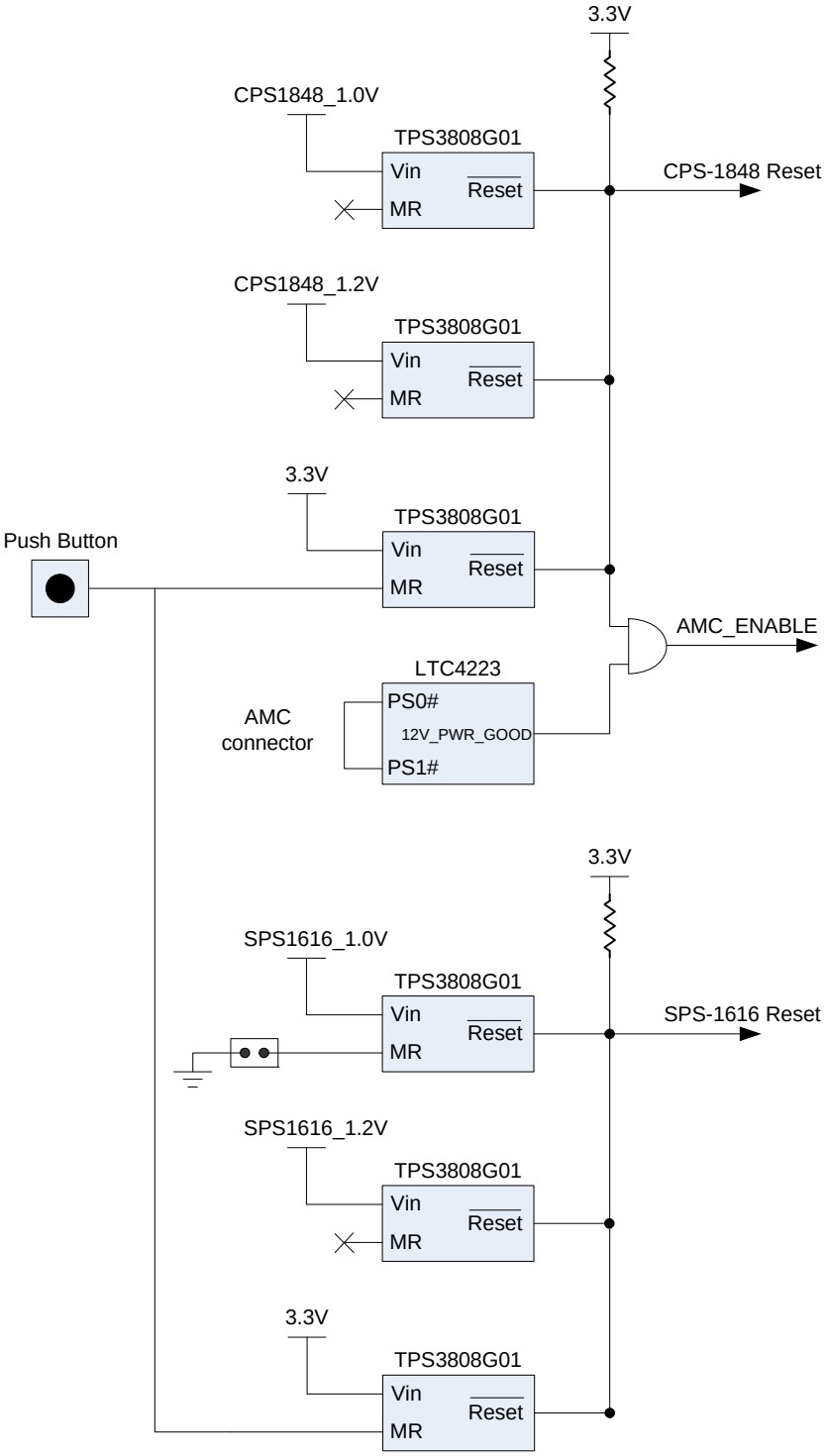
A jumper is provided to force the SPS-1616 device in reset.

2.4.3 Reset Status LED

Two board reset status LEDs indicate the reset signals are de-asserted: one for CPS-1848 and one for SPS-1616.

All three AMC connector’s AMC enable pin is also driven by the CPS-1848 reset. LEDs are provided to indicate the AMC is enabled.

Figure 4: Board Reset



2.5 Power

The SRDP2 is powered by the 12V and 3.3V rails from an ATX power supply. Current draw of the CEB is expected to be high because of the AMC module's current requirement. The CEB provides a 20-pin ATX power connector and an additional 12V ATX peripheral power connector. The auxiliary connector can be optionally used when two high-current AMC cards are plugged in.

The ATX power supply is turned On/Off by an on-board push button. The push button toggles a flip-flop which is used to drive the ON/OFF control of the ATX power supply. A jumper is provided to force the ATX supply ON. When the jumper is installed, the ATX supply is turned on regardless of the state of the flip-flop.

2.5.1 Voltage Regulators

The on-board voltage regulators are sized to supply the current requirement as listed in Table 3 and Table 4.

Table 3: SRDP2 Power Budget (except SPS-1616)

	3.3V	1.2V	1.0V
CPS-1848	0.027A	1.52A	6.62A
Clk buff	0.2A	-	-
2 x SFP pwr	0.6A	-	-
1 x QSFP pwr	0.3A	-	-
FTDI	0.22A	-	-
Total	1.35A	1.52A	6.62A

Table 4: SPS-1616 Power Budget

	3.3V	1.2V	1.0V
SPS-1616	0.026A	0.528A	3.98A

2.5.2 Power Distribution and Sequencing

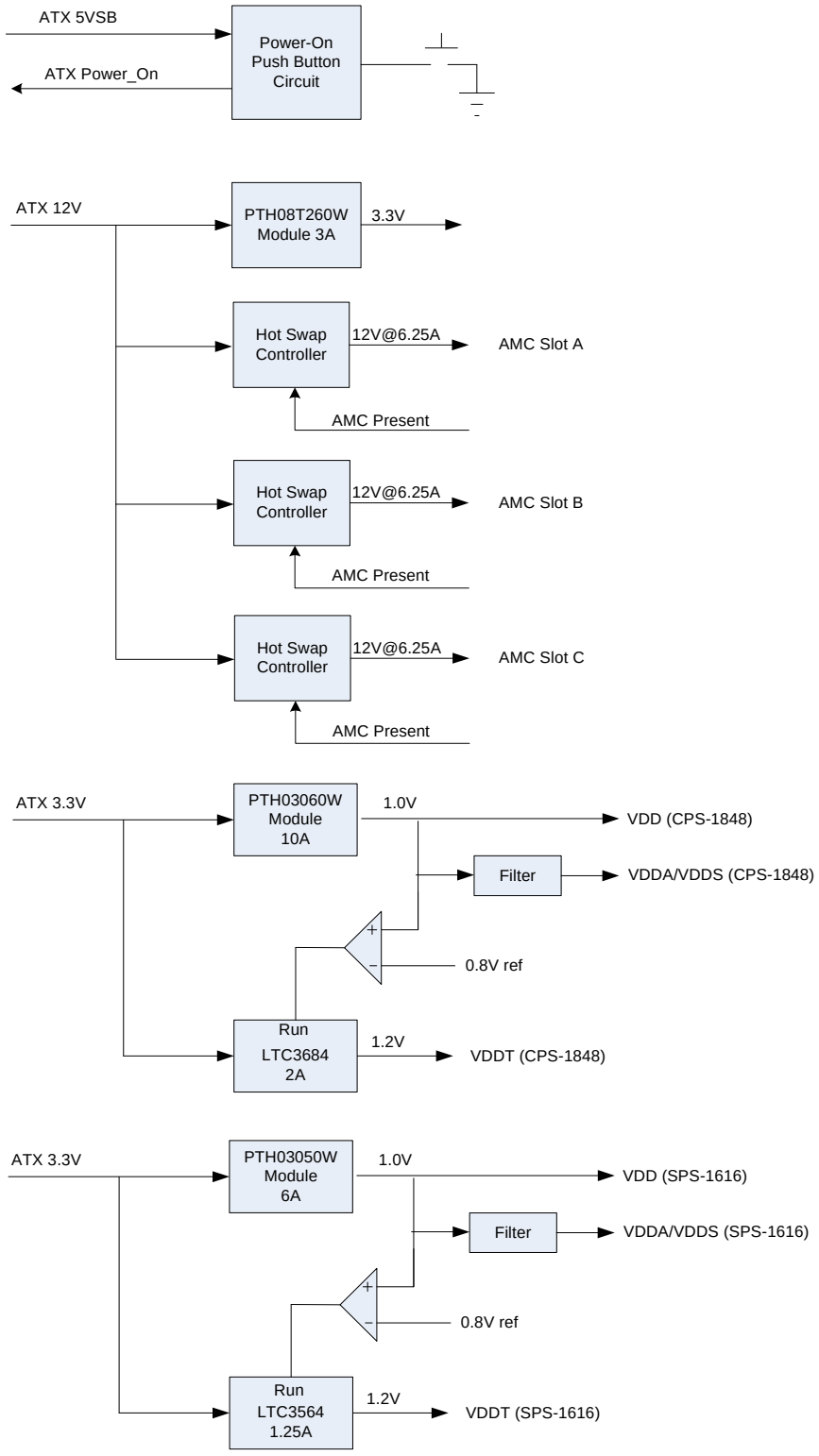
Figure 5 represents the voltage regulators and associated control circuits as implemented on the SRDP2. The CPS-1848 and SPS-1616 VDD (1.0V) rails are split on two separate regulators. This give us the advantage of keeping the current distribution on the power plane to less than 10 Amps. It also gives the option to do current measurement of each device individually.

The regulators' power up sequence is controlled such that the 1.2V regulator is enable after the 1.0V regulator is active. Since the ATX 12V and the ATX 3.3V ramp up somewhat concurrently, it is expected that the 3.3V regulator will also ramp up concurrently with the 1.0V regulator. LEDs are provided to indicate the status of the rails.

2.5.3 Current Measurement

Large banks of 0 Ohm regulators can be removed from the SRDP2 to isolate the regulators from the power planes. This would allow a series connection on a current meter is current measurement needed to be performed. For component locations, see the SRDP2 schematic.

Figure 5: Power Distribution

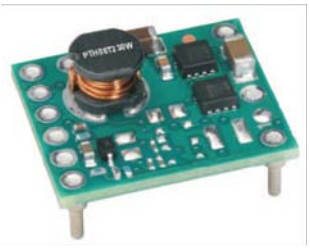


2.5.3.1 3.3V Regulator

The 3.3V rail for on-board components is supplied with a regulator. Using the 3.3V supply from the ATX supply would have been too noisy and not accurate enough for the clock buffer and the switches.

The PTH08T260 power module from Texas Instruments is supplied from the ATX 12V. It provides a 3.3V output with an accuracy of +/- 1.5%. The module provides 3A and is 95% efficient.

Figure 6: PTH08T260 Module



2.5.3.2 1.2V Regulators

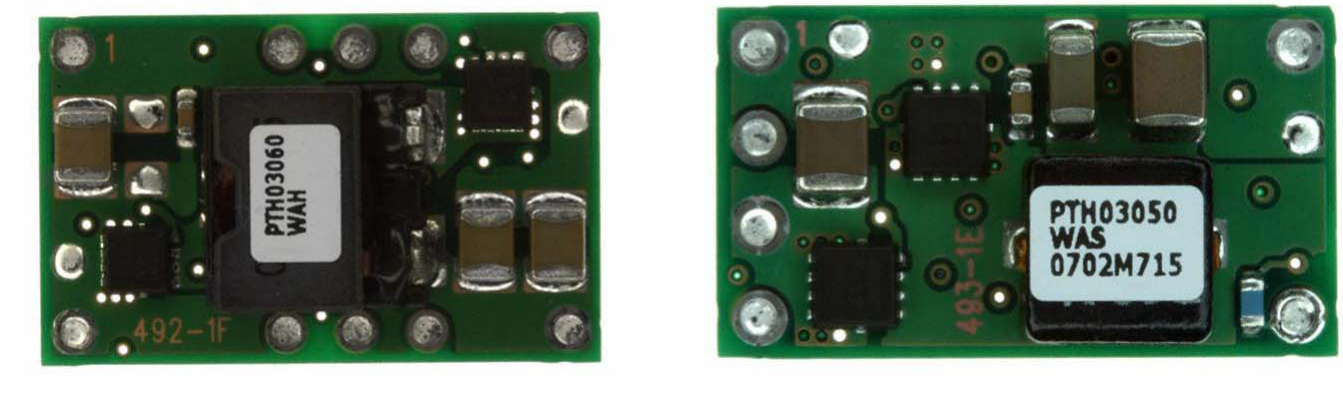
The LTC3564 device from Linear Tech is a switching monolithic regulator. It is composed of the controller chip and an external inductor, plus some capacitors. The output voltage is adjusted to 1.2V with the R1, R2 resistors displayed in the following diagram. The maximum output current is 1.25A.

Figure 7: LT3685 and LTC3564 Regulators

2.5.3.3 1.0V Regulator

The 1.0V regulators used for the switch's core supply are the TI PTH03060W and PTH03050W modules. They provide a maximum of 10A / 6A each, and are accurate to +/- 2% when 1% resistors are used to set the output voltage.

Figure 8: PTH03060W Module



2.6 JTAG

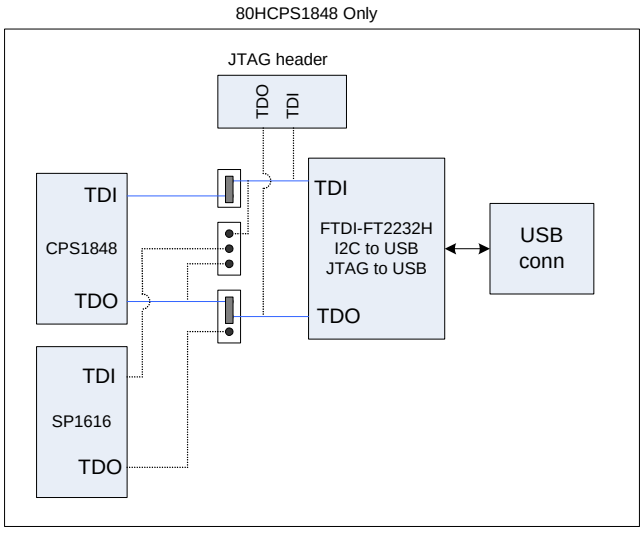
An on-board USB to JTAG bridge is provided. This feature allows users to access the JTAG chain without the need for a JTAG dongle. Only a single USB cable is required to connect the host PC to the SRDP2.

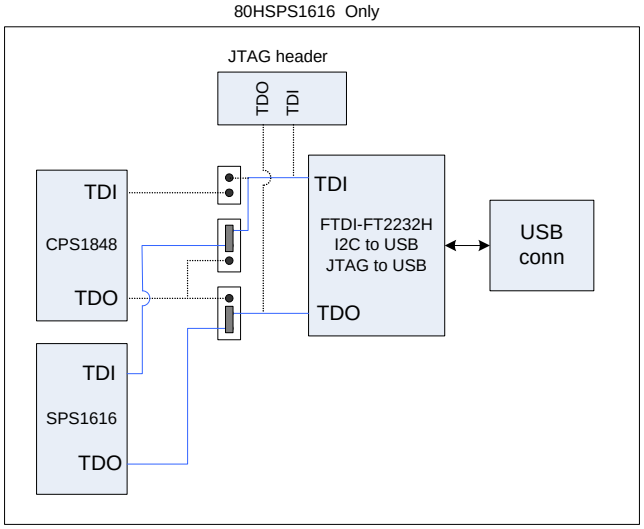
The USB to JTAG bridging is made by a FTDI-FT2232H device. The USB application drivers over Windows and Linux are provided for free from www.ftdchip.com.

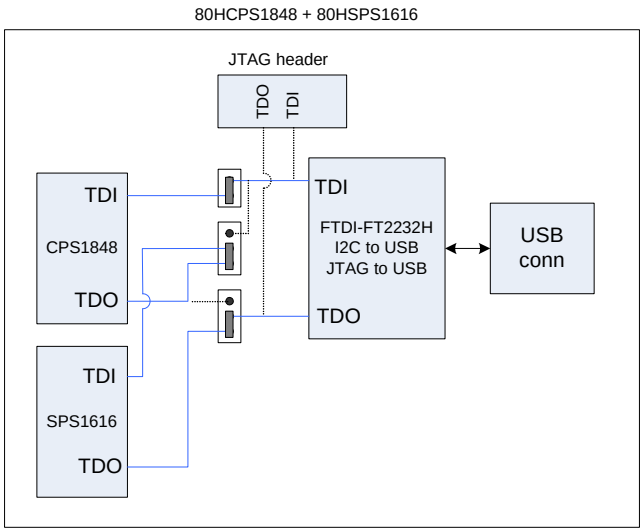
The two switches' JTAG ports are chained together and connected to the FTDI chip. A connector is also provided in case users need to drive the JTAG chain with another type of device. The connector is in parallel with the FTDI chip. Contention between the FTDI chip and the dongle is avoided by disconnecting the USB cable. This effectively cuts power to the FTDI chip.

There are three sets of jumpers that configure the JTAG chain. They configure to chain CPS-1848 only, SPS-1616 only, or both switches. Figure 9 shows all three options.

Figure 9: JTAG USB Driver







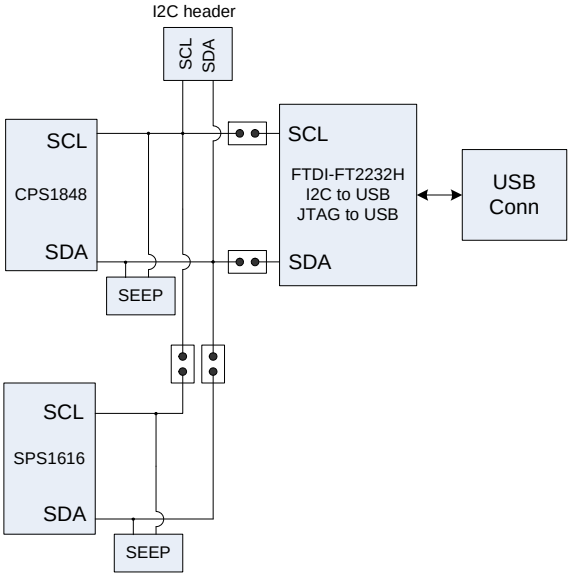
2.7 I2C

The FTDI chip has two multi-purpose ports. One is used for JTAG as described above, and the other one is used for the I2C port.

The I2C port of each switch is connected to a serial EEPROM and a header. The two I2C ports (from each switch) are not directly connected together because there would otherwise be contention on power up when the two switches would try to master the bus to read the serial EEPROMs. There is a pair of jumpers used to disconnect the two switches.

The FDTI USB-I2C link is optionally attached to the switches' I2C port with suitcase jumpers.

Figure 10: I2C Block Diagram



The serial EEPROMS installed on the SRDP2 are AT24C64s. They use 7-bit addressing and the 3 lower bits of their address are hardwired on the SRDP2. The CPS-1848 and SPS-1616 devices are also configured for 7-bit addressing with a default address as shown in Table 5. These devices can be programmed on-board through the I2C header or USB cable.

Table 5 shows the I2C address of each slave device on the bus.

Table 5: I2C Address Map

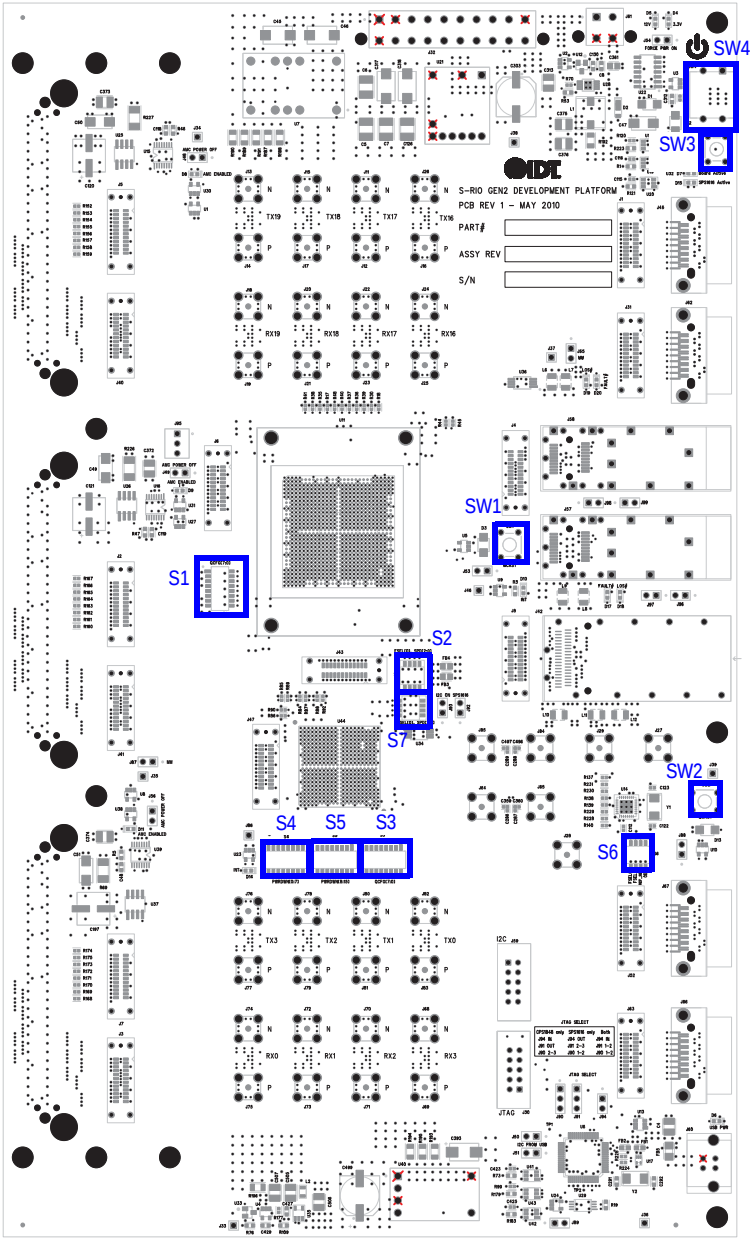
Device	I2C address
CPS-1848	b1100000
EEPROM for CPS1848	b1010000
SPS-1616	b1100001
EEPROM for SPS1616	b1010001

3. Controls and Configurations

This chapter describes the configuration options on the SRDP2.

3.1 Switches

Figure 11: Switch Location



3.1.1 S1 - Quadrant Configuration (CPS-1848)

The CPS-1848 Quadrant Configuration (QCFG) pins are set with DIP switches located on DIP switch S1.

Table 6: S1 Setting

Switch Number	Signal	Default Setting	Set up value	Description
1	QCFG0	ON	ON = 0 OFF = 1	Quadrant 0 port width: QCFG[1:0] • 0:0 Lanes[0–3] in 4x Lanes[16–19] in 4x Lanes[32–35] in 4x • 0:1 Lanes[0–1] in 2x Lanes[2–3] in 2x Lanes[16–19] in 4x Lanes[32–35] in 4x • 1:0 Lanes[0–1] in 2x Lanes[2–3] in 2x Lanes[16–19] in 4x Lanes[32–33] in 2x Lanes[34–35] in 2x • 1:1 Lanes[0–1] in 2x Lane[2] in 1x Lane[3] in 1x Lanes[16–19] in 4x Lanes[32–35] in 4x
2	QCFG1	ON		

Table 6: S1 Setting *(Continued)*

Switch Number	Signal	Default Setting	Set up value	Description
3	QCFG2	ON	ON = 0 OFF = 1	Quadrant 1 port width: QCFG[3:2] • 0:0 Lanes[4–7] in 4x Lanes[20–23] in 4x Lanes[36–39] in 4x • 0:1 Lanes[4–5] in 2x Lanes[6–7] in 2x Lanes[20–23] in 4x Lanes[36–39] in 4x • 1:0 Lanes[4–5] in 2x Lanes[6–7] in 2x Lanes[20–23] in 4x Lanes[36–37] in 2x Lanes[38–39] in 2x • 1:1 Lanes[4–5] in 2x Lane[6] in 1x Lane[7] in 1x Lanes[20–23] in 4x Lanes[36–39] in 4x
4	QCFG3	ON		

Table 6: S1 Setting *(Continued)*

Switch Number	Signal	Default Setting	Set up value	Description
5	QCFG4	ON	ON = 0 OFF = 1	Quadrant 2 port width: QCFG[5:4]] • 0:0 Lanes[8–11] in 4x Lanes[24–27] in 4x Lanes[40–43] in 4x • 0:1 Lanes[8–9] in 2x Lanes[10–11] in 2x Lanes[24–27] in 4x Lanes[40–43] in 4x • 1:0 Undefined • 1:1 Undefined
6	QCFG5	ON		
7	QCFG6	OFF	ON = 0 OFF = 1	Quadrant 3 port width: QCFG[7:6] • 0:0 Lanes[12–15] in 4x Lanes[28–31] in 4x Lanes[44–47] in 4x • 0:1 Lanes[12–13] in 2x Lanes[14–15] in 2x Lanes[28–31] in 4x Lanes[44–47] in 4x • 1:0 Undefined • 1:1 Undefined
8	QCFG7	ON		

3.1.2 S2 - Speed Select, Frequency Select (CPS-1848)

Table 7: S2 Setting

Switch Number	Signal	Default Setting	Set up value	Description
1	Switch B FSEL0	OFF	ON = 0 OFF = 1	FSEL0 = 0 Core Clock Frequency = 156.25 MHz FSEL0 = 1 Core Clock Frequency = 312.5 MHz
2	Switch B SPD2	OFF	ON = 0 OFF = 1	S-RIO port speed at RESET for all ports SPD[2:0] 000 = 1.25 Gbaud 001 = 2.5 Gbaud 01X = 5.0 Gbaud 100 = Reserved 101 = 3.125 Gbaud 11X = 6.25 Gbaud
3	Switch B SPD1	ON		
4	Switch B SPD0	OFF		

3.1.3 S3 - Quadrant Configuration (SPS-1616)

SPS-1616 Configuration (QCFG) pins are set with DIP switches located on DIP switch S3.

Table 8: S3 Setting

Switch Number	Signal	Default Setting	Set up value	Description
1	QCFG0	OFF	ON = 0 OFF = 1	Quadrant 0 port width: QCFG[1:0] 0:0 = Lane 0–3 in 4x 0:1 = Lane 0–1 in 2x, lane 2–3 in 2x 1:0 = Lane 0–1 in 2x lane 2 in 1x, lane 3 in 1x 1:1 = Lane 0 to 3 in 1x
2	QCFG1	OFF		
3	QCFG2	ON		Quadrant 1 port width: QCFG[3:2] 0:0 = Lane 4–7 in 4x 0:1 = Lane 4–5 in 2x, lane 6–7 in 2x 1:0 = Lane 4–5 in 2x lane 6 in 1x, lane 7 in 1x 1:1 = Lane 4 to 7 in 1x
4	QCFG3	ON		
5	QCFG4	ON		Quadrant 2 port width: QCFG[5:4] 0:0 = Lane 8–11 in 4x 0:1 = Lane 8–9 in 2x, lane 10–11 in 2x 1:0 = Lane 8–9 in 2x lane 10 in 1x, lane 11 in 1x 1:1 = Lane 8 to 11 in 1x
6	QCFG5	ON		
7	QCFG6	ON		Quadrant 0 port width: QCFG[7:6] 0:0 = Lane 12–15 in 4x 0:1 = Lane 12–13 in 2x, lane 14–15 in 2x 1:0 = Lane 12–13 in 2x lane 14 in 1x, lane 15 in 1x 1:1 = Lane 12 to 15 in 1x
8	QCFG7	ON		

3.1.4 S4 - Port Disable Pins 0–7 (SPS-1616)

S4 is used to set the Port disable pins.

Table 9: S4 Setting

Switch Number	Signal	Default Setting	Set up value	Description
1	PD7	OFF	ON = 0 OFF = 1	0 = Disabled 1 = Lane 7 Enabled
2	PD6	OFF		0 = Disabled 1 = Lane 6 Enabled
3	PD5	OFF		0 = Disabled 1 = Lane 5 Enabled
4	PD4	OFF		0 = Disabled 1 = Lane 4 Enabled
5	PD3	OFF		0 = Disabled 1 = Lane 3 Enabled
6	PD2	OFF		0 = Disabled 1 = Lane 2 Enabled
7	PD1	OFF		0 = Disabled 1 = Lane 1 Enabled
8	PD0	OFF		0 = Disabled 1 = Lane 0 Enabled

3.1.5 S5 - Port Disable Pins 8–15 (SPS-1616)

S5 is used to set the Port disable pins.

Table 10: S5 Setting

Switch Number	Signal	Default Setting	Set up value	Description
1	PD15	OFF	ON = 0 OFF = 1	0 = Disabled 1 = Lane 15 Enabled
2	PD14	OFF		0 = Disabled 1 = Lane 14 Enabled
3	PD13	OFF		0 = Disabled 1 = Lane 13 Enabled
4	PD12	OFF		0 = Disabled 1 = Lane 12 Enabled
5	PD11	OFF		0 = Disabled 1 = Lane 11 Enabled
6	PD10	OFF		0 = Disabled 1 = Lane 10 Enabled
7	PD9	OFF		0 = Disabled 1 = Lane 9 Enabled
8	PD8	OFF		0 = Disabled 1 = Lane 8 Enabled

3.1.6 S6 - Clock Synthesizer Control

S6 is tied to the ICS841N254I clock Synthesizer.

Table 11: S6 Setting

Switch Number	Signal	Default Setting	Set up value	Description
1	FSEL0	OFF	ON = 1 OFF = 0	FSEL[1:0] = Output Frequency 0:0 = 156.25 MHz 0:1 = 125 MHz 1:0 = 100 MHz 1:1 = 250 MHz
2	FSEL1	OFF		
3	REF_SEL	OFF		0 = Reference Clock from Crystal 1 = Reference Clock from J28
4	OEA_N	OFF		0 = QA[0:1] outputs (to J27/J29) is enabled 1 = QA[0:1] outputs (to J27/J29) is disabled

3.1.7 S7 - Speed Select, Frequency Select (SPS-1616)

Table 12: S7 Setting

Switch Number	Signal	Default Setting	Set up value	Description
1	FSEL0	OFF	ON = 0 OFF = 1	FSEL0 = 0 Core Clock Frequency = 156.25 MHz FSEL0 = 1 Core Clock Frequency = 312.5 MHz
2	SPD2	OFF	ON = 0 OFF = 1	S-RIO port speed at RESET for all ports SPD[2:0] 000 = 1.25 Gbaud 001 = 2.5 Gbaud 01X = 5.0 Gbaud 100 = Reserved 101 = 3.125 Gbaud 11X = 6.25 Gbaud
3	SPD1	ON		
4	SPD0	OFF		

3.1.8 SW1 - Multicast Push Button (CPS-1848)

SW1 is a push button tied to MCAST of the CPS-1848. When SW1 is pushed, a debounced rising edge is provided to the MCAST pin.

3.1.9 SW2 - Multicast Push Button (SPS-1616)

SW2 is a push button tied to MCAST of the SPS-1616. When SW2 is pushed, a debounced rising edge is provided to the MCAST pin.

3.1.10 SW3 - Board Reset

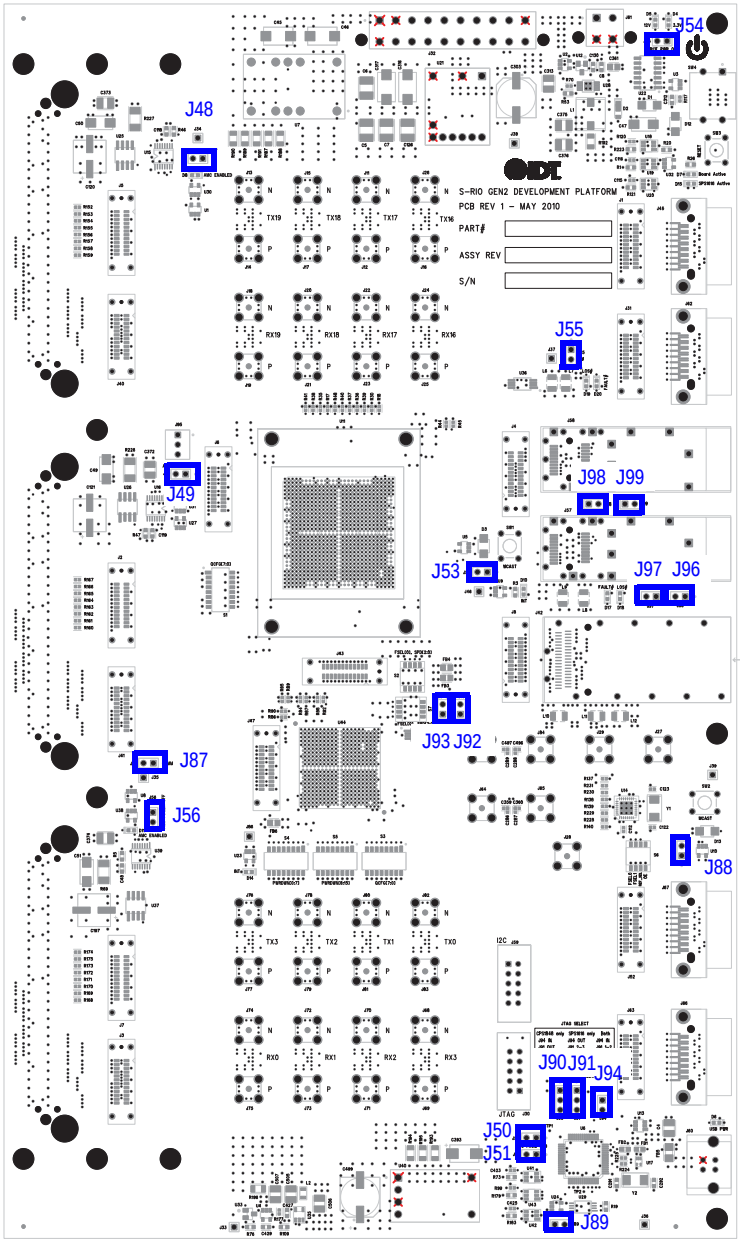
When SW3 is pushed, a debounced board reset is activated.

3.1.11 SW4 - Board Power

SW4 is a tactile push-button switch. Push once to enable the ATX power supply. Push again to disable power.

3.2 Jumpers

Figure 12: Jumper Locations



3.2.1 J48 - AMC1 Power OFF

Use J48 to force a power off condition to AMC1.

Table 13: J48 - AMC Power OFF

Shunt Jumper Location	Description	Default Setting
IN	AMC1 Power OFF	OUT
OUT	AMC1 Power under hot swap control	

3.2.2 J49 - AMC2 Power OFF

Use J49 to force a power off condition to AMC2.

Table 14: J49 - AMC Power OFF

Shunt Jumper Location	Description	Default Setting
IN	AMC2 Power OFF	OUT
OUT	AMC2 Power under hot swap control	

3.2.3 J50, J51 - I2C Chain On USB Controller

J50 and J51 connect the SRDP2's I2C SDA and SCL to the USB Controller. These jumpers should be installed when the I2C chain is controlled by a PC host via USB. They should be removed when the I2C chain is controlled by a dongle (in J59).

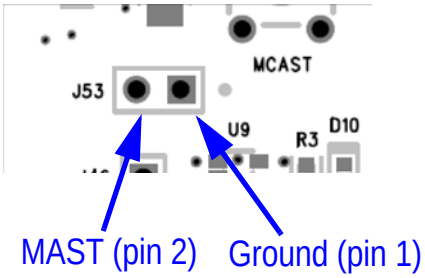
Table 15: J50, J51 - I2C Chain on USB controller

Shunt Jumper Location	Description	Default Setting
IN	I2C driven by USB controller	IN
OUT	I2C disconnected from USB controller	

3.2.4 J53 - Multicast External Input (CPS-1848)

J53 connects external equipment to the MCAST pin of the CPS-1848. The input voltage on J53 should not exceed 3.3V.

Figure 13: J53 Pin Assignment



3.2.5 J54 - Force ATX Power ON

Use J54 for the AXT supply ON.

Table 16: J54 - Force ATX Power ON

Shunt Jumper Location	Description	Default Setting
IN	Force the ATX supply ON	OUT
OUT	Normal operation. ATX supply is turned ON/OFF by push button SW4.	

3.2.6 J55 - I2C Master or Slave Mode (CPS-1848)

Use J55 to select the I2C master or slave mode for the CPS-1848.

Table 17: J55 - I2C Mode Switch A

Shunt Jumper Location	Description	Default Setting
IN	Master Mode	OUT
OUT	Slave Mode	

3.2.7 J56 - AMC3 Power OFF

Use J56 to force a power off condition to AMC3.

Table 18: J56 - AMC Power OFF

Shunt Jumper Location	Description	Default Setting
IN	AMC3 Power OFF	OUT
OUT	AMC3 Power under hot swap control	

3.2.8 J87 - I2C Master or Slave Mode (SPS-1616)

Use J87 to select the I2C master or slave mode for the SPS-1616.

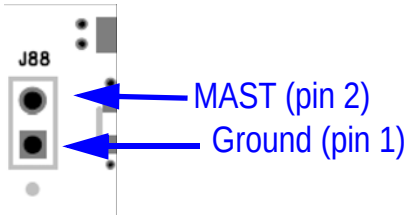
Table 19: J87 - I2C Mode Switch B

Shunt Jumper Location	Description	Default Setting
IN	Master Mode	OUT
OUT	Slave Mode	

3.2.9 J88 - Multicast External Input (SPS-1616)

J88 connects external equipment to the MCAST pin of the SPS-1616. The input voltage on J88 should not exceed 3.3V.

Figure 14: J63 Pin Assignment



3.2.10 J89 - Force Reset (SPS-1616)

Insert J89 to keep the device in reset.

Table 20: J89 - Force Reset (SPS-1616)

Shunt Jumper Location	Description	Default Setting
IN	SPS-1616 in Reset	OUT
OUT	Normal operation	

3.2.11 J90, J91, J94 - JTAG Select

Use these jumpers to select which device is part of the JTAG chain.

Figure 15: JTAG Select Jumpers

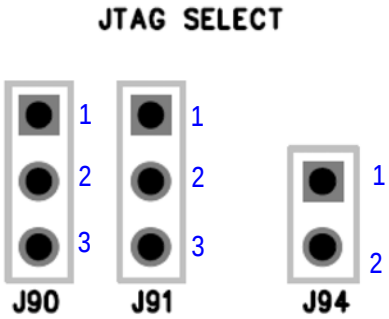


Table 21: JTAG Jumper Settings

Jumper	CPS-1848 Only	SPS-1616 Only	Both Devices
J94	IN	OUT	IN
J91	OUT	2 - 3	1 - 2
J90	2 - 3	1 - 2	1 - 2

3.2.12 J92, J93 - I2C Chain Disconnect (SPS-1616)

J92 and J93 connect the SRDP2's I2C SDA and SCL to the SPS-1616. They are removed to avoid contention when both switches are bus masters and both try to master the bus at the same time. The serial EEPROM for the SPS-1616 is still connected to the device's I2C port when the jumpers are removed.

Table 22: J92, J93 - I2C Chain Disconnect (SPS-1616)

Shunt Jumper Location	Description	Default Setting
IN	I2C chain connect to SPS-1616	OUT
OUT	I2C disconnected from SPS-1616	

3.2.13 J96, J97 - SFP (J57) Module Rate Select RS0, RS1

SFP module Rate Select pins (RS0 and RS1) are set with these two jumpers.

Table 23: J96, J97 - SFP (J57) RS0, RS1 Setting

Jumper	Shunt Jumper Location	Description	Default Setting
J97	IN	RS0 = 0	OUT
	OUT	RS0 = 1	
J96	IN	RS1 = 0	OUT
	OUT	RS1 = 1	

3.2.14 J98, J99 - SFP (J58) Module Rate Select RS0, RS1

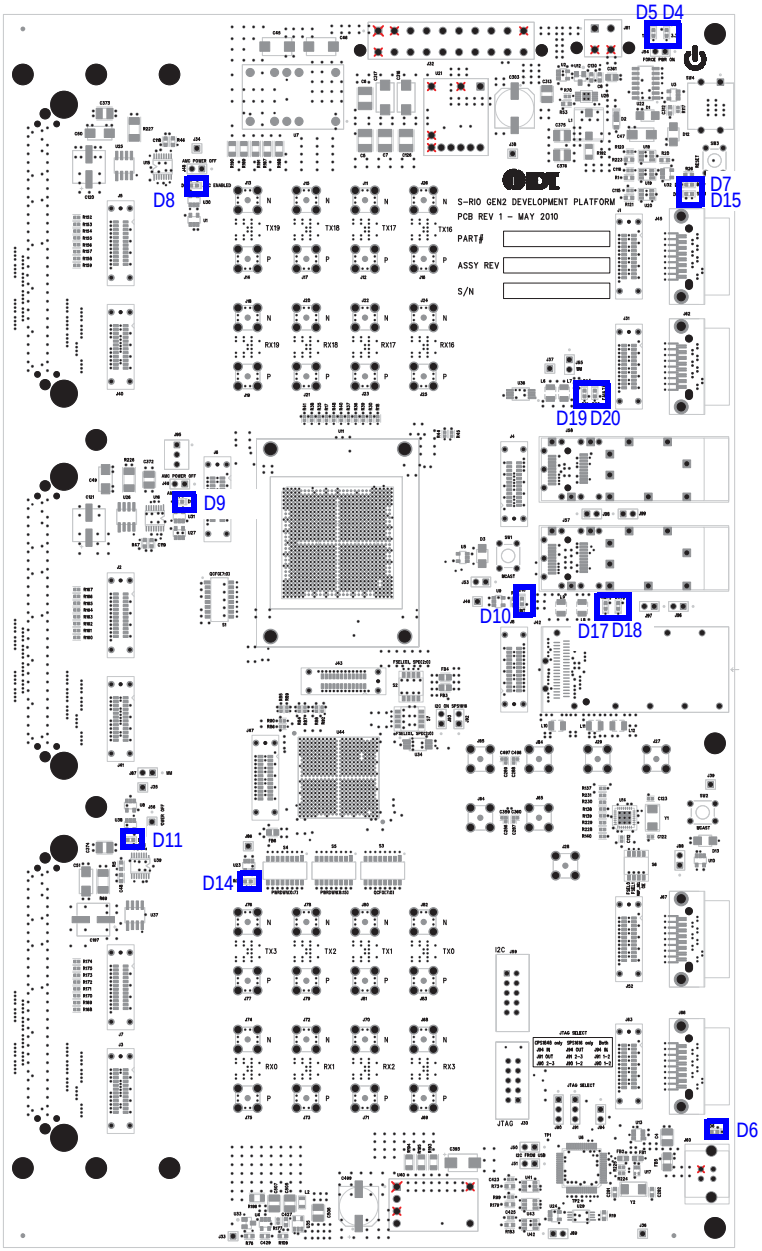
SFP module Rate Select pins (RS0 and RS1) are set with these two jumpers. J98, J99 - SFP (J58) RS0, RS1 setting.

Table 24: J98, J99 - SFP (J58) RS0, RS1 Setting

Jumper	Shunt Jumper Location	Description	Default Setting
J98	IN	RS0 = 0	OUT
	OUT	RS0 = 1	
J99	IN	RS1 = 0	OUT
	OUT	RS1 = 1	

3.3 Displays (LEDs)

Figure 16: LED Designation and Location



3.3.1 D4 - ATX 3.3V Power LED

D4 indicates the status of the ATX power supply 3.3V rail.

Table 25: D4 LED

Location	Color	Description
D4	Amber	ON = 3.3V Power is ON OFF = 3.3V Power is OFF

3.3.2 D5 - ATX 12V Power LED

D5 indicates the status of the ATX power supply 12V rail.

Table 26: D5 LED

Location	Color	Description
D5	Amber	ON = 3.3V Power is ON OFF = 3.3V Power is OFF

3.3.3 D6 - USB Power LED

D6 indicates the status of the power supplied by the host PC to the USB circuit. This LED must be on for the on-board USB to JTAG and USB to I2C controller to function properly.

Table 27: D6 LED

Location	Color	Description
D6	Green	ON = USB Power (from Host PC) is ON OFF = USB Power is not present

3.3.4 D7 - Board Reset Status LED

D7 indicates the status of the on-board reset circuit. Reset is controller by a push button and the on-board voltage supervisors.

Table 28: D7 LED

Location	Color	Description
D7	Blue	ON = SRDP2 is out of reset OFF = SRDP2 is in reset

3.3.5 D8 - AMC-1 Enable Status LED

D8 indicates the status of the AMC - 1 module power.

Table 29: D8 LED

Location	Color	Description
D8	Green	ON = 12V and 3.3V Power is ON OFF = Power is OFF

3.3.6 D9 - AMC- 2 Enable Status LED

D9 indicates the status of the AMC - 2 module power.

Table 30: D9 LED

Location	Color	Description
D9	Green	ON = 12V and 3.3V Power is ON OFF = Power is OFF

3.3.7 D10 - Interrupt Pending LED (CPS-1848)

D10 indicates the interrupt pin on CPS-1848 is low, indicating an interrupt pending.

Table 31: D10 LED (CPS-1848)

Location	Color	Description
D10	Orange	ON = Interrupt Pending OFF = No Interrupt

3.3.8 D11 - AMC- 3 Enable Status LED

D11 indicates the status of the AMC - 3 module power.

Table 32: D11 LED

Location	Color	Description
D11	Green	ON = 12V and 3.3V Power is ON OFF = Power is OFF

3.3.9 D14 - Interrupt Pending LED (SPS-1616)

D14 indicates the interrupt pin on SPS-1616is low, indicating an interrupt pending.

Table 33: D14 LED (SPS-1616)

Location	Color	Description
D14	Orange	ON = Interrupt Pending OFF = No Interrupt

3.3.10 D15 - Reset Status LED (SPS-1616)

D15 indicates the status of the on-board reset circuit for SPS-1616. Reset is controller by a push button and the on-board voltage supervisors.

Table 34: D15 LED (SPS-1616)

Location	Color	Description
D15	Blue	ON = SPS-1616 is out of reset OFF = SPS-1616 is in reset

3.3.11 D17, D18 - SFP Module (J57) Status LED

These two LEDs are tied to the LOS and FAULT status pins from the SFP.

Table 35: D17, D18 LEDs

Location	Color	Description
D18	Green	ON = RX_LOS is normal (no Loss of signal) OFF = RX_LOS is indicating loss of signal
D17	Green	ON = TX_FAULT is normal (no fault) OFF = TX_FAULT is indicating a fault

3.3.12 D19, D20 - SFP Module (J58) Status LED

These two LEDs are tied to the LOS and FAULT status pins from the SFP.

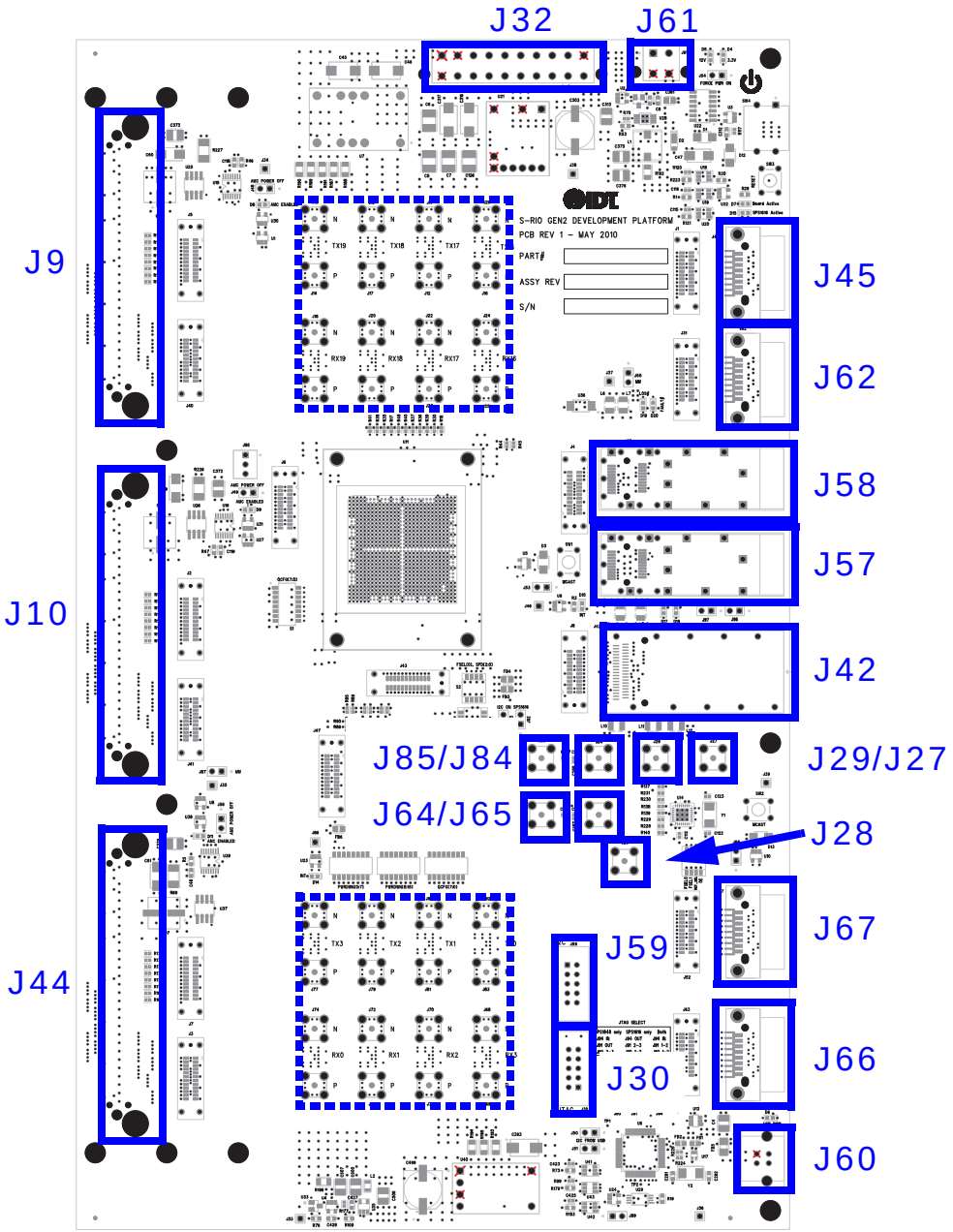
Table 36: D19, D20 LEDs

Location	Color	Description
D19	Green	ON = RX_LOS is normal (no Loss of signal) OFF = RX_LOS is indicating loss of signal
D20	Green	ON = TX_FAULT is normal (no fault) OFF = TX_FAULT is indicating a fault

4. Connectors

This chapter describes the connectors on the SRDP2.

4.1 Connector Locations

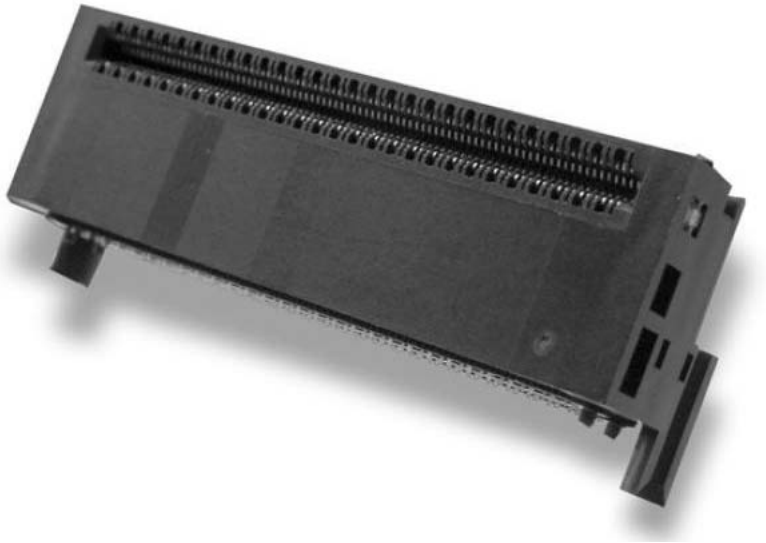


4.2 Connector Specification

This section describes the SRDP2's connectors and their pin assignments.

4.2.1 AMC Connectors

Figure 17: AMC Connector



The three AMC connectors are from Yamaichi: CN074-170-0005 [CONN AMC B+ MEZZ 170POS 0.75MM]. They are installed on the PCB using Compression Mount Technology. As such they are not soldered on the SRDP2. The electrical contact is established through the compression of each connector's contact on the PCB by screwing the component to the PCB. They are specified to support 12.5 Gbaud.

PICMG AMC.0 R2.0 specification defines the connectors' pin mapping - AMC carrier connector pin assignment for the B+ footprint. S-RIO lane mapping for AMC connectors is defined by AMC.4 Fabric Port Assignment on Basic and Extended Connectors.

4.2.1.1 AMC Connector Pinout

Table 37: J9, J10, J44 - AMC Connector Signal Assignment

Pin Number	AMC Signal	AMC1 (J9)	AMC2 (J10)	AMC3 (J44)	Description
B2	MB_PWR	12V rail			Payload Power
B3	MB_PS1#	Pull up to 3.3V ATX			Presence 1
B4	MB_MP	Hot Swap Controller 3.3V (150mA)			Management Power
B5	MB_GA0	GND			Geographic Addr. 0
B6	MB_RSRVD6	NC			Reserved, not connected
B8	MB_RSRVD8	NC			Reserved, not connected
B9	MB_PWR	12V rail			Payload Power
B11	MB_Rx0+	NC			Port 0 Receiver +
B12	MB_Rx0-	NC			Port 0 Receiver -
B14	MB_Tx0+	NC			Port 0 Transmitter +
B15	MB_Tx0-	NC			Port 0 Transmitter -
B17	MB_GA1	GND			Geographic Addr. 1
B18	MB_PWR	12V rail			Payload Power
B20	MB_Rx1+	NC			Port 1 Receiver +
B21	MB_Rx1-	NC			Port 1 Receiver -
B23	MB_Tx1+	NC			Port 1 Transmitter +
B24	MB_Tx1-	NC			Port 1 Transmitter -
B26	MB_GA2	GND			Geographic Addr. 2
B27	MB_PWR	12V rail			Payload Power
B29	MB_Rx2+	NC			Port 2 Receiver +
B30	MB_Rx2-	NC			Port 2 Receiver -
B32	MB_Tx2+	NC			Port 2 Transmitter +
B33	MB_Tx2-	NC			Port 2 Transmitter -
B35	MB_Rx3+	NC			Port 3 Receiver +
B36	MB_Rx3-	NC			Port 3 Receiver -
B38	MB_Tx3+	NC			Port 3 Transmitter +
B39	MB_Tx3-	NC			Port 3 Transmitter -

Table 37: J9, J10, J44 - AMC Connector Signal Assignment *(Continued)*

Pin Number	AMC Signal	AMC1 (J9)	AMC2 (J10)	AMC3 (J44)	Description
B41	MB_ENABLE#	Hot Swap Controller and Board Reset Circuit			AMC Enable
B42	MB_PWR	12V RAIL			Payload Power
B44	MB_Rx4+	Lane 0 Rx+	Lane 4 Rx+	Lane 20 Rx+	Port 4 Receiver +
B45	MB_Rx4-	Lane 0 Rx-	Lane 4 Rx-	Lane 20 Rx-	Port 4 Receiver -
B47	MB_Tx4+	Lane 0Tx+	Lane 4Tx+	Lane 20Tx+	Port 4 Transmitter +
B48	MB_Tx4-	Lane 0 Tx-	Lane 4 Tx-	Lane 20 Tx-	Port 4 Transmitter -
B50	MB_Rx5+	Lane 1 Rx+	Lane 5 Rx+	Lane 21 Rx+	Port 5 Receiver +
B51	MB_Rx5-	Lane 1 Rx-	Lane 5 Rx-	Lane 21 Rx-	Port 5 Receiver -
B53	MB_Tx5+	Lane 1 Tx+	Lane 5 Tx+	Lane 21 Tx+	Port 5 Transmitter +
B54	MB_Tx5-	Lane 1 Tx-	Lane 5 Tx-	Lane 21 Tx-	Port 5 Transmitter -
B56	MB_SCL_L	NC			IPMB-L Clock
B57	MB_PWR	12V rail			Payload Power
B59	MB_Rx6+	Lane 2 Rx+	Lane 6 Rx+	Lane 22 Rx+	Port 6 Receiver +
B60	MB_Rx6-	Lane 2 Rx-	Lane 6 Rx-	Lane 22 Rx-	Port 6 Receiver -
B62	MB_Tx6+	Lane 2 Tx+	Lane 6 Tx+	Lane 22 Tx+	Port 6 Transmitter +
B63	MB_Tx6-	Lane 2 Tx-	Lane 6 Tx-	Lane 22 Tx-	Port 6 Transmitter -
B65	MB_Rx7+	Lane 3 Rx+	Lane 7 Rx+	Lane 23 Rx+	Port 7 Receiver +
B66	MB_Rx7-	Lane 3 Rx-	Lane 7 Rx-	Lane 23 Rx-	Port 7 Receiver -
B68	MB_Tx7+	Lane 3 Tx+	Lane 7 Tx+	Lane 23 Tx+	Port 7 Transmitter +
B69	MB_Tx7-	Lane 3 Tx-	Lane 7 Tx-	Lane 23 Tx-	Port 7 Transmitter -
B71	MB_SDA_L	NC			IPMB-L Data
B72	MB_PWR	12V rail			Payload Power
B74	MB_TCLKA+ (CLK1)	NC			Telecom Clock A +
B75	MB_TCLKA- (CLK1)	NC			Telecom Clock A -
B77	MB_TCLKB+ (CLK2)	NC			Telecom Clock B +

Table 37: J9, J10, J44 - AMC Connector Signal Assignment *(Continued)*

Pin Number	AMC Signal	AMC1 (J9)	AMC2 (J10)	AMC3 (J44)	Description
B78	MB_TCLKB-(CLK2)	NC			Telecom Clock B -
B80	MB_FCLKA+(CLK3)	NC			Fabric Clock A +
B81	MB_FCLKA-(CLK3)	NC			Fabric Clock A -
B83	MB_PS0#	GND			Presence 0
B84	MB_PWR	12V rail			Payload Power
B87	MB_Tx8-	Lane 32 Tx+	Lane 36 Tx+	Lane 8 Tx+	Port 8 Transmitter -
B88	MB_Tx8+	Lane 32 Tx-	Lane 36 Tx-	Lane 8 Tx-	Port 8 Transmitter +
B90	MB_Rx8-	Lane 32 Rx+	Lane 36 Rx+	Lane 8 Rx+	Port 8 Receiver -
B91	MB_Rx8+	Lane 32 Rx-	Lane 36 Rx-	Lane8 Rx-	Port 8 Receiver +
B93	MB_Tx9-	Lane 33 Tx+	Lane 37 Tx+	Lane 9 Tx+	Port 9 Transmitter -
B94	MB_Tx9+	Lane 33 Tx-	Lane 37 Tx-	Lane 9 Tx-	Port 9 Transmitter +
B96	MB_Rx9-	Lane 33 Rx+	Lane 37 Rx+	Lane 9 Rx+	Port 9 Receiver -
B97	MB_Rx9+	Lane 33 Rx-	Lane 37 Rx-	Lane 9 Rx-	Port 9 Receiver +
B99	MB_Tx10-	Lane 34 Tx+	Lane 38 Tx+	Lane 10 Tx+	Port 10 Transmitter -
B100	MB_Tx10+	Lane 34 Tx-	Lane 38 Tx-	Lane 10 Tx-	Port 10 Transmitter +
B102	MB_Rx10-	Lane 34 Rx+	Lane 38 Rx+	Lane 10Rx+	Port 10 Receiver -
B103	MB_Rx10+	Lane 34 Rx-	Lane 38 Rx-	Lane 10 Rx-	Port 10 Receiver +
B105	MB_Tx11-	Lane 35 Tx+	Lane 39 Tx+	Lane 11 Tx+	Port 11 Transmitter -
B106	MB_Tx11+	Lane 35 Tx-	Lane 39 Tx-	Lane 11 Tx-	Port 11 Transmitter +
B108	MB_Rx11-	lane 35 Rx+	Lane 39 Rx+	Lane 11 Rx+	Port 11 Receiver -
B109	MB_Rx11+	Lane 35 Rx-	Lane 39 Rx-	Lane 11 Rx-	Port 11 Receiver +
B111	MB_Tx12-	NC			Port 12 Transmitter -
B112	MB_Tx12+	NC			Port 12 Transmitter +
B114	MB_Rx12-	NC			Port 12 Receiver -
B115	MB_Rx12+	NC			Port 12 Receiver +
B117	MB_Tx13-	NC			Port 13 Transmitter -

Table 37: J9, J10, J44 - AMC Connector Signal Assignment *(Continued)*

Pin Number	AMC Signal	AMC1 (J9)	AMC2 (J10)	AMC3 (J44)	Description
B118	MB_Tx13+	NC			Port 13 Transmitter +
B120	MB_Rx13-	NC			Port 13 Receiver -
B121	MB_Rx13+	NC			Port 13 Receiver +
B123	MB_Tx14-	NC			Port 14 Transmitter -
B124	MB_Tx14+	NC			Port 14 Transmitter +
B126	MB_Rx14-	NC			Port 14 Receiver -
B127	MB_Rx14+	NC			Port 14 Receiver +
B129	MB_Tx15-	NC			Port 15 Transmitter -
B130	MB_Tx15+	NC			Port 15 Transmitter +
B132	MB_Rx15-	NC			Port 15 Receiver -
B133	MB_Rx15+	NC			Port 15 Receiver +
B135	MB_TCLKC-	NC			Telecom Clock C -
B136	MB_TCLKC+	NC			Telecom Clock C +
B138	MB_TCLKD-	NC			Telecom Clock D -
B139	MB_TCLKD+	NC			Telecom Clock D +
B141	MB_Tx17-	NC			Port 17 Transmitter -
B142	MB_Tx17+	NC			Port 17 Transmitter +
B144	MB_Rx17-	NC			Port 17 Receiver -
B145	MB_Rx17+	NC			Port 17 Receiver +
B147	MB_Tx18-	NC			Port 18 Transmitter -
B148	MB_Tx18+	NC			Port 18 Transmitter +
B150	MB_Rx18-	NC			Port 18 Receiver -
B151	MB_Rx18+	NC			Port 18 Receiver +
B153	MB_Tx19-	NC			Port 19 Transmitter -
B154	MB_Tx19+	NC			Port 19 Transmitter +
B156	MB_Rx19-	NC			Port 19 Receiver -
B157	MB_Rx19+	NC			Port 19 Receiver +
B159	MB_Tx20-	NC			Port 20 Transmitter -

Table 37: J9, J10, J44 - AMC Connector Signal Assignment *(Continued)*

Pin Number	AMC Signal	AMC1 (J9)	AMC2 (J10)	AMC3 (J44)	Description
B160	MB_Tx20+	NC			Port 20 Transmitter +
B162	MB_Rx20-	NC			Port 20 Receiver -
B163	MB_Rx20+	NC			Port 20 Receiver +
B165	MB_TCK	NC			JTAG Test clock Input
B166	MB_TMS	NC			JTAG Test Mode Select In
B167	MB_TRST#	NC			JTAG Test Reset Input
B168	MB_TDO	NC			JTAG Test clock Output
B169	MB_TDI	NC			JTAG Test clock Input

4.2.2 SMA Connectors

The switch lane connected to SMA connectors are assigned as follows:

- Each TX+ connects to one SMA
- Each TX- connects to one SMA adjacent to TX+
- Each RX+ connects to one SMA
- Each RX- connects to one SMA adjacent to RX+

In total, there are 16 SMA connectors per quadrant. The lanes are identified on the PCB as shown in Figure 18 and Figure 19

Figure 18: Signal Distribution on SMA Connectors (CPS-1848)

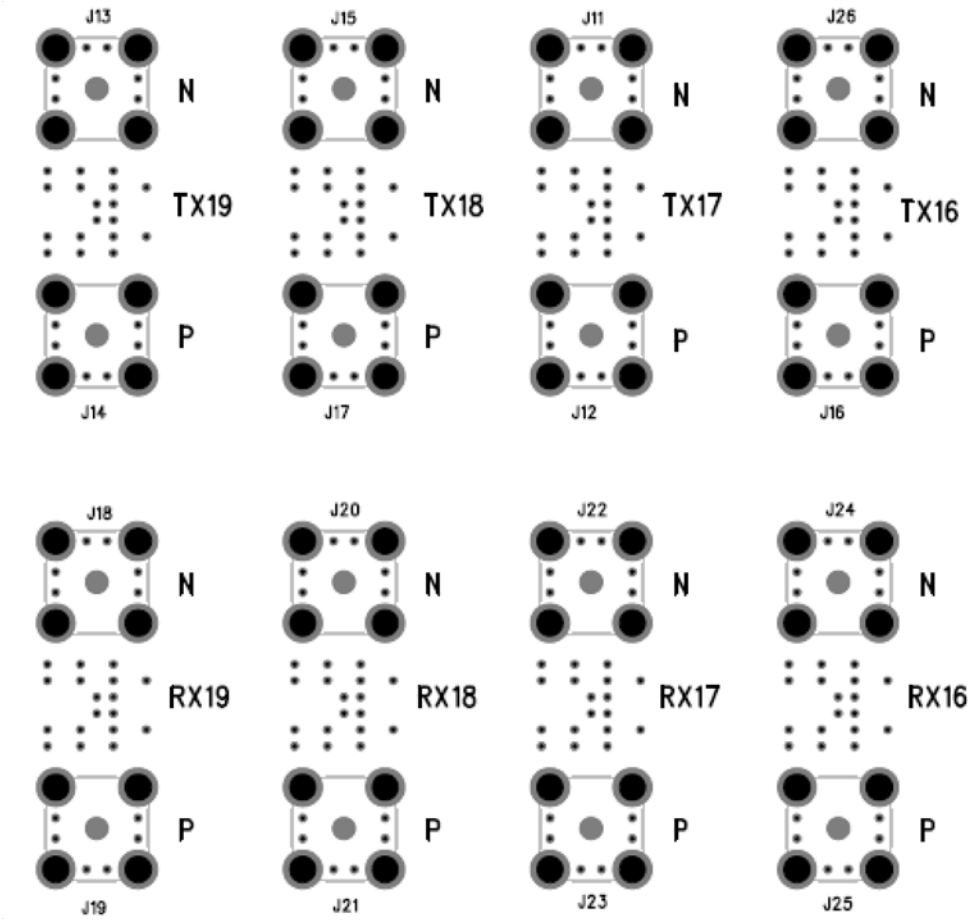
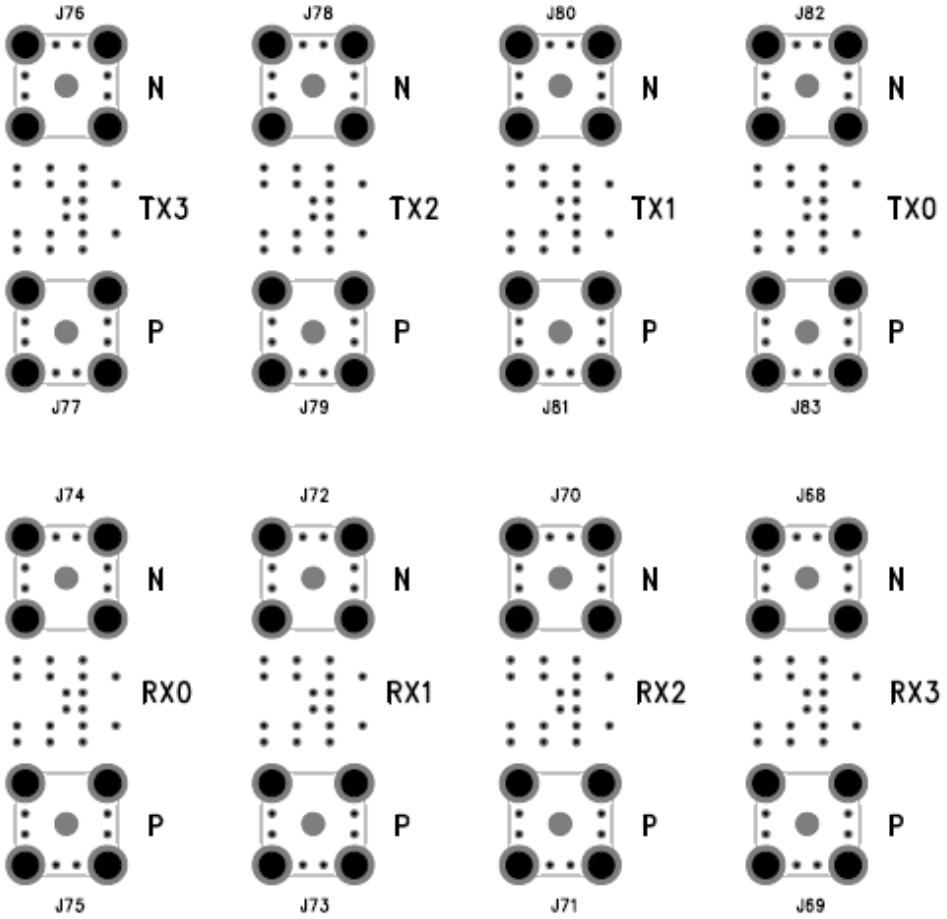


Figure 19: Signal Distribution on SMA Connectors (SPS-1616)



4.2.3 J45 - J62 - J66 - J67 InfiniBand Connectors

Fujitsu's MicroGIGaCN FCN268-D008G/1D InfiniBand connectors and cable assemblies are targeted for 2.5 Gbaud (per link) applications.

- Insertion loss – 2.3dB @ 2.5 Gbaud (1.25 GHz, 1 Meter Cable Assembly)
- Skew within differential pair – 14.4 ps (2 connectors and 2 meter of cable)
- Skew pair to pair – 21.2 ps (2 connectors and 2 meter of cable)

Switch lane to connector mapping is displayed in Table 38. The connector pinout is described in Figure 20. S(1) and S(2) are connected to a differential pair. There are eight differential pairs on the connector. The switch lane to connector connection is wired to match the InfiniBand connectivity specification. As such, it is possible to connect to any other InfiniBand compatible board using an InfiniBand crossover cable.

Figure 20: InfiniBand Connector Pin Assignment

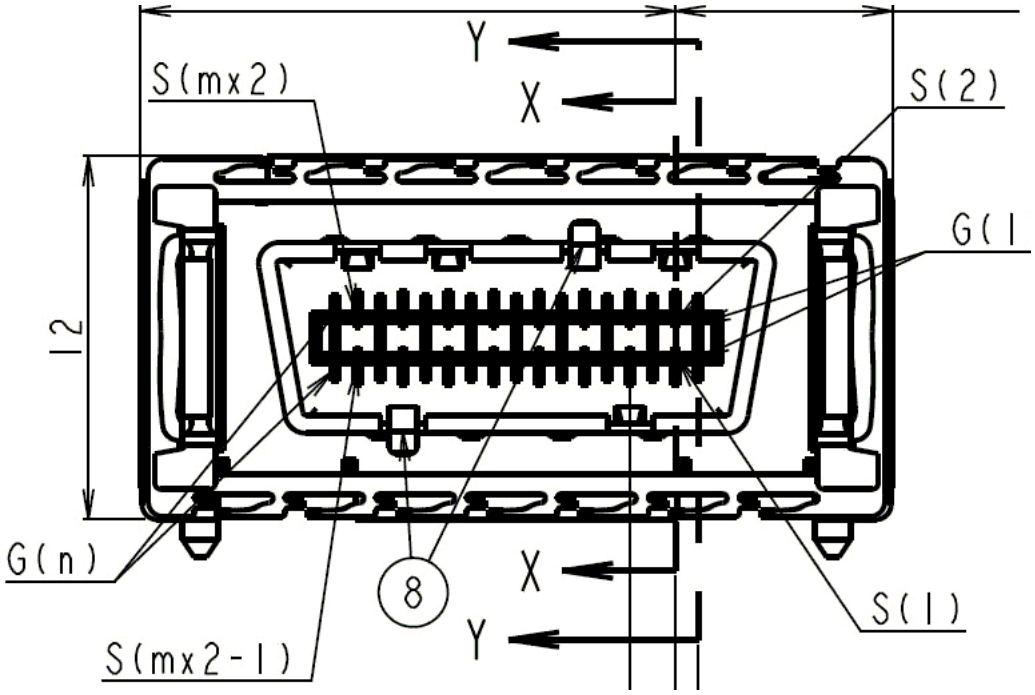


Table 38: J45 - J62 - J66 - J67 InfiniBand Connector to Switch Lane Mapping

Connector Pin Number	InfiniBand Signal Name	CPS-1848		SPS-1616	
		J45	J62	J66	J67
S1	IBtxIp(0)	Lane 28 Rx+	Lane 44 Rx+	Lane 4 Rx+	Lane 8 Rx+
S2	IBtxIn(0)	Lane 28 Rx-	Lane 44 Rx-	Lane 4 Rx-	Lane 8 Rx-
S3	IBtxIp(1)	Lane 29 Rx+	Lane 45 Rx+	Lane 5 Rx+	Lane 9 Rx+
S4	IBtxIn(1)	Lane 29 Rx-	Lane 45 Rx-	Lane 5 Rx-	Lane 9 Rx-
S5	IBtxIp(2)	Lane 30 Rx+	Lane 46 Rx+	Lane 6 Rx+	Lane 10 Rx+
S6	IBtxIn(2)	Lane 30 Rx-	Lane 46 Rx-	Lane 6 Rx-	Lane 10 Rx-
S7	IBtxIp(3)	Lane 31 Rx+	Lane 47 Rx+	Lane 7 Rx+	Lane 11 Rx+
S8	IBtxIn(3)	Lane 31 Rx-	Lane 47 Rx-	Lane 7 Rx-	Lane 11 Rx-
S9	IBtxOn(3)	Lane 31 Tx-	Lane 47 Tx-	Lane 7 Tx-	Lane 11 Tx-
S10	IBtxOp(3)	Lane 31 Tx+	Lane 47 Tx+	Lane 7 Tx+	Lane 11 Tx+
S11	IBtxOn(2)	Lane 30 Tx-	Lane 46 Tx-	Lane 6 Tx-	Lane 10 Tx-
S12	IBtxOp(2)	Lane 30 Tx+	Lane 46 Tx+	Lane 6 Tx+	Lane 10 Tx+
S13	IBtxOn(1)	Lane 29 Tx-	Lane 45 Tx-	Lane 5 Tx-	Lane 9 Tx-

Table 38: J45 - J62 - J66 - J67 InfiniBand Connector to Switch Lane Mapping *(Continued)*

Connector Pin Number	InfiniBand Signal Name	CPS-1848		SPS-1616	
		J45	J62	J66	J67
S14	IBtxOp(1)	Lane 29 Tx+	Lane 45 Tx+	Lane 5 Tx+	Lane 9 Tx+
S15	IBtxOn(0)	Lane 28 Tx-	Lane 44 Tx-	Lane 4 Tx-	Lane 8 Tx-
S16	IBtxOp(0)	Lane 28 Tx+	Lane 44 Tx+	Lane 4 Tx+	Lane 8 Tx+

4.2.4 J42 - QSFP Connector

The QSFP connectors on the SRDP2 can support an active optical module, or a passive cable assembly based on the INF-8438 Multi Source Agreement. The QSFP is connected as displayed in Table 39. The QSFP connector is part number 1761987-9 from Tyco. The cage is part number 1888617-1 from Tyco.

Figure 21: QSFP Cage

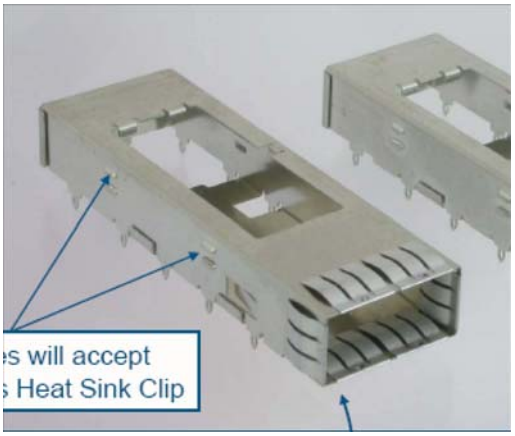


Table 39: QSFP Connectors

Pin Number	QSFP MSA Signal Name	QSFP J42 Connection
1	GND	GND
2	TX2n	CPS-1848 TX25_n
3	TX2p	CPS-1848 TX25_p
4	GND	GND
5	Tx4n	CPS-1848 TX27_n
6	Tx4p	CPS-1848 TX27_p
7	GND	GND
8	ModSelL	NC
9	LPMode_Reset	NC

Table 39: QSFP Connectors *(Continued)*

Pin Number	QSFP MSA Signal Name	QSFP J42 Connection
10	VccRx	3.3V
11	SCL	NC
12	SDA	NC
13	GND	GND
14	Rx3p	CPS-1848 RX26_p
15	Rx3n	CPS-1848 RX26_n
16	GND	GND
17	Rx1p	CPS-1848 RX24_p
18	RX1n	CPS-1848 RX24_n
19	GND	GND
20	GND	GND
21	RX2n	CPS-1848 RX25_n
22	RX2p	CPS-1848 RX25_p
23	GND	GND
24	RX4n	CPS-1848 RX27_n
25	RX4p	CPS-1848 RX27_p
26	GND	GND
27	ModPrsL	NC
28	IntL	NC
29	VccTx	3.3V
30	Vcc1	3.3V
31	Reserved	NC
32	GND	GND
33	TX3p	CPS-1848 TX26_p
34	TX3n	CPS-1848 TX26_N
35	GND	GND
36	TX1p	CPS-1848 TX24_p
37	TX1n	CPS-1848 TX24_n
38	GND	GND

4.2.5 J57 - J58 SFP Connectors

There are two SFP connectors on the SRDP2. Each SFP is connected as indicated in Table 40. The SFP+ connector is part number 1888247-1 from Tyco. The cage is part number 1489962-3 from Tyco. Signal assignment is based on the SFP+ (SFF-8431) Multi Source Agreement.

Figure 22: SFP Cage

Table 40: SFP Connectors

Pin Number	SFF-8431 Signal Name	Function	J57	J58
1	VeeT	Transmitter Ground	GND	
2	TX Fault	Transmitter Fault Indication	Fault LED	
3	TX Disable	Transmitter Disable	GND (always enabled)	
4	SDA	2-wire Serial Interface Data Line (Same as MOD-DEF2 in INF-8074i)	NC	NC
5	SCL1	2-wire Serial Interface Clock (Same as MOD-DEF1 in INF-8074i)	NC	NC
6	Mod ABS	Module Absent, connected to VeeT or VeeR in the module	NC	NC
7	RS0	Rate Select 0, optionally controls SFP+ module receiver	Pull-up with shunt jumper J97 to GND	Pull-up with shunt jumper J98 to GND
8	RX_LOS	Receiver Loss of Signal Indication (In FC designated as Rx_LOS and in Ethernet designated as Signal Detect)	LOS LED	
9	RS1	Rate Select 1, optionally controls SFP+ module transmitter	Pull-up with shunt J96 jumper to GND	Pull-up with shunt J99 jumper to GND

Table 40: SFP Connectors *(Continued)*

Pin Number	SFF-8431 Signal Name	Function	J57	J58
10	VeeR	Receiver Ground	GND	
11	VeeR	Receiver Ground	GND	
12	RD-	Inv. Received Data Out	CPS-1848 RX12_p	CPS-1848 RX14_p
13	RD+	Received Data Out	CPS-1848 RX12_n	CPS-1848 RX14_n
14	VeeR	Receiver Ground	GND	
15	VccR	Receiver Power	3.3V	
16	VccT	Transmitter Power	3.3V	
17	VeeT	Transmitter Ground	GND	
18	TD+	Transmit Data In	CPS-1848 TX12_p	CPS-1848 TX14_p
19	TD-	Inv. Transmit Data In	CPS-1848 TX12_n	CPS-1848 TX14_n
20	VeeT	Transmitter Ground	GND	

4.3 J28 - Optional 25-MHz Clock Input

The SMA connector at J28 can provide an external 25-MHz clock to the clock synthesizer. Use the REF_SEL setting on S6.3 to select the external source. The external clock source must be 3.3V LVTTL or LVCMOS levels.

4.4 J27 and J29, 156.25-MHz LVDS Clock Outputs

Use J27 and J29 to monitor the output of the clock synthesizer. They are LVDS differential signals and are not AC coupled.

- J27 is output clock +
- J29 is output clock -

4.5 J32 and J61 ATX Power Connectors

Use a standard ATX power supply to connect to J32. If several high power AMC cards are plugged in, IDT recommends to also connect J61; otherwise, J61 is optional.

Figure 23: J32 - ATX Power Connector Pinout

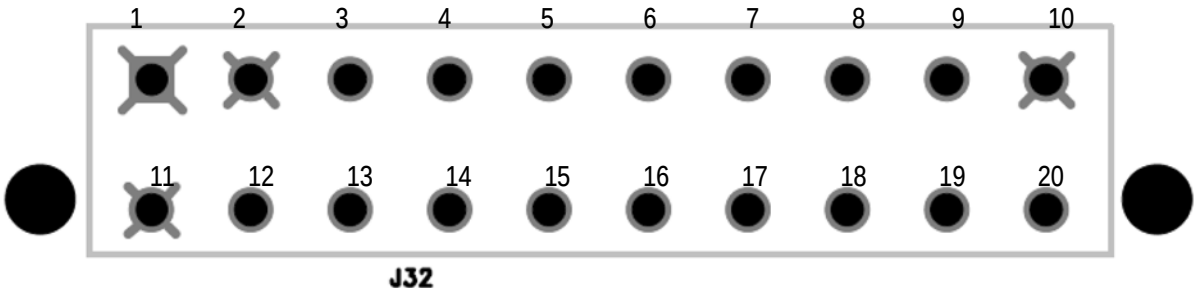


Table 41: J32 - ATX Power Connector Signal Description

Pin Number	Description	Pin Number	Description
1	3.3V	11	3.3V
2	3.3V	12	-12V
3	GND	13	GND
4	5V	14	PS ON
5	GND	15	GND
6	5V	16	GND
7	GND	17	GND
8	POWER OK	18	-5V
9	5VSB	19	5V
10	12V	20	5V

Figure 24: J61 - Optional 12V ATX Supply

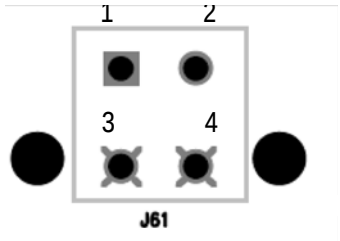


Table 42: J61 - Signal Description

Pin Number	Description
1	GND
2	GND
3	12V
4	12V

4.6 J30 - JTAG Header

J30 is used to connect the SRDP2's JTAG chain to an external JTAG pod. When an external JTAG pod is used, the USB cable (J60) must be disconnected; otherwise, there will be contention between the external pod and the on-board USB-JTAG controller.

Figure 25: J30 - JTAG Header

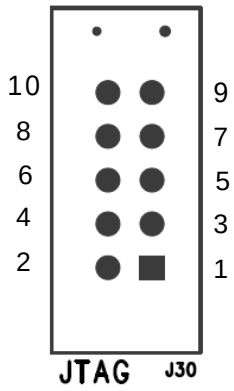


Table 43: J30 - Signal Description

Pin Number	Description
1	TRST#
2	GND
3	TDI
4	GND
5	TDO
6	GND
7	TMS
8	GND
9	TCK
10	GND

4.7 J59 - I2C Header

J59 is used to connect the SRDP2's I2C chain to an external I2C pod. When an external I2C pod is used, the USB cable (J60) must be disconnected; otherwise, there will be contention between the external pod and the on-board USB-I2C controller.

Figure 26: J59 - I2C Header

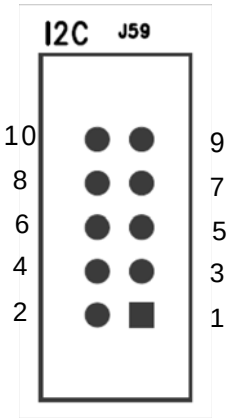


Table 44: J59 - Signal Description

Pin Number	Description
1	SCL
2	GND
3	SDA
4	NC
5	NC
6	NC
7	NC
8	NC
9	NC
10	GND

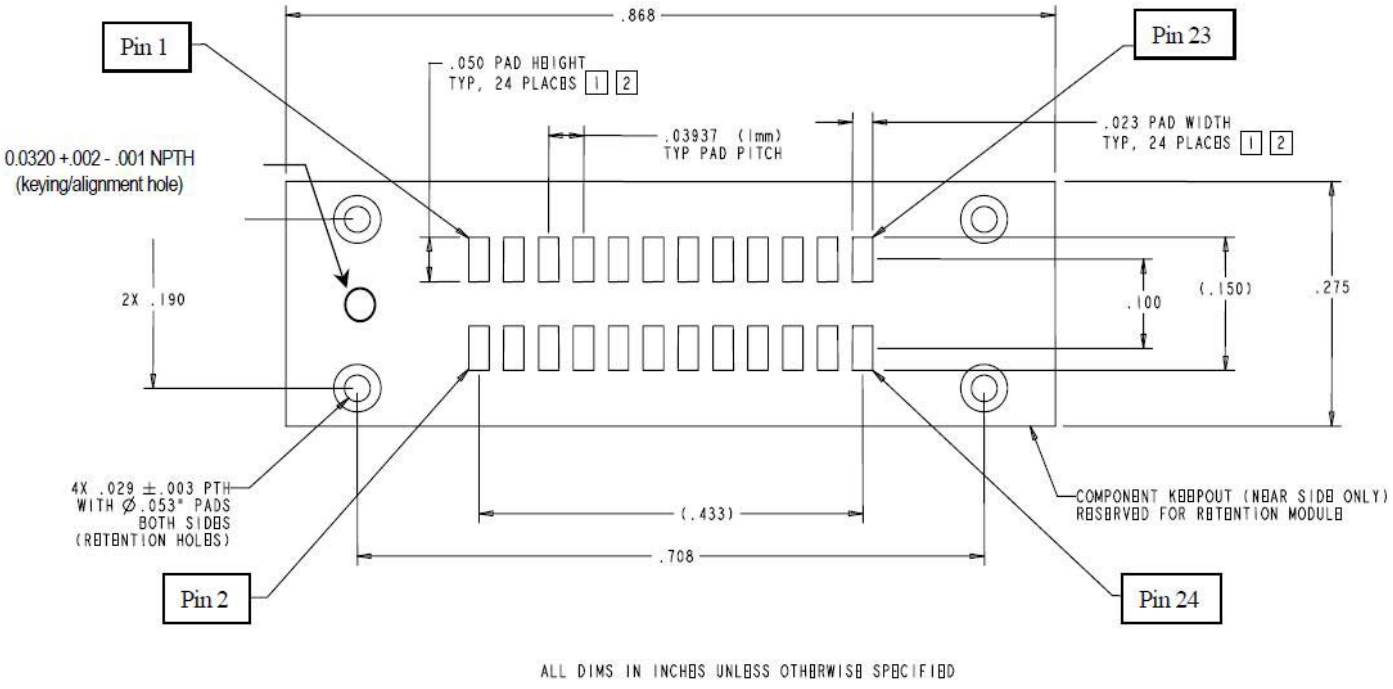
4.8 J60 - USB Connector

Use a standard USB type-B cable to connect a host PC to the on-board USB controller. The on-board USB controller uses power for the USB host (the PC). When the SRDP2 is powered off, the USB controller can still be detected by the host PC.

4.9 Logic Analyzer Pads

All S-RIO lanes are connected to a logic analyzer pad. Use the SRDP2 schematic to identify the location and the lanes on the logic analyzer pads. The footprint for the logic analyzer probe is compatible with Nexus Technology's Mid-bus Serial Probe.

Figure 27: Logic Analyzer Footprint



4.10 J95 - Fan Sink Power Connector

J95 is used to connect the fan sink's power. The fan uses 12V.

Table 45: J95 - Signal Description

Pin Number	Description
1	GND
2	12V
3	NC

5. PCB and Mechanical

This chapter describes the PCB and mechanical characteristics of the SRDP2.

5.1 Board Stack-up

The SRDP2 is built with FR4-08 material. The PCB is composed of ten layers (see Figure 28). Of the ten layers four are used for routing signals, two are grounds, and four are power planes.

Figure 28: Board Stack-up

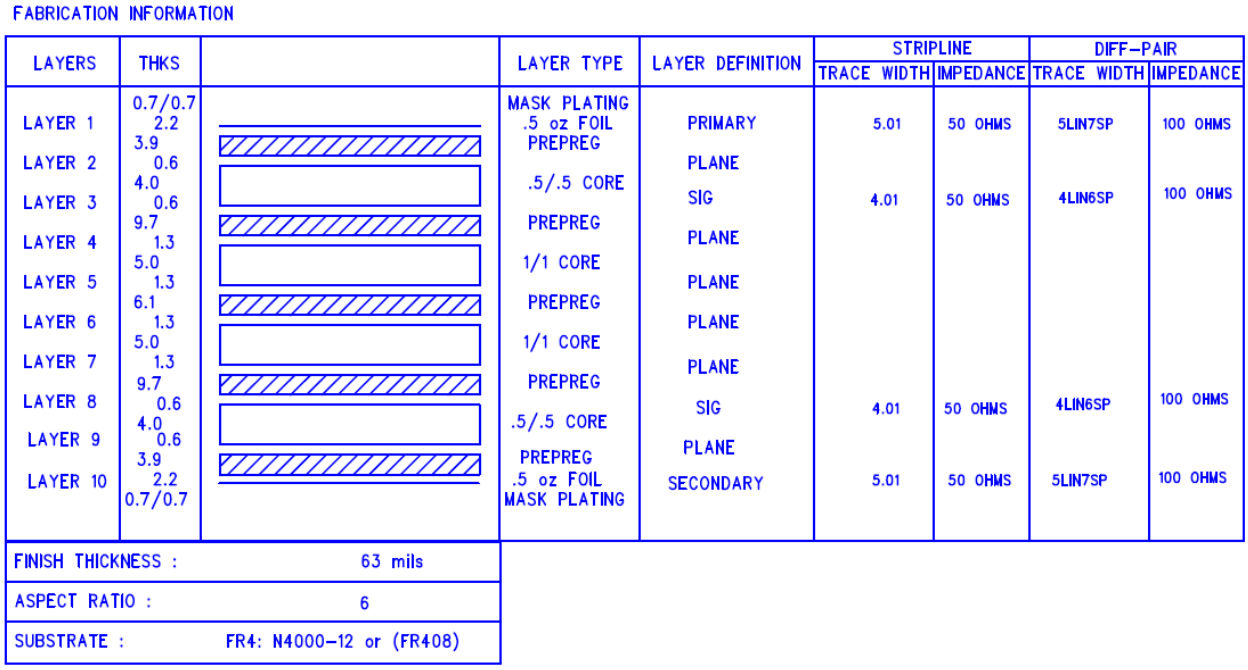


Table 46: Layer Assignment

Layer Number	Designation	Assignment
1	TOP	Most Components Differential Traces
2	GND1	Solid, continuous ground plane
3	SIG1	Differential Traces Low frequency signals
4	PWR1	Power, 3.3V
5	PWR2	Power, 1.0V and 12V

Table 46: Layer Assignment *(Continued)*

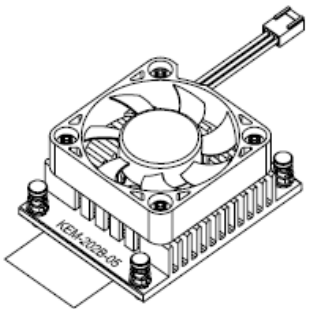
Layer Number	Designation	Assignment
6	PWR3	Power, 1.0V (VDDA/VDDS), 12V_AMC
7	PWR4	Power, 1.2V
8	SIG2	Differential Traces Low frequency signals
9	GND2	Solid, continuous ground plane
10	BOTTOM	Decoupling and passive Differential Traces

5.2 Thermal

5.2.1 Thermal (CPS-1848)

The CPS-1848 maximum power draw is 8.53W. With no heatsink and no airflow, the junction temperature would rise up to 121°C above ambient. The maximum junction temperature can be exceeded without the help of a heatsink. The fansink mounted on the BGA reduces the case-to-ambient resistance to 1.08°C/W.

Figure 29: Heatsink with Fan Mounted on CPS-1848



5.2.2 Thermal (SPS-1616)

At 5.123W maximum power draw, the junction temperature is expected to rise to 80°C above ambient temperature with no air flow. For example, if the ambient temperature is 25°C, the junction temperature should not exceed 105°C. In a normal interior environment a heatsink is not required.

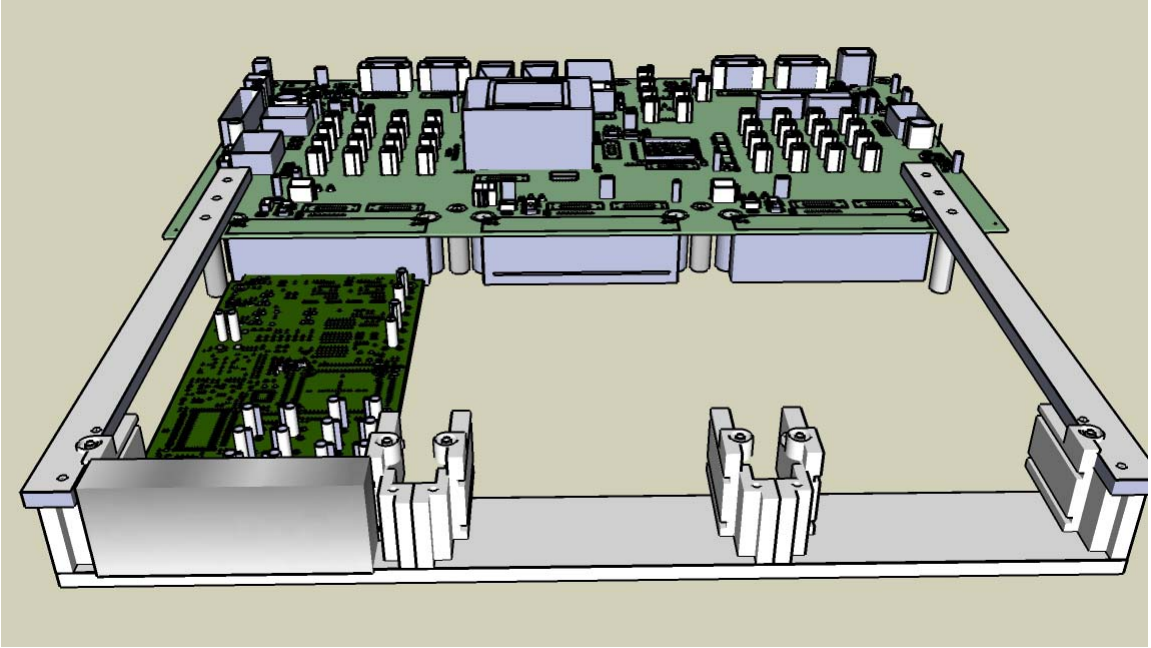
Table 47: Junction Temperature (SPS-1616)

Power	Jc+Ja	Junction Temperature at Ambient 25°C
5.2W (max)	80°C	105°C
4.2W (normal)	65°C	90°C
1.7W (min)	26°C	51°C

5.3 AMC Bay and Card Guide Assembly

The three AMC bays provide card guides for proper support of the modules. AMC modules are inserted in the card guide right side-up, such that the top of the modules face upward. This permits full size (and taller) modules to be used without any restriction. If AMC modules require cooling, a bench-top fan shall be used.

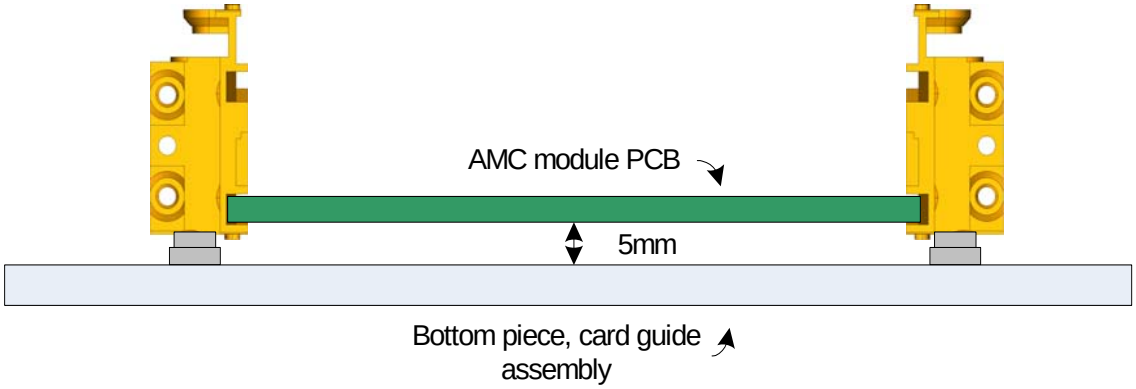
Figure 30: AMC Module Insertion Orientation



5.3.1 Bottom Clearance

The clearance between the bottom portion of the card guide assembly and the AMC PCB is higher than the maximum component height on the bottom side of the modules. There is a space of 5 mm between the bottom of the module's PCB and the card guide assembly.

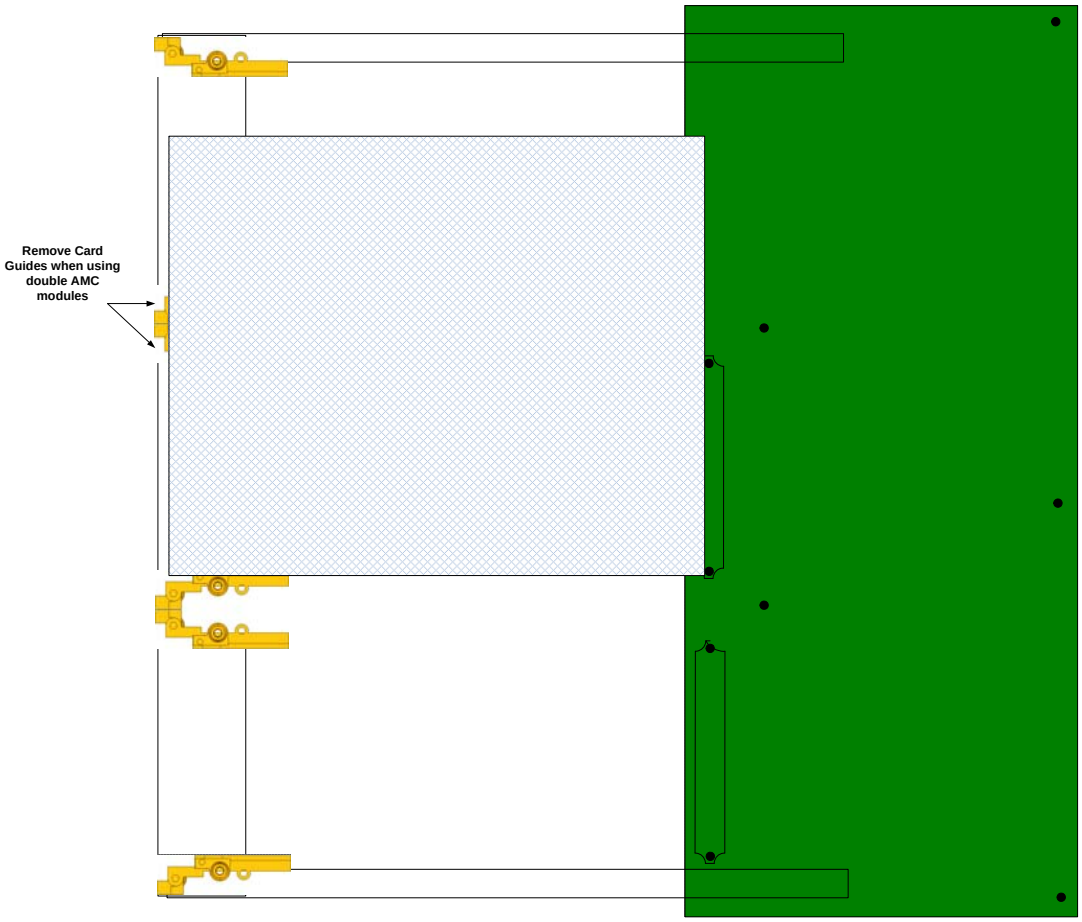
Figure 31: AMC Module – Bottom Side Clearance



5.3.2 AMC Double Modules

A double module can be inserted in the AMC card guides. In order to clear the space near the faceplate area, two of the card guide must be removed.

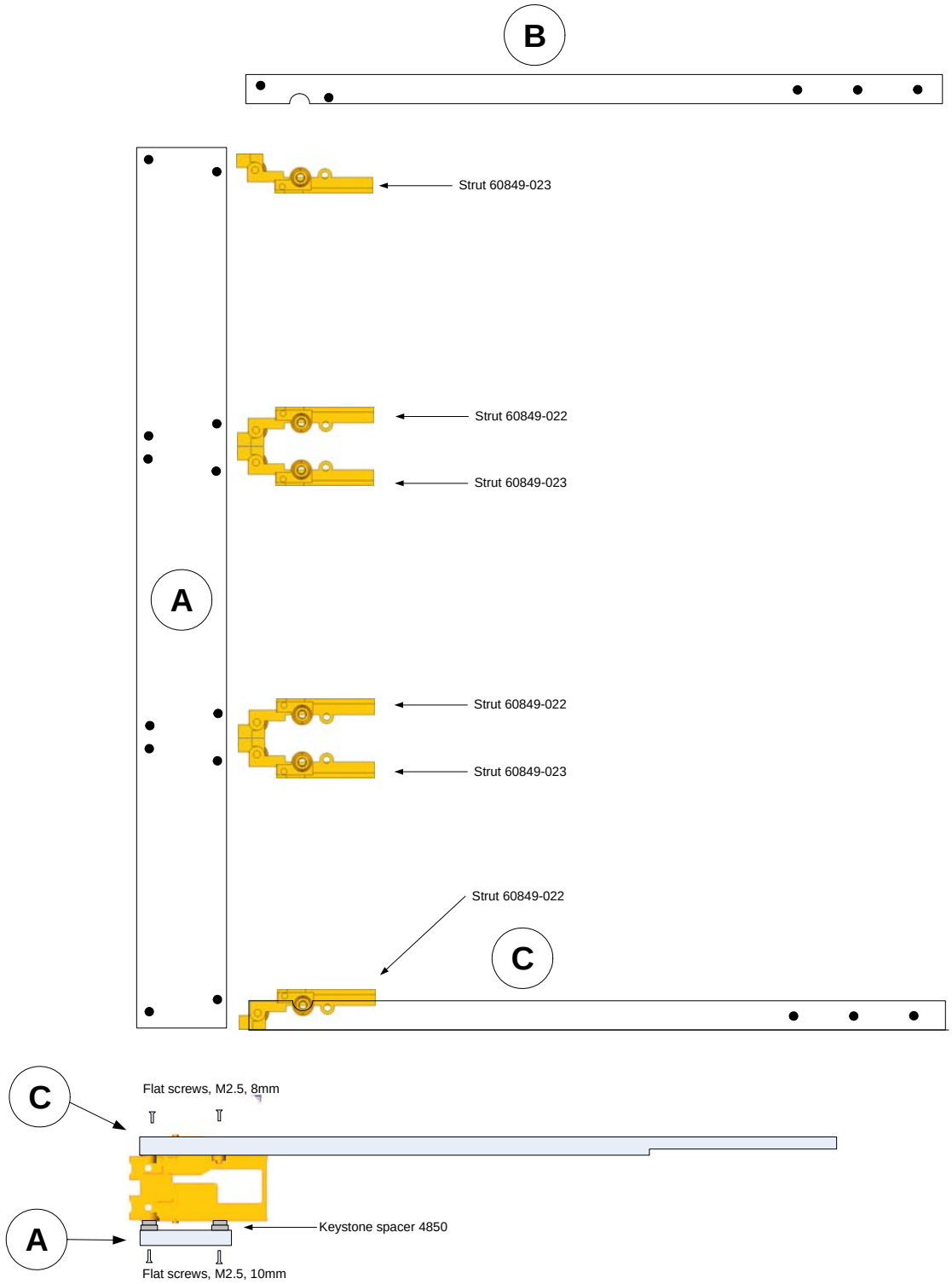
Figure 32: AMC Double Module Area



5.3.3 Card Guide Assembly

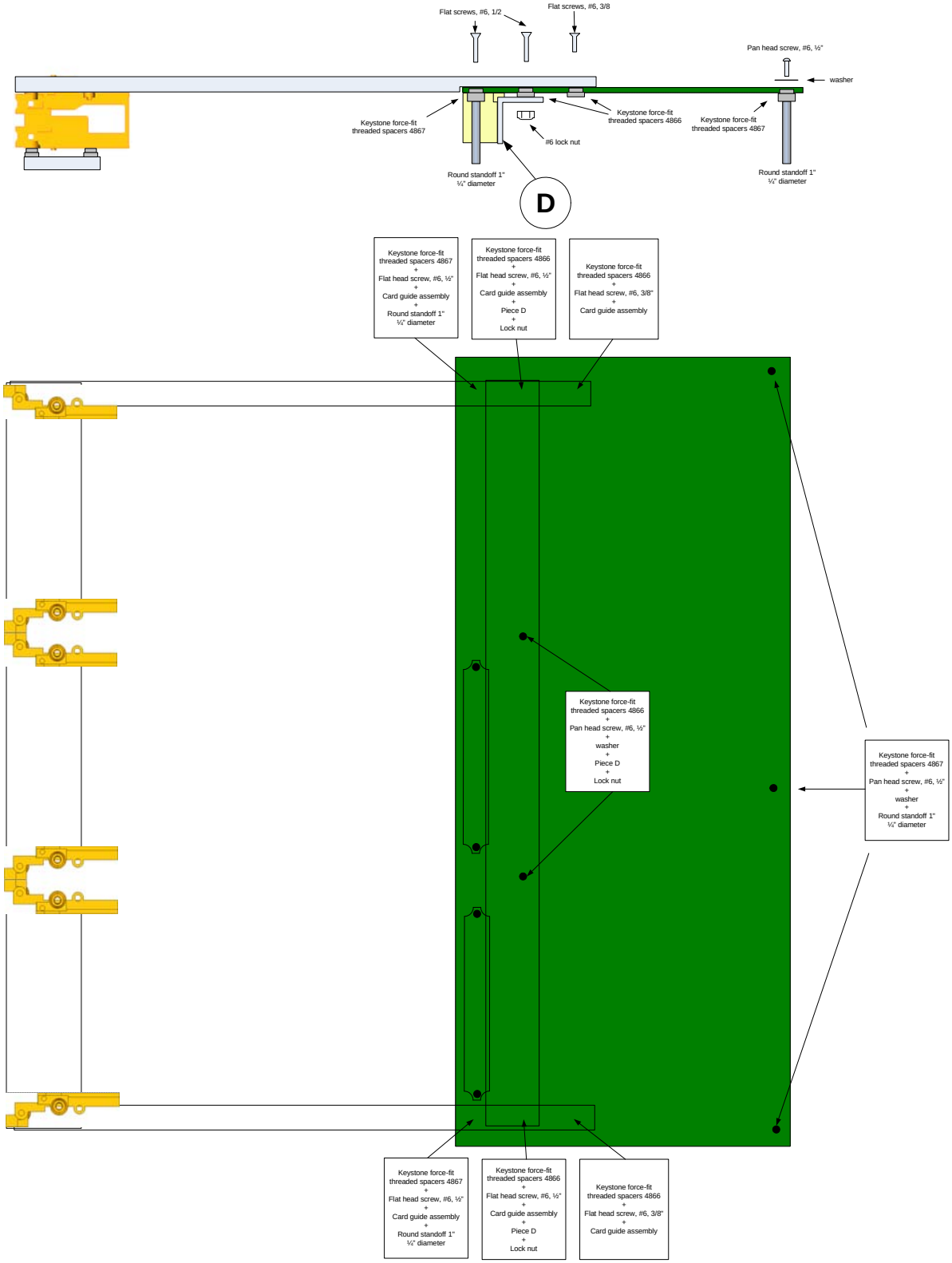
The AMC card guide assembly is made with custom aluminium parts and Schroff's ATCA struts. The assembly is very sturdy. If the assembly becomes loose, the screw should be tightened with a phillips screw driver.

Figure 33: Card Guide Assembly



5.3.4 SRDP2 Mechanical Assembly

Figure 34: SRDP2 Mechanical Assembly



6. Recommended Cables

This chapter discusses the recommended cables to use with the SRDP2.

6.1 CX4 Infiniband Cable Assemblies

Infiniband cables are offered in various length and signaling rate specification.

Single Data Rate (SDR) infiniband cables are specified for 2.5 Gbps signaling rate. They are suitable for the SPS-1616 and CPS-1848 switches at bit rates up to 6.25 Gbps, and in lengths up to 2 meters. Longer SDR cables (2–5 meters) may also be suitable for 5 and 6.25 Gbps bit rates with the SPS-1616 and CPS-1848. However, each switch's SerDes will likely require signal strength and post/pre-emphasis adjustments.

Double Data Rate (DDR) infiniband cables are specified for 5 Gbps signaling rate. They are better suited for bit rates higher than 3.125Gbps and length longer than 2 meters.

Table 48: Infiniband Cable Vendors

Vendor	Product Description	Part Number
FCI	EyeMax Infiniband 4x cable assembly, 1 meter	10007290-N0100CULF
Molex	LaneLink Infiniband 4x cable assembly, 1 meter	74506-3002
Amphenol	4X SDR InfiniBand cable with Fujitsu InfiniBand connectors (SFF-8470 Latch), 1 meter	NW-28INFINI4X-001 (www.cablesondemand.com)

6.2 QSFP+ Passive (Unequalized) Cables

QSFP+ cables are typically specified for 5 Gbps and faster bit rates. QSFP+ cables of various length are suitable for the CPS-1848 switch.

Table 49: QSFP Cable Vendors

Vendor	Product Description	Part Number
FCI	QSFP+ cable assembly, 30 AWG, 1 meter, passive	10093084-2010LF
3M	3M™ Twin axial cable assemblies for QSFP+ applications, 9Q series, 1 meter	9QA0-111-01-1.00
Molex	QSFP-to-QSFP cable assembly, 30 AWG, 1 meter	74757-1101
Tyco Electronics	QSFP/QSFP+ cable assembly, 1 meter	2053638-1

6.3 SFP+ Passive (Unequalized) Cables

SFP+ cables are typically specified for 10 Gbps and faster signal rates. SFP+ cables of various length are suitable for the CPS-1848 switch.

Table 50: SFP Cable Vendors

Vendor	Product Description	Part Number
FCI	SFP+ cable assembly, 32 AWG, 1 meter, passive	10110818-1010LF
3M	Cable assemblies for SFP+ applications, 1410 series, 1 meter	1410-P-15-00-1.00
Molex	SFP+ passive cable assembly, 10 Gbps, 28 AWG cable, Pull-to-release plunger style latch, 1 meter	74752-2101
Tyco	Cable assembly sub-type; SFP+, 1 meter	2127934-2
Amphenol	SFP+ cable - amphenol 10 GbE SFP+ Direct attach copper cable, 1 meter	SFPP2EPASS-001

6.4 SMA Cables

SMA cables are made of SMA type connectors and a 50 Ohm coaxial cable. Cable assemblies are available in various length and RF characteristics. When selecting a coaxial cable, consider the insertion loss of the cable at 3.125 GHz (for bit rates of 6.25 Gbps). Use cables that have total insertion loss of less than 10dB. Use cables that are length matched (±3 mm or better) within a differential pair. Length matching is not required, however, between lanes of the same port.

Table 51: SMA Cable Vendors

Vendor	Website
Lighthorse	www.rfconnector.com
Rosenberger	www.rosenbergerna.com
Amphenol Connex	www.amphenolconnex.com
Samtec	www.samtec.com

7. Ordering Information

The SRDP2 platform is available from Silicon Turnkey Express (see www.silicontkx.com).

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