Description

This document describes the specification for the F1953 Digital Step Attenuator. The F1953 is part of a family of *Glitch-Free™* DSAs optimized for the demanding requirements of communications Infrastructure. These devices are offered in a compact 4 x 4 mm QFN package with 50Ω impedances for ease of integration.

Competitive Advantage

Digital step attenuators are used in Receivers and Transmitters to provide gain control. The F1953 is a 6-bit step attenuator optimized for these demanding applications. The silicon design has very low insertion loss and low distortion (> +60dBm $IP3_I$.) The device has pinpoint accuracy and settles to final attenuation value within 400ns. Most importantly, the F1953 includes Renesas' ***Glitch-Free™*** technology which results in less than 0.5dB of overshoot ringing during MSB transitions. This is in stark contrast to competing DSAs that *glitch as much as 10dB*.

- ✓ Lowest insertion loss for best SNR
- ✓ Glitch-Free™ when transitioning – won't damage PA or ADC
- ✓ Extremely accurate with low distortion

Applications

- Base Station 2G, 3G, 4G, TDD radio-cards
- Repeaters and E911 systems
- Digital Pre-Distortion
- Point to Point Infrastructure
- Public Safety Infrastructure
- WIMAX Receivers and Transmitters
- Military Systems, JTRS radios
- RFID handheld and portable readers
- Cable Infrastructure

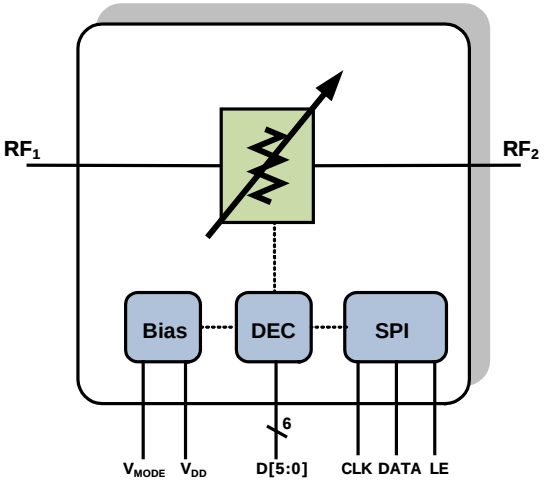
Part# Matrix

Part#	Freq range	Resolution / Range	Control	IL	Pinout
F1950	150 - 4000	0.25 / 31.75	Parallel & Serial	-1.3	PE43702 PE43701
F1951	100 - 4000	0.50 / 31.5	Serial Only	-1.2	HMC305
F1952	100 – 4000	0.50 / 15.5	Serial Only	-0.9	HMC305
F1953	**400 - 4000**	**0.50 / 31.5**	**Parallel & Serial**	**-1.3**	**PE4302** **DAT-31R5**

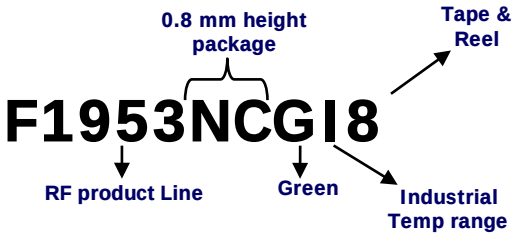
Features

- *Glitch-Free™*, < 0.6dB transient overshoot
- Spurious Free Design
- 2.7 to 3.6 V supply
- Attenuation Error < 0.5dB at 2GHz
- Low Insertion Loss < 1.4dB at 2GHz
- Excellent Linearity >+60dBm $IP3_I$
- Fast settling time, < 400ns
- Serial or Parallel Interface 31.5dB Range
- Stable Integral Non-Linearity over temperature
- Low Power Consumption < 200µA
- Integrated DC blocking capacitors
- Drop-In replacement
- 4 x 4 mm thin 20-VFQFPN package

Device Block Diagram



Ordering Information



ABSOLUTE MAXIMUM RATINGS

V_{DD} to GND	-0.3V to +4.0V
D[5:0], DATA, CLK,LE,V_{MODE}	-0.3V to 3.6V
RF Input Power (RF1, RF2) calibration and testing	+29dBm
RF Input Power (RF1, RF2) continuous RF operation	+23dBm
θ_{JA} (Junction – Ambient)	+50°C/W
θ_{JC} (Junction – Case) The Case is defined as the exposed paddle	+3°C/W
Operating Temperature Range (Case Temperature)	T_C = -40°C to +100°C
Maximum Junction Temperature	140 °C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (soldering, 10s)	+260°C

Stresses above those listed above may cause permanent damage to the device. Functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD Caution

This product features proprietary protection circuitry. However, it may be damaged if subjected to high energy ESD. Please use proper ESD precautions when handling to avoid damage or loss of performance.

F1953 RECOMMENDED OPERATING CONDITIONS

Parameter	Comment	Sym	Min	Typ	Max	Units
Supply Voltage	Main Supply	V_{DD}	2.7	3.0	3.6	V
Temperature Range	Operating Range (Case)	T_C	-40		+100	°C
Frequency Range	Operating Range	F_{RF}	400		4000	MHz
RF1 Impedance	Single-Ended	Z_{RF1}		50		Ω
RF2 Impedance	Single-Ended	Z_{RF2}		50		Ω

F1953 SPECIFICATION (31.5 dB Range)

Specifications apply at **V_{DD} = +3.0 V**, **f_{RF} = 2000 MHz**, T_C= +25°C, V_{MODE} > V_{IH} (Serial Mode) EVkit losses are de-embedded.

Parameter	Comment	Sym	Min	Typ	Max	Units
Logic Input High	CLK, DATA, LE, V_{MODE}, D[5:0]	**V_{IH}**	***0.7xV_{DD}***		***V_{DD}***	V
Logic Input Low	CLK, DATA, LE, V_{MODE}, D[5:0]	**V_{IL}**			***0.3xV_{DD}***	V
Logic Current	V_{MODE}, D[5:0]	**I_{IH}, I_{IL}**	***-5***		***+5***	µA
Logic Current	LE	**I_{IH}, I_{IL}**	***-35***		***+35***	µA
Supply Current	Total V_{DD} = 3V	**I_{DD}**		***0.16***	***0.25***[1]	mA
RF1,RF2 Return Loss	20*log(**S_{11}**), 20*log(**S_{22}**)	**S_{11},S_{22}**		-23		dB
Minimum Attenuation	D[5:0] = [000000]	**A_{MIN}**		***1.35***	***1.90***	dB
Maximum Attenuation	D[5:0] = [111111]	**A_{MAX}**	32.0	32.4		dB
Minimum Gain Step	Least Significant Bit	**LSB**		0.50		dB
Phase Delta	Phase change A_{MIN} vs. A_{MAX}	**Φ_{Δ}**		39		deg
Differential ATTN Error	Between adjacent steps	**DNL**		0.09		dB
Integral ATTN Error	Error vs. line (A_{MIN} ref) to 13.5dB ATTN	**INL_1**		***0.20***	***0.60***	dB
Integral ATTN Error	Error vs. line (A_{MIN} ref) to 31.5dB ATTN	**INL_2**		0.47	0.75	dB
Input IP3	D[5:0] = [000000] = A_{MIN} D[5:0] = [011111] = $A_{15.5}$ D[5:0] = [111111] = A_{MAX} ▪ P_{IN} = +10 dBm per tone ▪ 50 MHz Tone Separation	**$IP3I_1$** **$IP3I_2$** **$IP3I_3$**	+57[2] +53 +53	+66 +60 +60		dBm
0.1 dB Compression *Please note ABS MAX P_{IN} on Page 2*	▪ D[5:0] = [000101] = $A_{2.5}$ ▪ Baseline P_{IN} = 20dBm	**$P_{0.1}$**		28.5		dBm
Settling Time (parallel mode)	▪ Start LE rising edge > V_{IH} ▪ End +/-0.10dB Pout settling ▪ 15.5 – 16.0 transition	**T_{LSB}**		400		ns
Serial Clock Speed	SPI 3 wire bus	**F_{CLK}**		***10***	***50***	MHz
Serial Setup Time	From rising edge of Vmode to rising edge of CLK for D5	**A**	***20***			ns
Clock width	Clock high pulse width	**B**	***10***			ns
LE setup time	From rising edge of CLK pulse for D0 to LE rising edge	**C**	***10***			ns
LE pulse	LE minimum pulse width	**D**	***30***			ns

SPECIFICATION NOTES:

1 – Items in min/max columns in ***bold italics*** are confirmed by Test.
2 – All other Items in min/max columns are confirmed by Design Characterization.

SERIAL CONTROL

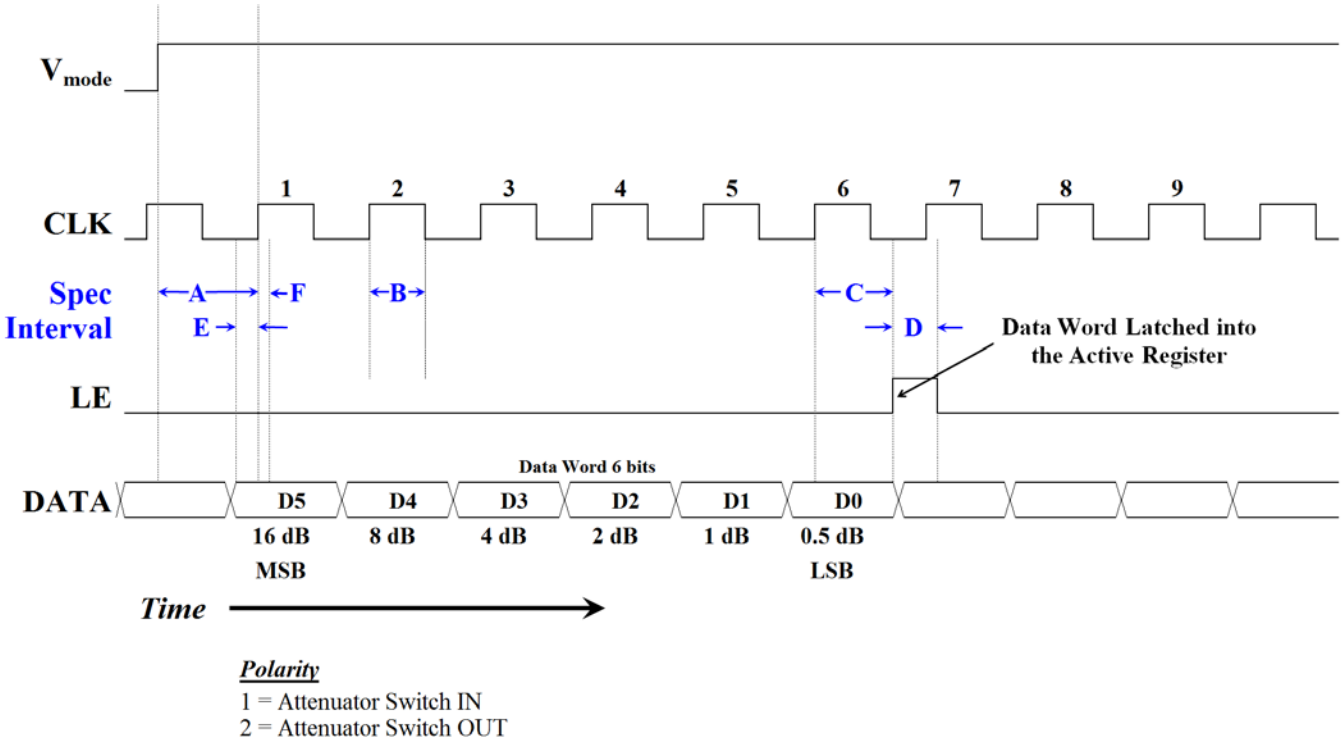
Serial mode is selected when V_{MODE} is pulled high (> V_{IH}), In serial mode the F1953 attenuation setting is programmed via the 3 wire bus (LE, CLK, DATA). In serial mode data is clocked in MSB first. Note the timing diagram below.

Note – *The F1953 includes a CLK inhibit feature designed to minimize sensitivity to CLK bus noise when the device is not being programmed. When Latch enable is high (> V_{IH}), the CLK input is disabled and DATA will not be clocked into the shift register. It is recommended that LE be pulled high (> V_{IH}) when the device is not being programmed.*

SERIAL REGISTER DEFAULT CONDITION

If the device is powered up in Serial Mode, the device will default to whatever attenuation state is defined by the six parallel data input pins D5,D4,D3,D2,D1,D0 thus allowing *any attenuation setting* to be specified as the power up state.

SERIAL REGISTER TIMING DIAGRAM: (Note the Timing Spec Intervals in **Blue**)



SERIAL REGISTER TIMING TABLE

Interval Symbol	Description	Min Spec	Max Spec	Units
A	From rising edge of Vmode to rising edge of CLK for D5	***20***		ns
B	Clock high pulse width	***10***		ns
C	From rising edge of CLK pulse for D0 to LE rising edge	***10***		ns
D	LE minimum pulse width	***30***		ns
E	Serial data set-up time before clock rising edge	***10***		ns
F	Serial data hold time after clock rising edge	***10***		ns

PARALLEL CONTROL MODE

The user has the option of running in one of two parallel modes: *Direct Parallel Mode* or *Latched Parallel Mode.*

DIRECT-PARALLEL MODE:

Direct-parallel mode is selected when V_{MODE} (pin 13) is < V_{IL} and LE (pin 5) is > V_{IH}. In this mode the device will immediately react to any voltage changes to the parallel control pins [pins 1, 15, 16, 17, 19, 20]. Use direct-parallel mode for the fastest settling time.

LATCHED-PARALLEL MODE:

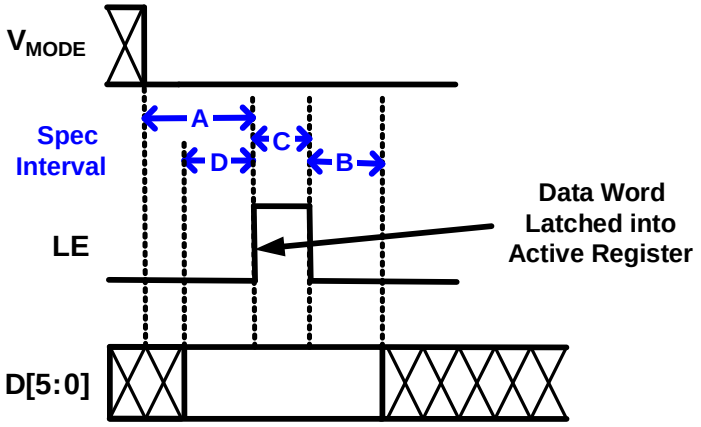
Latched-parallel mode is selected when V_{MODE} (pin 13) is < V_{IL} and LE (pin 5) is toggled from < V_{IL} to > V_{IH}

To utilize latched-parallel mode:

- Set LE < V_{IL}
- Adjust pins [1, 15, 16, 17, 19, 20] to the desired attenuation setting. (Note the device will not react to these pins while LE < V_{IL}.)
- Pull LE > V_{IH}. The device will then transition to the attenuation settings reflected by these pins.

When the device is powered up In Latched Parallel Mode [V_{MODE} < V_{IL} and LE > V_{IH}] the attenuation setting defaults to the state defined by the six parallel data pins [pins 1, 15, 16, 17, 19, 20]

LATCHED PARALLEL MODE TIMING DIAGRAM: (Note the Timing Spec Intervals in **Blue**)

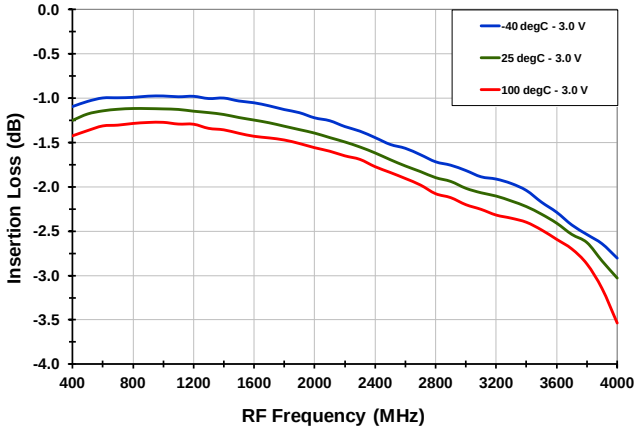


LATCHED PARALLEL MODE TIMING TABLE:

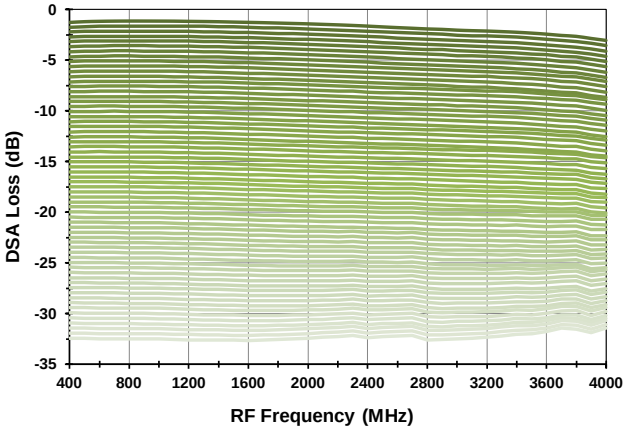
Interval Symbol	Description	Min Spec	Max Spec	Units
A	Serial to Parallel Mode Setup Time	100		ns
B	Parallel Data Hold Time	10		ns
C	LE minimum pulse width	10		ns
D	Parallel Data Setup Time	10		ns

TYPICAL OPERATING PARAMETRIC CURVES (EVKit loss de-embedded, 3.0V unless otherwise noted)

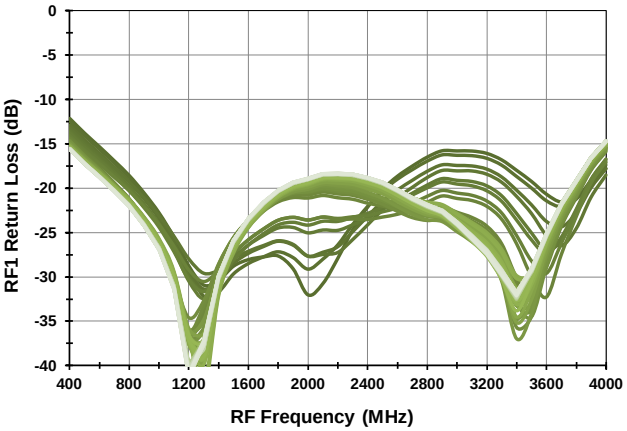
Insertion Loss vs. Frequency [AMIN]



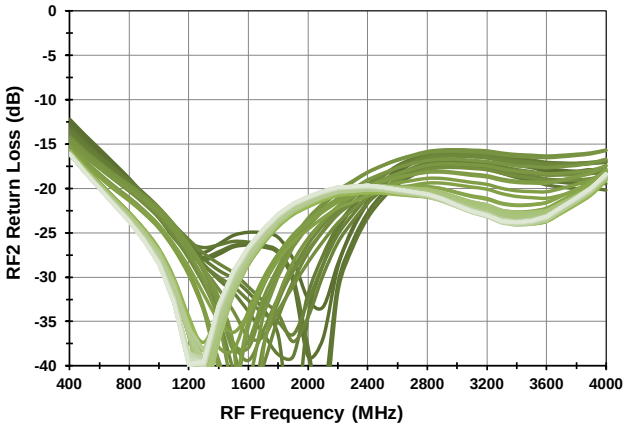
Attenuation vs. Freq [TCASE = +25C, 0.5 dB steps]



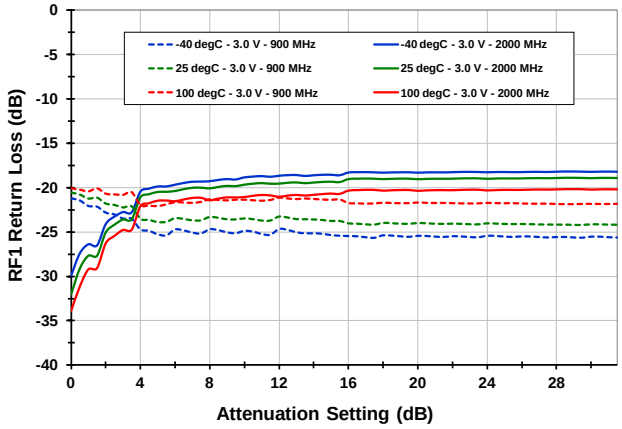
S11 vs. Frequency [TCASE = +25C, 0.5 dB steps]



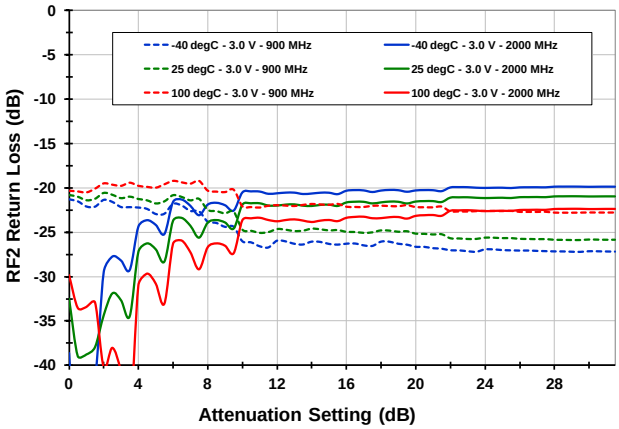
S22 vs. Frequency [TCASE = +25C, 0.5 dB steps]



S11 vs. Attenuation State

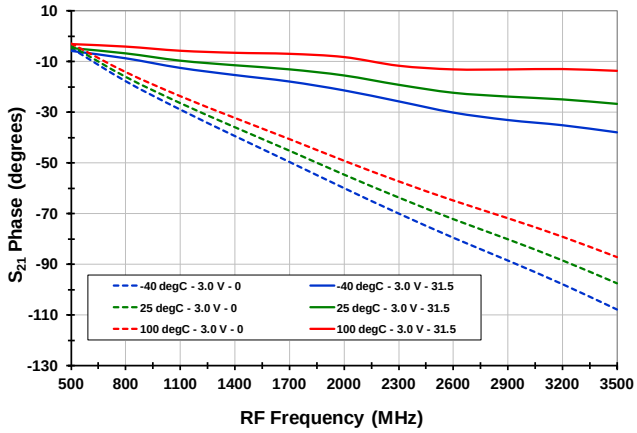


S22 vs. Attenuation State

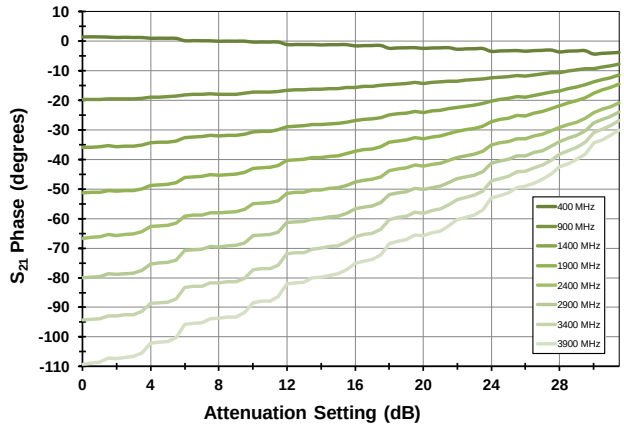


TOCS CONTINUED (-2-)

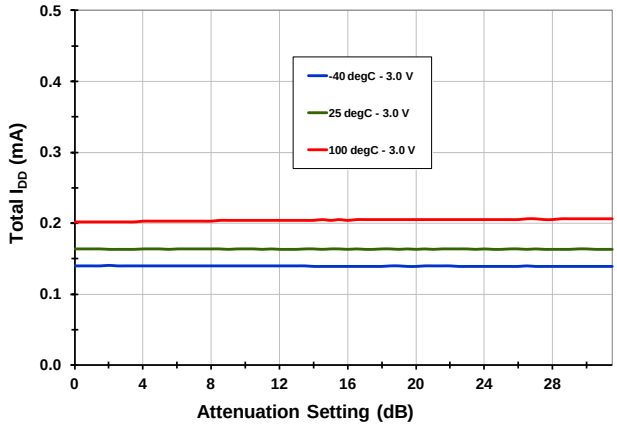
Phase vs. Frequency



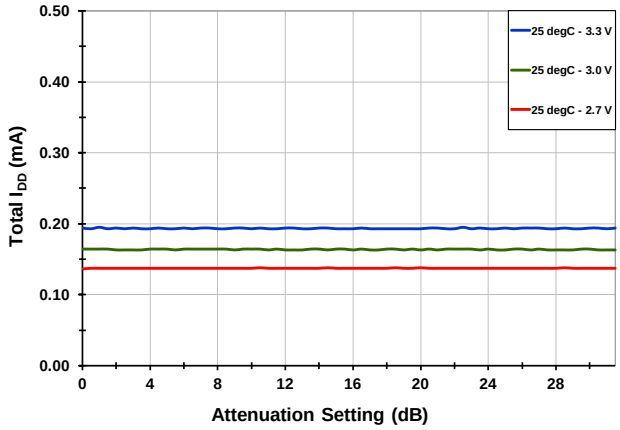
Phase vs. Attenuation Setting



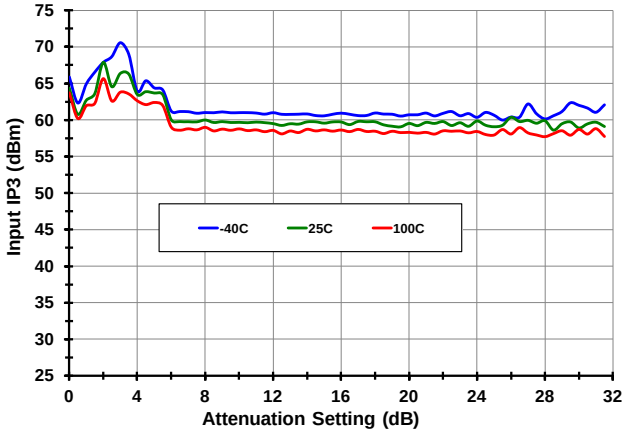
Supply Current I_{DD} [vs. Temp]



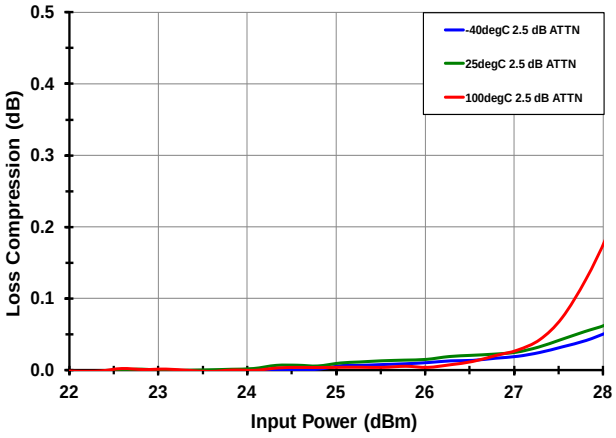
Supply Current I_{DD} [vs. V_{DD}]



Input IP3 [f_{RF} = 1900 MHz, V_{DD} = 3.0 V]

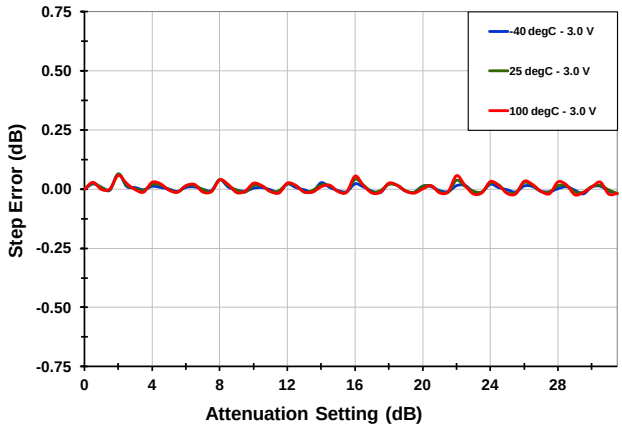


Compression [f_{RF} = 2000 MHz, ATTN = 2.5 dB]

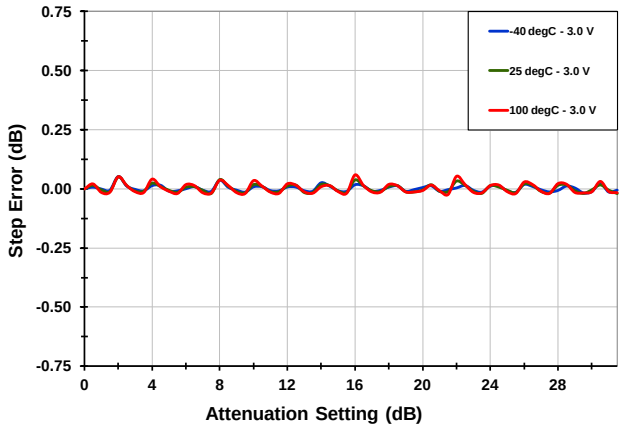


TOCs CONTINUED (-3-)

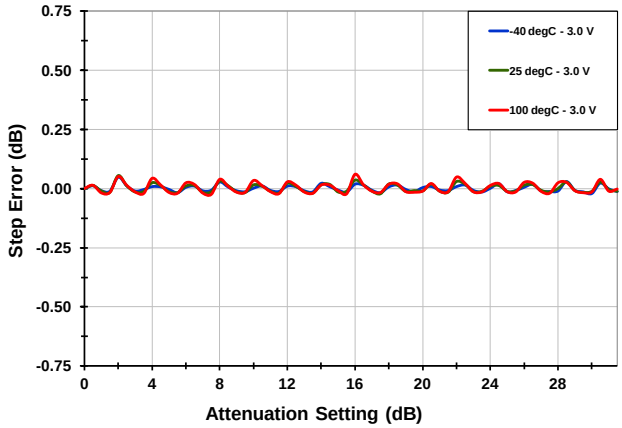
DNL [400 MHz]



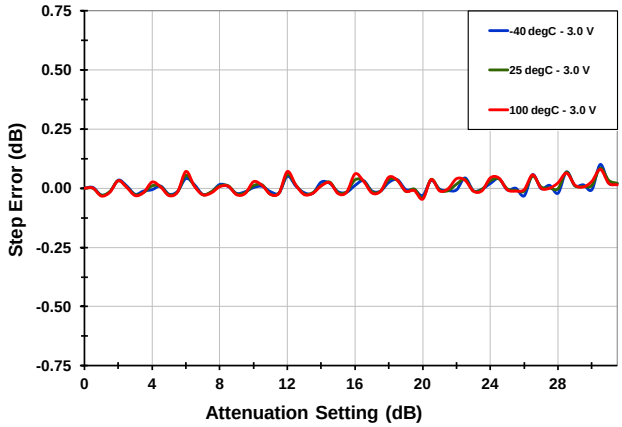
DNL [700 MHz]



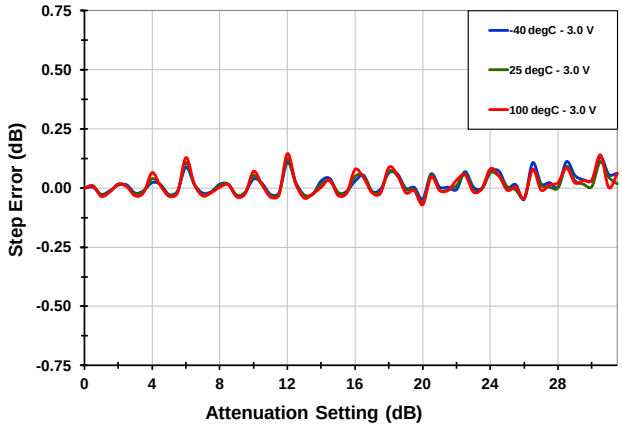
DNL [900 MHz]



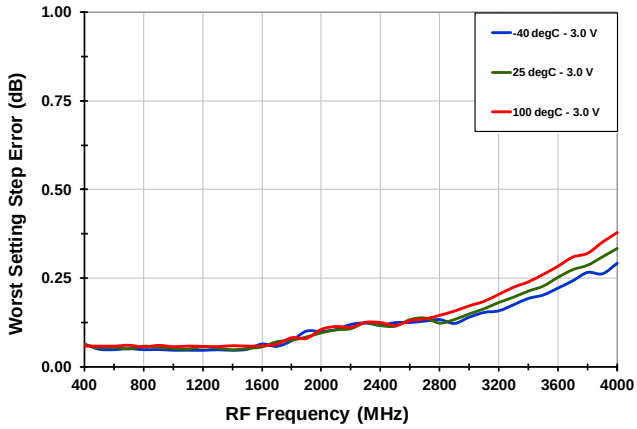
DNL [1900 MHz]



DNL [2800 MHz]

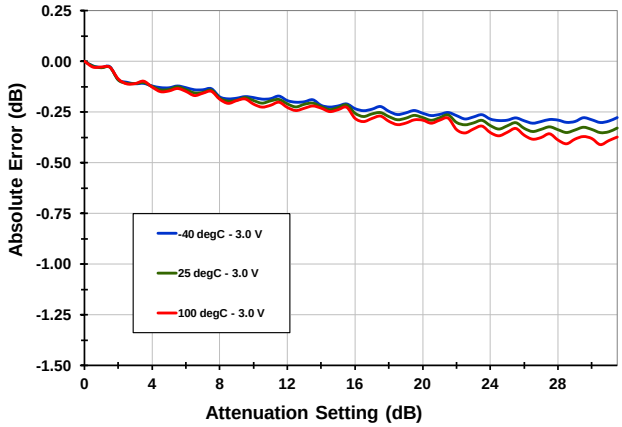


Worst Setting DNL

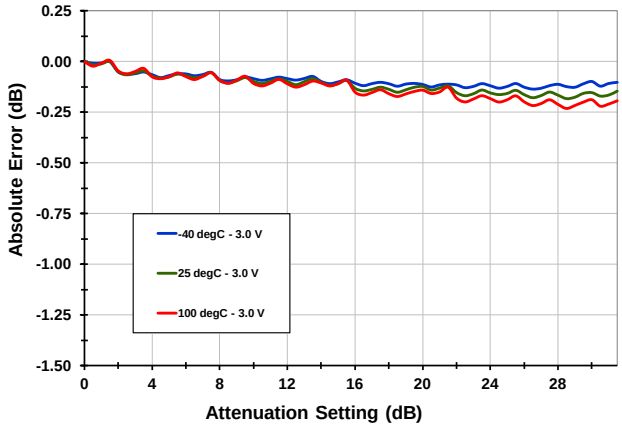


TOCs CONTINUED (-4-)

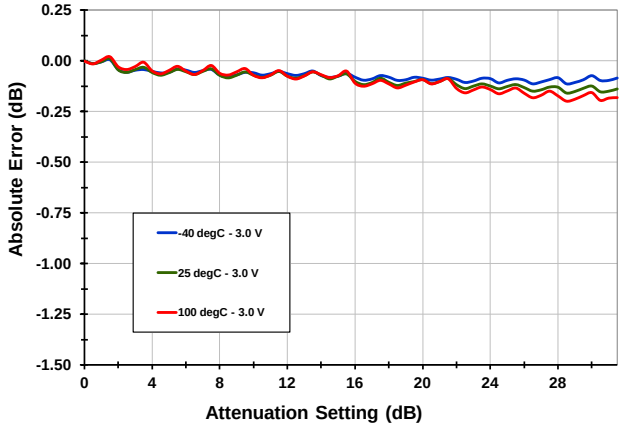
INL [400 MHz]



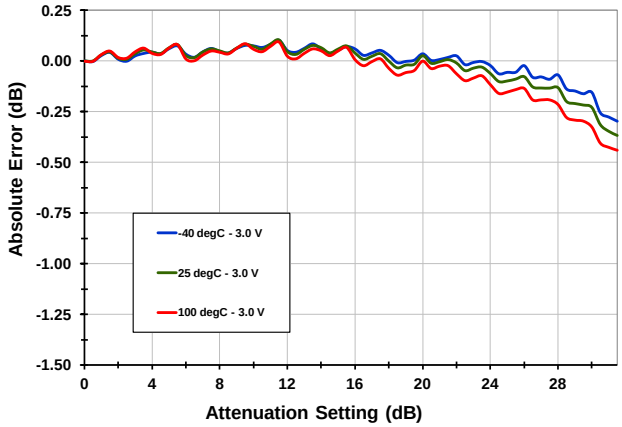
INL [700 MHz]



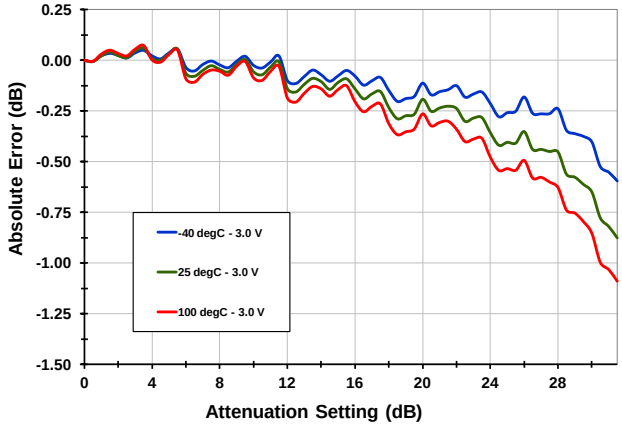
INL [900 MHz]



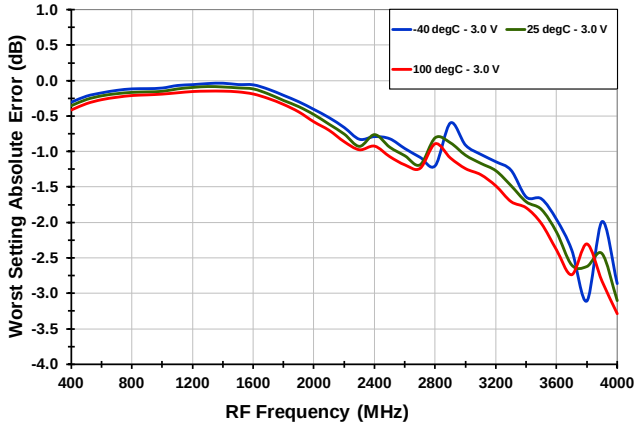
INL [1900 MHz]



INL [2900 MHz]

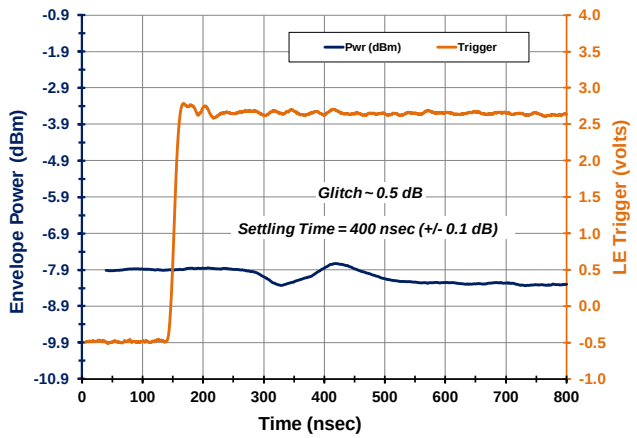


Worst Setting INL

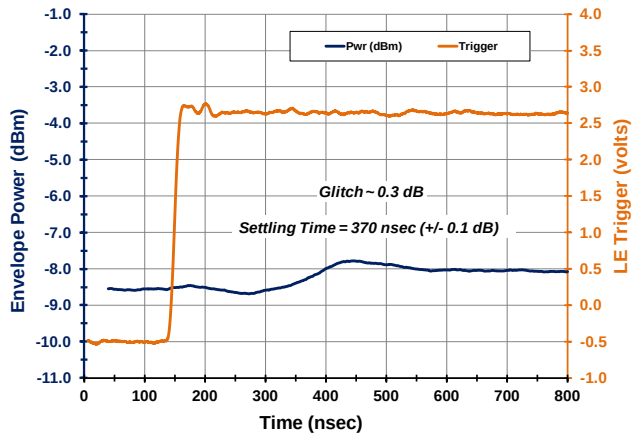


TOCs CONTINUED (-5-) [f_{RF} = 900 MHz]

Transient [15.5 to 16.0 (MSB+) 3.3V *F1953*]



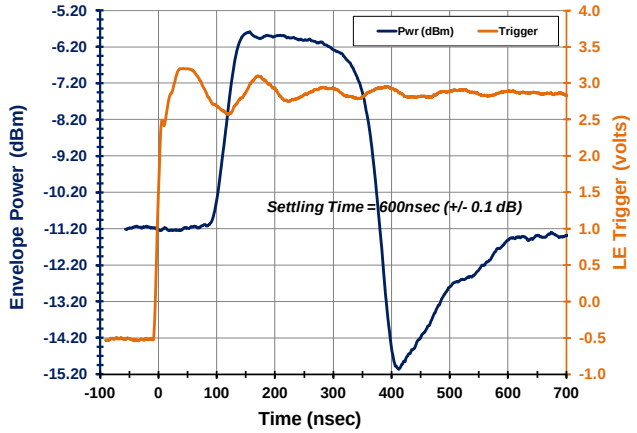
Transient [16.0 to 15.5 (MSB-) 5.0V *F1953*]



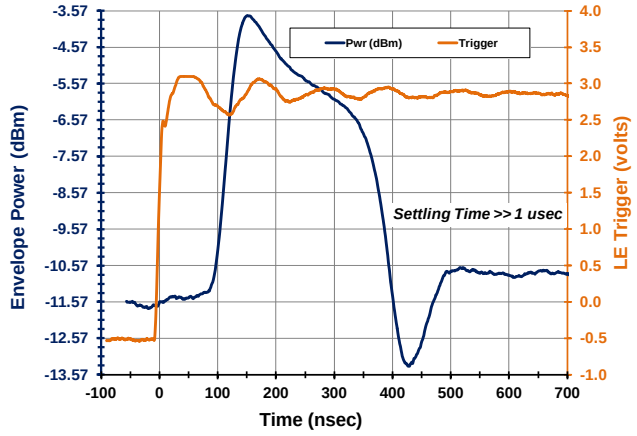
The graphs ***ABOVE*** show the transient overshoot and settling time performance for both the MSB+ and MSB- cases for the F1953. The device settles very quickly (~400) ns with benign (~0.5) dB overshoot.

The graphs ***BELOW*** show the transient overshoot and settling time performance for a popular competing DSA. *Note the overshoot/undershoot excursion of almost 10 dB* and the very long settling time. For the MSB- case, the settling time is off the scale, ~ 3 µsec.

Transient [15.75 to 16.00 (MSB+) *Standard DSA*]



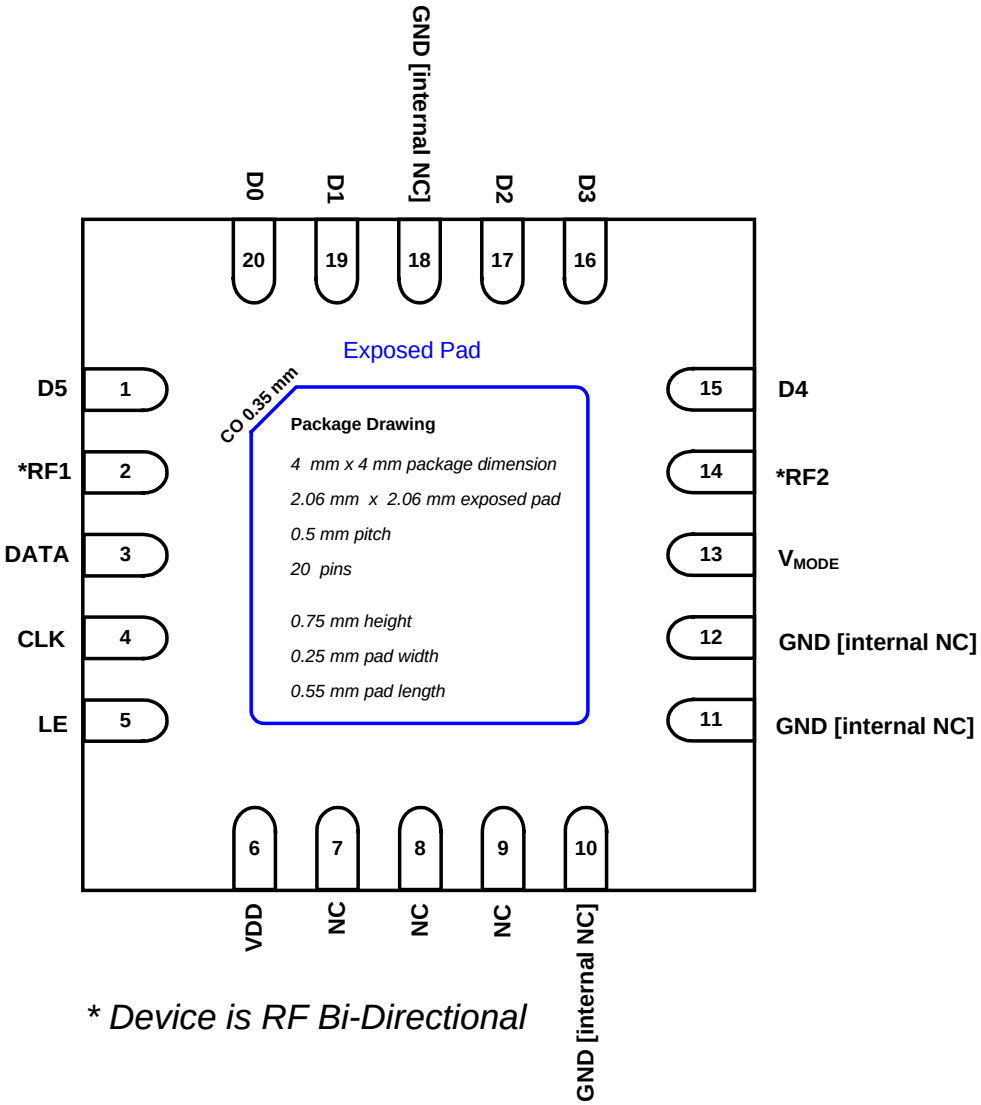
Transient [16.00 to 15.75 (MSB-) *Standard DSA*]



PIN DIAGRAM

TOP View

(looking through the top of the package)



** Device is RF Bi-Directional*

PACKAGE OUTLINE DRAWINGS

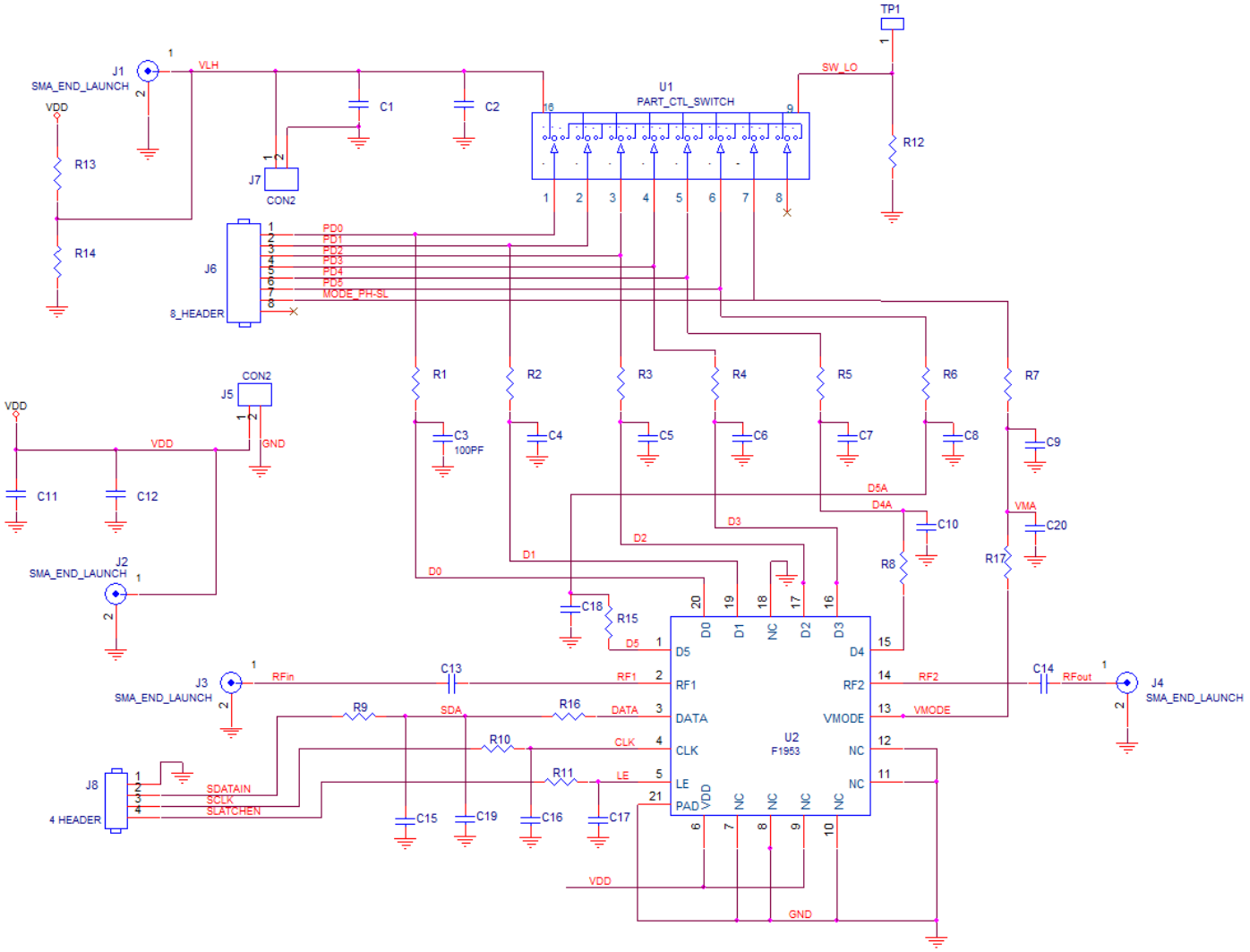
The package outline drawings for the 20-VFQFPN are located at the end of this document and are accessible from the Renesas website. The package information is the most current data available and is subject to change without revision of this document.

PIN DESCRIPTIONS

Pin #	Pin Name	Pin Function
1	D5	16dB Attenuation Control Bit. Pull high for 16dB ATTN.
2	RF1	Device RF input or output (bi-directional). Internally DC blocked.
3	DATA	Serial interface Data Input.
4	CLK	Serial interface Clock Input.
5	LE	Serial interface Latch Enable Input. Internal pull-up (100K ohm).
6	VDD	Power supply pin.
7	NC	No internal connection. These pins can be left unconnected, voltage applied, or connected to ground (recommended).
8	NC	No internal connection. These pins can be left unconnected, voltage applied, or connected to ground (recommended).
9	NC	No internal connection. These pins can be left unconnected, voltage applied, or connected to ground (recommended).
10	NC	No internal connection. These pins can be left unconnected, voltage applied, or connected to ground (recommended).
11	NC	No internal connection. These pins can be left unconnected, voltage applied, or connected to ground (recommended).
12	NC	No internal connection. These pins can be left unconnected, voltage applied, or connected to ground (recommended).
13	VMODE	Pull high for serial mode. Ground for Parallel control mode.
14	RF2	Device RF input or output (bi-directional). Internally DC blocked.
15	D4	8dB Attenuation Control Bit. Pull high for 8dB ATTN.
16	D3	4dB Attenuation Control Bit. Pull high for 4dB ATTN.
17	D2	2dB Attenuation Control Bit. Pull high for 2dB ATTN.
18	NC	No internal connection. These pins can be left unconnected, voltage applied, or connected to ground (recommended).
19	D1	1dB Attenuation Control Bit. Pull high for 1dB ATTN.
20	D0	0.5dB Attenuation Control Bit. Pull high for 0.5dB ATTN.
EP	Exposed Paddle	Connect to Ground with multiple vias for good thermal relief.

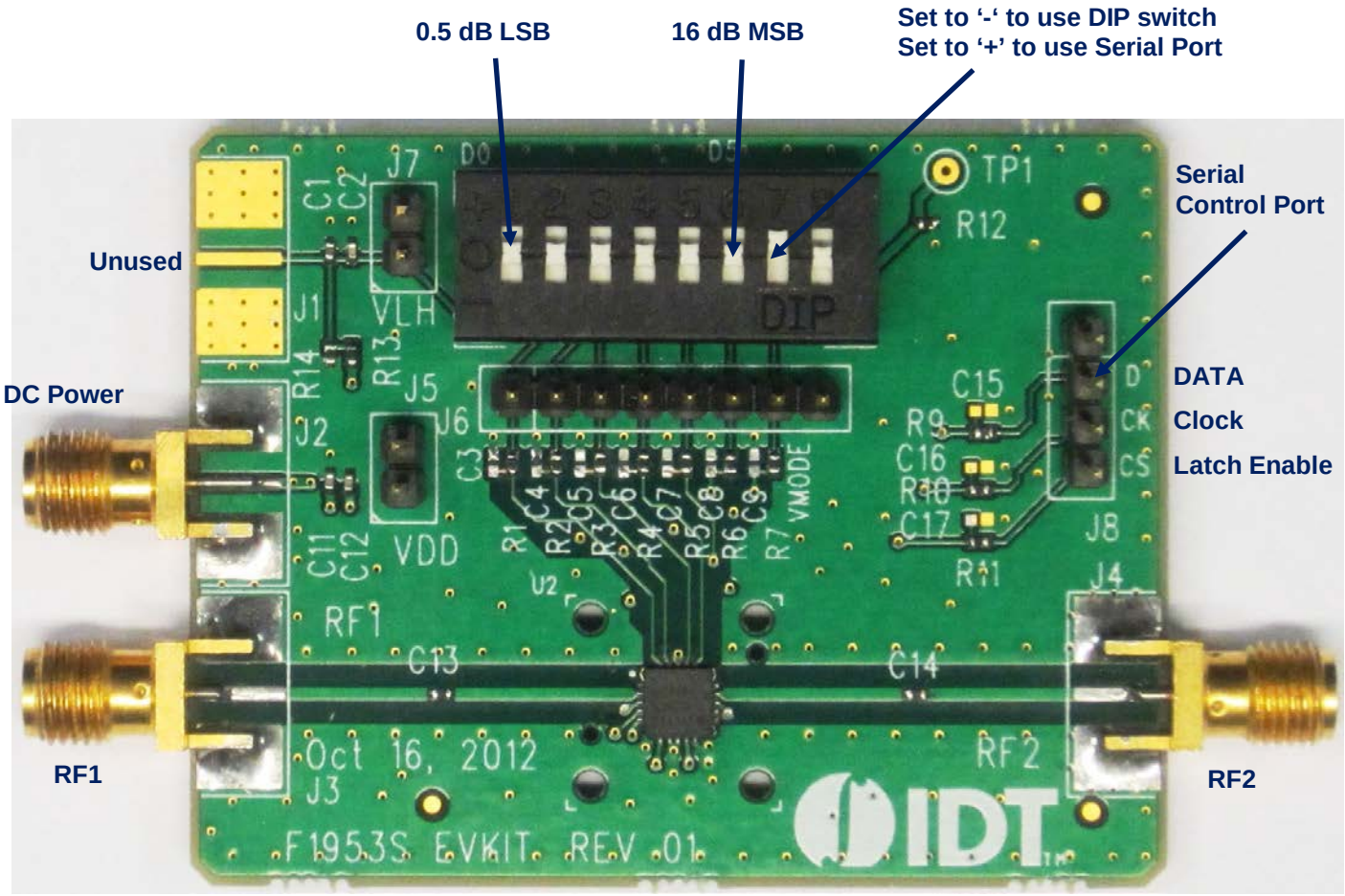
EVKIT SCHEMATIC

The diagram below describes the recommended applications / EVkit circuit:



EVKIT OPERATION

The picture and graphic below describe how to operate the EVkit.

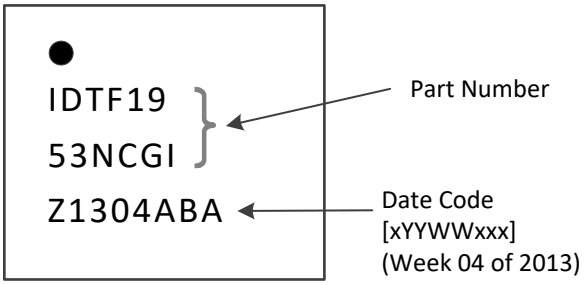


EVKIT BOM (F1953)

F1953 BOM Rev 01 PCB Rev 01 11/15/2012

Item #	Value	Size	Desc	Mfr. Part #	Mfr.	Part Reference	Qty
1	10nF	0402	CAP CER 10000PF 16V 10% X7R 0402	GRM155R71C103KA01D	MURATA	C2,12	2
2	0.1uF	0402	CAP CER 0.1UF 16V 10% X7R 0402	GRM155R71C104KA88D	MURATA	C1,11	2
3	Header 2 Pin	TH 2	CONN HEADER VERT SGL 2POS GOLD	961102-6404-AR	3M	J5,7	2
4	Header 4 Pin	TH 4	CONN HEADER VERT SGL 4POS GOLD	961104-6404-AR	3M	J8	1
5	Header 8 Pin	TH 8	CONN HEADER VERT SGL 8POS GOLD	961108-6404-AR	3M	J6	1
6	SMA_END_LAUNCH	.062	SMA_END_LAUNCH (Small)	142-0711-821	Emerson Johnson	J2,3,4	3
7	0	0402	RES 0.0 OHM 1/10W 0402 SMD	ERJ-2GE0R00X	Panasonic	R1-7,12,C13,C14	10
8	3K	0402	RES 3.00K OHM 1/10W 1% 0402 SMD	ERJ-2RKF3001X	Panasonic	R9-11	3
9	10K	0402	RES 10K OHM 1/10W 1% 0402 SMD	ERJ-2RKF1002X	Panasonic	R8,15-17	4
10	100K	0402	RES 100KOHM 1/10W 1% 0402 SMD	ERJ-2RKF104X	Panasonic	R13	1
11	267K	0402	RES 267K OHM 1/10W 1% 0402 SMD	ERJ-2RKF2673X	Panasonic	R14	1
12	DIPSwitch	TH 10	8 POSITION DIP SWITCH	KAT1108E	E-Switch	U1	1
13	Digital Step Attenuator		F1953Z	F1953Z	IDT	U2	1
14	PCB		PCB Rev 01	F1953S Evkit Rev 01	SBC		1
15	100pF	0402	CAP CER 100PF 16V 10% X7R 0402	GRM155R71C103KA01D	MURATA	C3-10,15-20	**DNP**
16	SMA_END_LAUNCH	.062	SMA_END_LAUNCH (Small)	142-0711-821	Emerson Johnson	J1	**DNP**
						Total	**33**

TOP MARKINGS



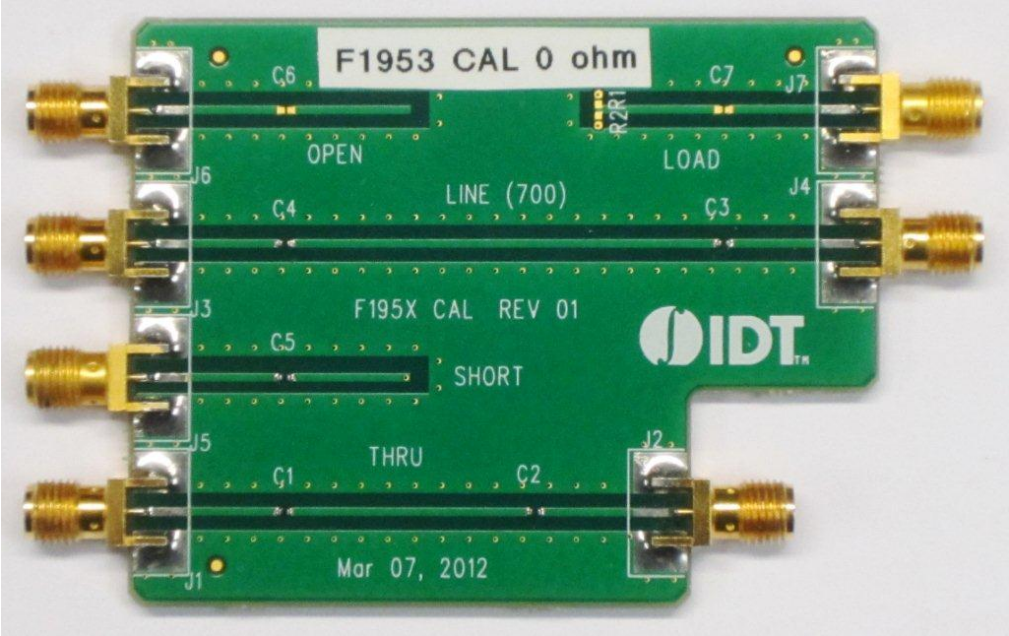
EVKIT THROUGH-REFLECT-LINE (TRL) CALIBRATION

The “Through-Reflect-Line” (TRL) method [1] is used to de-embed the evaluation board losses from the S-parameter measurements of the F1953. This method requires the use of three standards: a through, a reflection, and a line. The TRL method has the advantage over other calibration methods in that it requires only one of these three standards to be well defined.

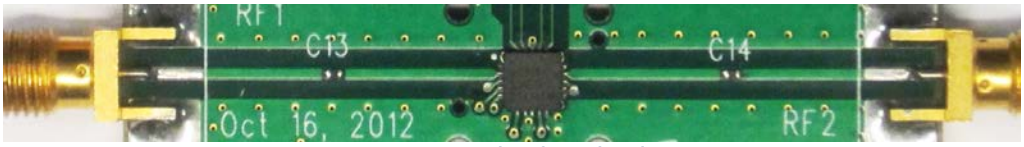
The TRL through which is used for the F1953 TRL calibration was constructed identically to the evaluation board, minus the DUT and its corresponding length. Therefore, the through corresponds to a precise zero length connection between the input and output reference planes of the DUT. This through satisfies the requirement of the TRL method that one of the three standards be precisely specified.

The TRL reflection standard used is constructed identically to the input and output lines of the evaluation board, with a short placed at the reference plane of the DUT. In accordance with the TRL method’s requirements, the actual magnitude and phase were not accurately specified, but the phase was known to within 90 degrees and the TRL reflection standard has a magnitude close to one.

The TRL line standard is identical to the TRL through, but with an additional length of 0.8 inches (2cm). This satisfies the TRL method’s requirement that the TRL be a different length than the TRL through, that it have the same impedance and propagation constant as the through, and that the phase difference between the through and the line be between 20 degrees and 160 degrees. The difference in length yields a phase difference of approximately 20 degrees at 500MHz, and a phase difference of 160 degrees at 4GHz.



Standards used for F195x TRL calibration



F1953 evaluation circuit

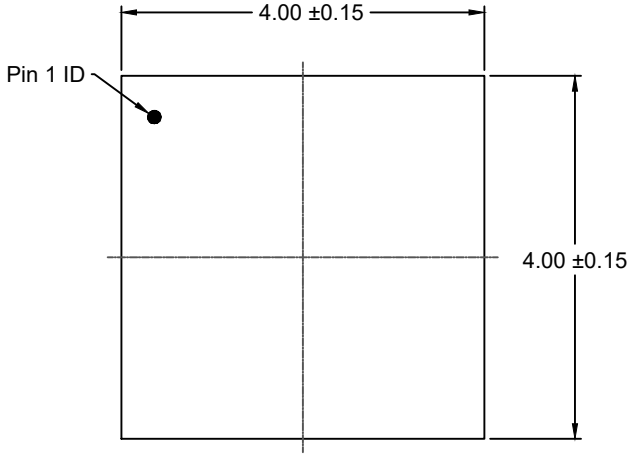
Engen, G.F.; Hoer, C.A.; “Thru-Reflect-Line: An Improved Technique for Calibrating the Dual Six-Port Automatic Network Analyzer,” **IEEE Transactions on Microwave Theory and Techniques**, Volume: 27 Issue:12, pp. 987 – 993, Dec 1979.

Revision History

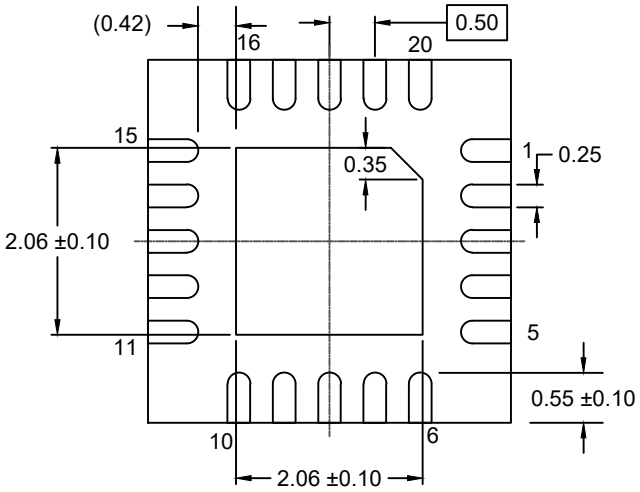
Revision Date	Description
February 9, 2022	Rebranded to Renesas.
September 5, 2018	▪ Updated document template. ▪ Updated Package Outline Drawings section. Now references the latest official drawing. No changes to dimensions. ▪ Added disclaimer paragraph.
December 3, 2015	▪ Corrected logic voltage. ▪ Add recommended operating conditions table. ▪ Updated serial timing figure. ▪ Updated pin description table. ▪ Updated evaluation board schematic.
April 10, 2014	▪ Correct top marking drawing.
March 30, 2013	▪ Initial release.

Package Outline Drawing

PSC-4445-01
NCG20P1
20-VFQFPN 4.0 x 4.0 x 0.75 mm Body, 0.5mm Pitch
Rev.03, May 28, 2025

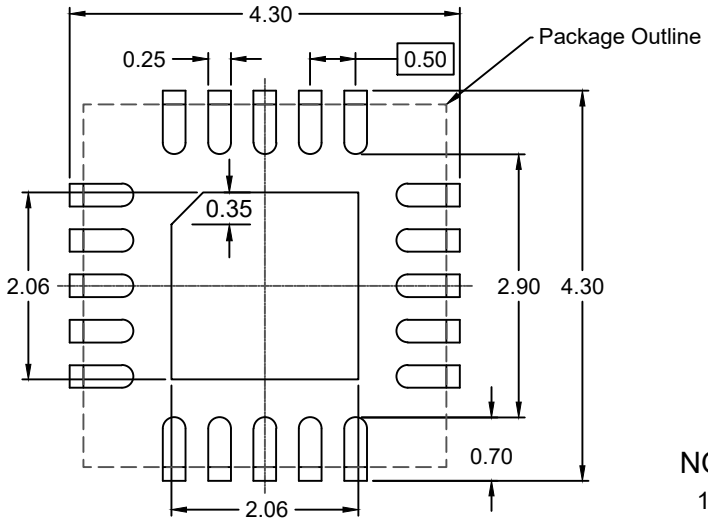


TOP VIEW



BOTTOM VIEW

SIDE VIEW



RECOMMENDED LAND PATTERN
(PCB Top View, NSMD Design)

NOTES:

1. JEDEC compatible
2. All dimensions are in mm and angles are in degrees
3. Use ±0.05 mm for the non-toleranced dimensions
4. Numbers in ( ) are for reference only

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