RAA271041

Cold Crank Boost and Buck Controller with Drivers for ASIL-D Automotive Applications

The RAA271041 is a controller for a dual regulator system capable of supporting ASIL-D automotive systems that must operate during battery dropout conditions. The Channel 2 Boost regulator maintains the voltage rail supplying the downstream Channel 1 Buck regulator, allowing the Buck output to maintain regulation during a battery dropout event such as cold cranking.

For cold crank applications, the Channel 2 Boost has an adjustable output and is active when the V_{BAT} input voltage falls below a user-programmable threshold. If the V_{BAT} input is above the user-programmed threshold, the Boost controller offers a Boost Bypass mode in which the high-side MOSFET of the Boost channel is held on and the V_{BAT} input voltage is passed directly to the Boost output. The Boost channel can also be configured as a standalone Boost, which is always on.

The Boost output from Channel 2 supplies the input for Channel 1 buck. The Buck can be configured either as fixed 5V or fixed 3.3V output or as an adjustable output from 0.8V to 12V using a resistor divider from VOUT1 to FB1 to ground.

The RAA271041 requires a minimum input voltage of 6V for start-up. The Channel 2 Boost has an input range from 2.2V to 42V, while the Channel 1 Buck has an input range from 3.5V to 42V.

The RAA271041 Buck channel can operate in Energy Conservation Mode (ECM) to provide a low I_Q mode by reducing quiescent current draw to 6µA (typical) when no external load is applied. The Buck and Boost switching frequencies are factory programmed to 400kHz or 2.2MHz. Optional spread spectrum operation allows for a reduction of EMI and noise levels.

Features

- ASIL-D Functional Safety
- 40V Boost and Buck integrated driver controller
- FET drivers support source/sink current of 2A/3A
- Low I_Q with ECM mode of 6µA typical
- Separate Wake (Enable) inputs for each channel
- Minimized FET ON and OFF times (20ns and 50ns)
- Optional pseudo-random spread spectrum clocking
- Buck frequency options 400kHz or 2.2MHz
- Boost frequency options 400kHz or 2.2MHz (2.2MHz requires Buck frequency at 2.2MHz)
- VBATS sense for boost enable during cold crank
- Boost Bypass mode (with buck in CCM)
- External synchronization via SYNC pin
- Dual over-temperature protection monitors
- 6x6mm 36Ld SC-QFN package
- AEC-Q100 grade 1 qualified

Functional Safety Features

- Built-In Self Test (BIST) at power up
- Recurring checks: internal references, PWM clock, system clock, PGND/AGND connection, dual over-temperature monitor, ECM exit delay, VCC supply.
- Independent references and feedback sense paths for Buck and Boost OV/UV detection
- Independent fault indicators for Buck and Boost
- Fail-safe output, logic high indicates a trusted device state with all safety monitors active.

Applications

- Automotive battery supplied applications
- In cabin systems
- ADAS: Advanced Driver Assist Systems
- Start-stop protected systems (such as head unit, cluster, e-Mirror)

Contents

1. Overview

1.1 Typical Application Schematic

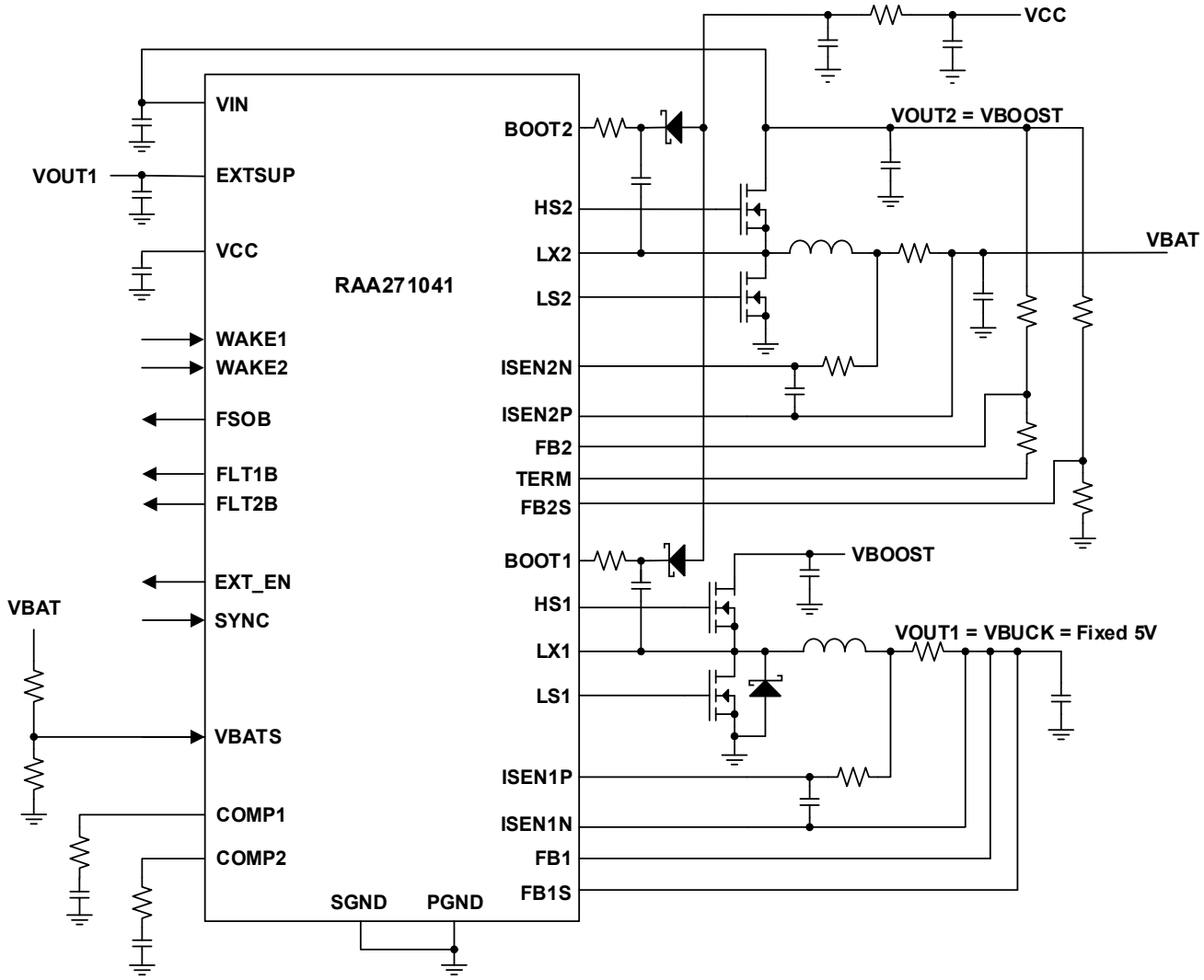


Figure 1. Typical Cold Crank Applications Schematic (Channel 1 Fixed at 5V)

1.2 Block Diagram

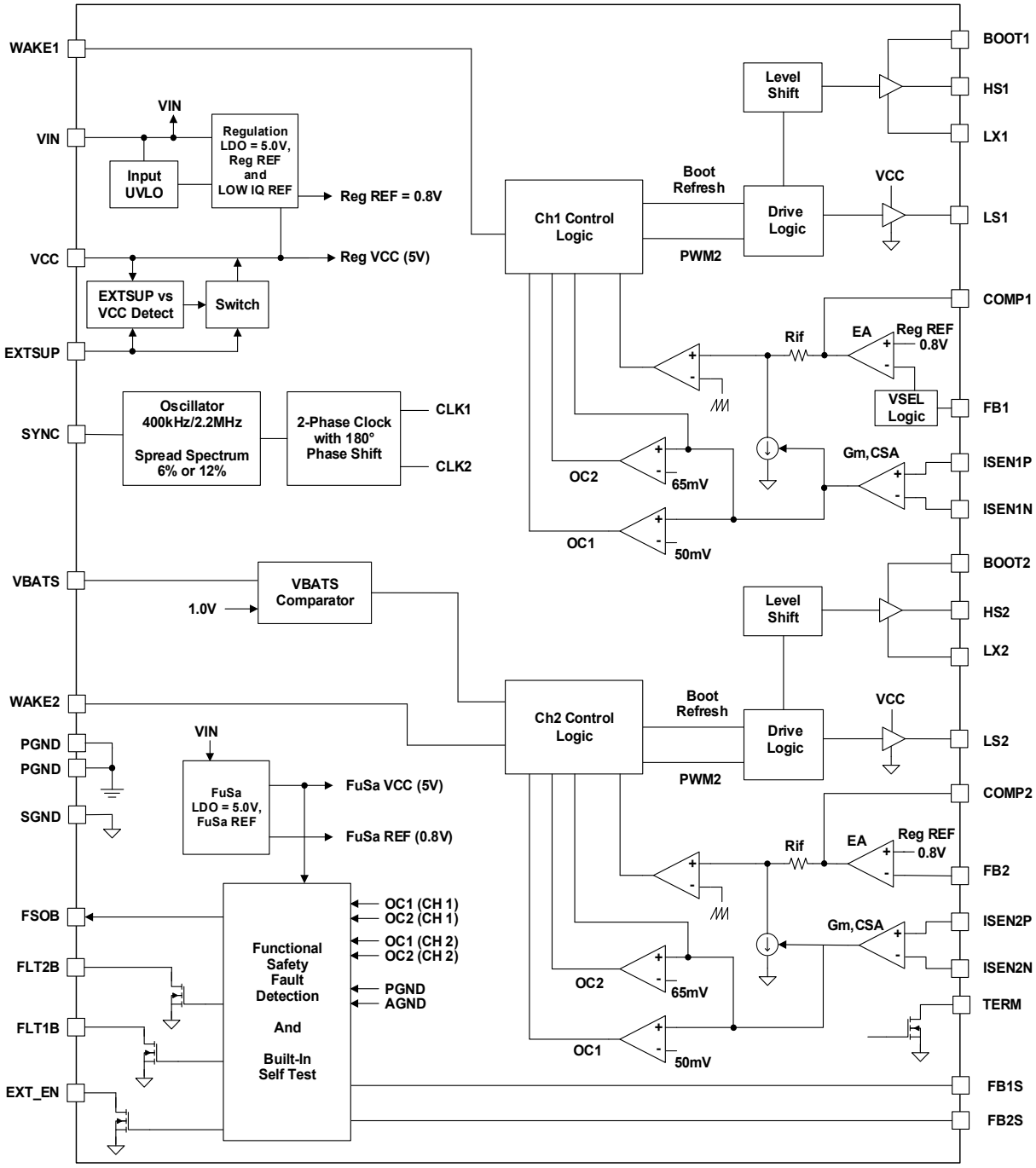
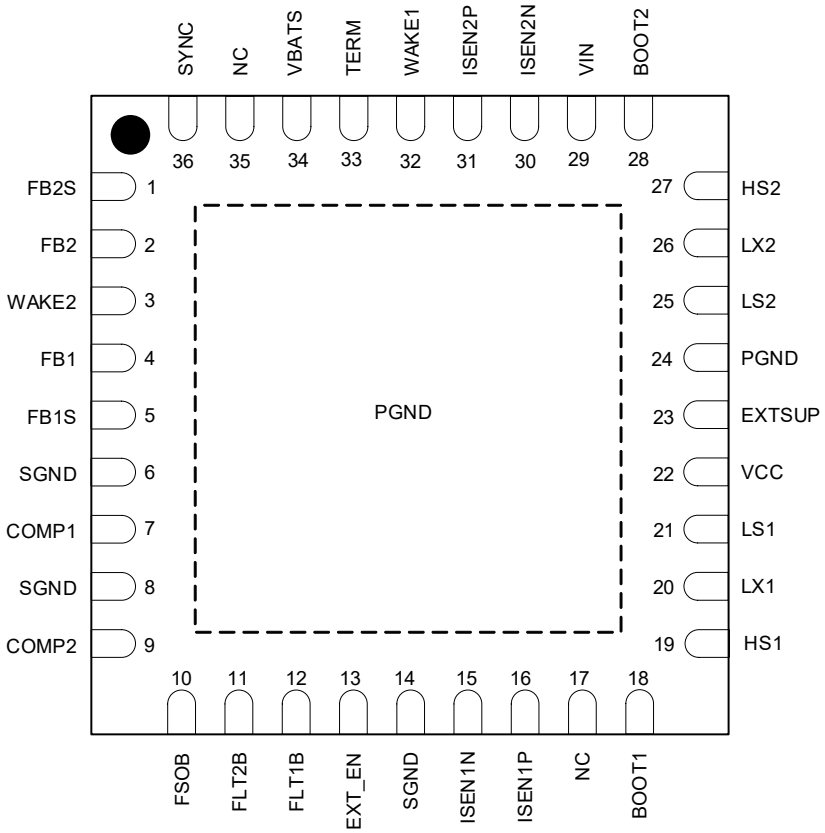


Figure 2. Block Diagram

2. Pin Information

2.1 Pin Assignments



Top View

2.2 Pin Descriptions

Pin Number	Pin Names	Description
1	FB2S	Fault detection sense input for Channel 2 Boost regulator. Connect to a resistor divider from Channel 2 Boost output to the TERM pin. For ASIL protection, this resistor divider must be a separate copy of the divider used for the FB2 pin.
2	FB2	Regulation feedback pin for Channel 2 adjustable-output Boost regulator. Connect to a resistor divider from Channel 2 Boost output to the TERM pin. FB2 is regulated to 0.8V.
3	WAKE2	Enable input for both channels for Enable Fuse option 1. Enable input for Channel 2 only for Enable Fuse option 2. Logic high activates the enable.
4	FB1	Regulation feedback pin for Channel 1 Buck regulator. For fixed output voltages of 5.0V or 3.3V, this pin connects directly to the output of Channel 1 buck. For adjustable output, this pin connects to a resistive divider from Channel 1 output to ground, and the FB1 voltage is regulated to 0.8V.
5	FB1S	Fault detection feedback pin for Channel 1 Buck regulator. For fixed output voltages of 5.0V or 3.3V, this pin connects directly to the output of Channel 1 Buck. For adjustable output, this pin connects to a resistive divider from Channel 1 output to ground. For ASIL protection, this resistor divider must be a separate copy of the divider used for the FB1 pin.
6	SGND	SGND for customer use; IC for internal use.
7	COMP1	Loop compensation pin for Channel 1 with a resistor/capacitor network connected to ground, to provide control loop compensation for Channel 1 Buck regulator.

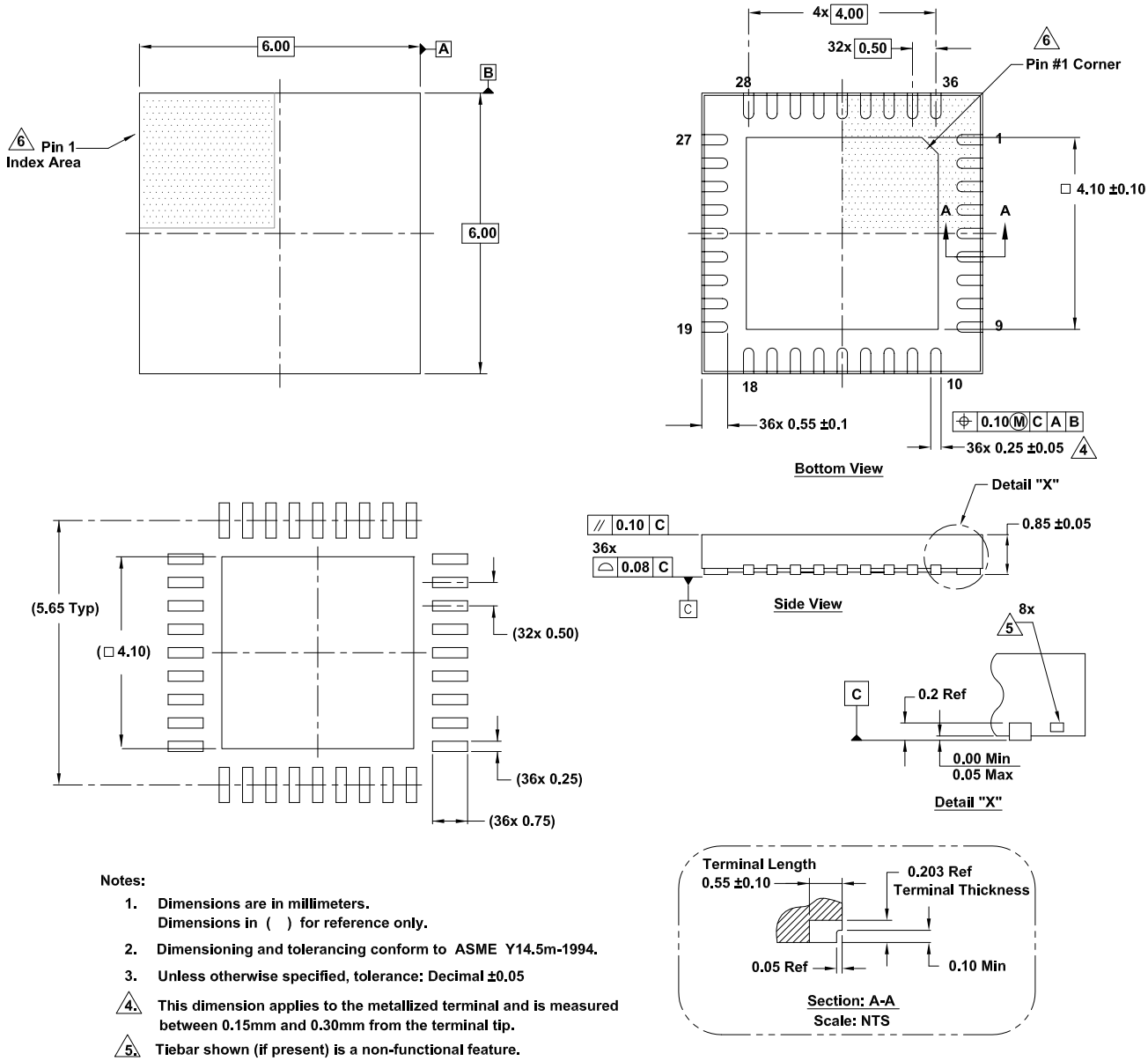
Pin Number	Pin Names	Description
8	SGND	SGND for customer use; IC for internal use.
9	COMP2	Loop compensation pin for Channel 2 with a resistor/capacitor network connected to ground. Provides control loop compensation for Channel 2 Boost regulator.
10	FSOB	Fail-Safe Output (Indicator). Asserted high indicates the device is in a Trusted State and all safety monitors are active.
11	FLTB2	Open-drain Fault Indicator for Channel 2 (Boost). Output low state indicates a Channel 2 fault.
12	FLTB1	Open-drain Fault indicator for Channel 1 (Buck). Output low state indicates a Channel 1 fault.
13	EXT_EN	Open-drain indicator for Channel 1. Open state indicates that Channel 1 buck is enabled and is operating in regulation.
14	SGND	Analog GND for the IC. Connect to the PGND pin and device PAD using PCB copper on the same layer as the device.
15	ISEN1N	Negative input to Channel 1 Buck output current sense. Connect to the output voltage of Channel 1.
16	ISEN1P	Positive input to Channel 1 Buck output current sense. Connect through an R-C filter to the positive (inductor) side of the Channel 1 output current-sense resistor.
17	NC	Leave this pin unconnected to allow proper node clearance.
18	BOOT1	Floating supply voltage for Channel 1 high-side MOSFET gate driver. Connect to a ceramic capacitor that connects from BOOT1 to LX1. The capacitor is charged through an external diode connected to VCC through an R-C filter.
19	HS1	Output of Channel 1 high-side MOSFET gate driver.
20	LX1	Channel 1 switch node and return path for the high-side MOSFET gate driver between BOOT1 and LX1.
21	LS1	Output of Channel 1 low-side MOSFET gate driver; switches between VCC and GND.
22	VCC	Bias supply (5V typical) for the IC and the MOSFET gate drivers. Decouple with a 10µF ceramic capacitor. This pin is supplied by the internal LDO during start-up. After initial start-up, the bias voltage can be supplied from either the buck 5V output or an external supply, using the automatic switchover feature of the EXTSUP pin.
23	EXTSUP	Input to the automatic switchover circuit for the VCC bias supply. EXTSUP accepts an external 5V supply derived from either a Channel 1 output of 5V or an independent 5V supply. External bias should not be applied to EXTSUP until VIN has exceeded the initial start-up voltage; however, a voltage such that EXTSUP - VIN $\leq$ 0.5V can be tolerated.
24	PGND	Connection point for power ground of the switching circuits for Channel 1 and Channel 2, and is the return path for the low-side MOSFET gate drivers.
25	LS2	Output of Channel 2 low-side MOSFET gate driver, switches between VCC and GND.
26	LX2	Channel 2 switch node, also is the return path for the high-side MOSFET gate driver between BOOT2 and LX2.
27	HS2	Output of Channel 2 high-side MOSFET gate driver.
28	BOOT2	Floating supply voltage for Channel 2 high-side MOSFET gate driver. Connect to a ceramic capacitor that connects from BOOT2 to LX2. The capacitor is charged through an external diode connected to VCC through an R-C filter.
29	VIN	Connected to the high voltage input supply for the buck regulators, and is normally supplied from the vehicle battery. This pin is decoupled using a 0.1µF or larger ceramic capacitor.
30	ISEN2N	Negative input to Channel 2 Boost input current sense. Connect through an R-C filter to the negative (inductor) side of the Channel 2 input current-sense resistor.
31	ISEN2P	Positive input to Channel 2 Boost input current sense. Connect to the positive side of the Channel 2 input current-sense resistor, typically connected to VBAT, which is the DC input voltage.
32	WAKE1	Enable input for Channel 1 Buck.
33	TERM	Open drain pull-down for the bottom side of the FB2 and FB2S resistor dividers. This pin becomes open (float) when the boost converter is disabled to eliminate power loss in the FB2 and FB2S resistor dividers.

Pin Number	Pin Names	Description
34	VBATS	VBAT sense input sets the boost turn-on threshold for when the battery input falls below normal, such as during Cold Crank. Connect to a resistor divider to set the voltage threshold, which enables the boost channel. VBATS threshold is 1.0V.
35	NC	No Connect.
36	SYNC	Synchronization input and operating mode control. Connect to VCC to force the part into Fixed frequency Continuous Conduction Mode (FCCM) operation using the internal oscillator. Connect to GND to allow the controller to automatically switch between FCCM, Diode Emulation Mode (DEM), or ECM mode, depending on load current. The pin can be switched during operation (VCC to GND, or GND to VCC) to change the operating mode. To synchronize switching to an external clock, connect to an external clock at 400kHz or 2.2MHz.
37	EPAD	Bottom pad. Connect to PGND and SGND under the IC. Connect to internal PCB GND layers using multiple vias.

3. Package Outline Drawing

For the most recent package outline drawing, see L36.6x6D.

L36.6x6D
36 Lead Step Cut Quad Flat No-Lead Plastic Package (SCQFN)
Rev 0, 12/20



Notes:

1. Dimensions are in millimeters.
   Dimensions in ( ) for reference only.
2. Dimensioning and tolerancing conform to ASME Y14.5m-1994.
3. Unless otherwise specified, tolerance: Decimal ±0.05
4. This dimension applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier is either a mold or mark feature.

4. Revision History

Revision	Date	Description
1.00	Sep 28, 2021	Initial release.

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