# RENESAS TECHNICAL UPDATE

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Renesas Electronics Corporation

<table>
<thead>
<tr>
<th></th>
<th></th>
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</tr>
</thead>
<tbody>
<tr>
<td><strong>Title</strong></td>
<td>RH850/C1M-A1, RH850/C1M-A2 User's Manual Hardware Rev.1.20 Errata</td>
<td>TN-RH8-B0246B/E</td>
<td>2.00</td>
<td></td>
</tr>
<tr>
<td><strong>Applicable Product</strong></td>
<td>RH850/C1M-A1, RH850/C1M-A2</td>
<td>Information Category</td>
<td>Technical Notification</td>
<td></td>
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<tr>
<td><strong>Lot No.</strong></td>
<td>-</td>
<td>Reference Document</td>
<td>Refer to the below</td>
<td></td>
</tr>
</tbody>
</table>

1. **Explanation**

This document is errata of RH850/C1M-A1, RH850/C1M-A2 User's Manual Hardware Rev.1.20.

No.1 to No.15 have already been notified on the previous edition of TN-RH8-B0246A/E.
No.16 to No.53 are additional items.

**[Reference Documents]**

<table>
<thead>
<tr>
<th>Series</th>
<th>Series</th>
<th>Series</th>
<th>Rev.</th>
<th>Document No</th>
</tr>
</thead>
<tbody>
<tr>
<td>No.</td>
<td>PDF page</td>
<td>Section</td>
<td>Chapter title (Chart title)</td>
<td>Error</td>
</tr>
<tr>
<td>-----</td>
<td>----------</td>
<td>---------</td>
<td>-----------------------------</td>
<td>-------</td>
</tr>
<tr>
<td>1</td>
<td>285</td>
<td>Interrupt</td>
<td>Figure 6.1 Example of External Interrupt Processing Flow</td>
<td><img src="image1.png" alt="Diagram" /></td>
</tr>
<tr>
<td>2</td>
<td>2531</td>
<td>ADCC</td>
<td>27.4.7.3 Wiring-Break Detection Self-Diagnosis Circuit Function</td>
<td><img src="image3.png" alt="Diagram" /></td>
</tr>
<tr>
<td>3</td>
<td>2537</td>
<td>ADCC</td>
<td>27.5.5 Procedure for Setting Wiring-Break Detection Self-Diagnosis</td>
<td><img src="image5.png" alt="Diagram" /></td>
</tr>
<tr>
<td>4</td>
<td>2538</td>
<td>ADCC</td>
<td>Figure 27.28 Flow of Wiring-Break Detection Self-Diagnostic Settings</td>
<td><img src="image7.png" alt="Diagram" /></td>
</tr>
<tr>
<td>5</td>
<td>2649</td>
<td>Functional Safety</td>
<td>Table 29.66 List of ECC Modules</td>
<td><img src="image9.png" alt="Diagram" /></td>
</tr>
</tbody>
</table>

The changes are shown below. Error: red, Correct: blue.

### Writing Error

#### Section 27.4.7.3 Wiring-Break Detection Self-Diagnosis Circuit Function
- **Original:** This is a function to detect a wiring break in a pin due to solder separation.
- **Change:** Discharge the target analog pin for the specified time in the wiring break detection control register (ADCCxxODCR register) and then perform A/D conversion. If the conversion result attenuates to approximately 0 V, you can determine that a wiring break is present.

#### Section 27.5.5 Procedure for Setting Wiring-Break Detection Self-Diagnosis
- **Original:** Wiring-breach detection is a facility for detecting wiring breaks in ANI. Both pull-down and pull-up methods are used for detection. In pull-down method, if a wiring break occurs, the result of the AD conversion is attenuated to approximately 0 V, which is detected as an abnormal value. Therefore, the user can judge that a wiring break has been detected. In pull-up method, if a wiring break occurs, the result of the AD conversion is boosted to approximately 5 V, which is detected as an abnormal value. Therefore, the user can judge that a wiring break has been detected.
- **Change:** Wiring break detection is a facility for detecting wiring breaks in ANI. In wiring break detection mode, a pull-down or pull-up resistor is connected for sampling of the sample-and-hold circuits when the width of pulse is fixed (18 states). In pull-down method, if a wiring break occurs, the result of the AD conversion is attenuated to approximately AVSS, which is detected as an abnormal value. Therefore, the user can judge that a wiring break has been detected. In pull-up method, if a wiring break occurs, the result of the AD conversion is boosted to approximately AVCC, which is detected as an abnormal value. Therefore, the user can judge that a wiring break has been detected.
### Functional Safety

28.3.3 Usage Notes

Reading a register with a value that is undefined after a reset without initializing the register may lead to a lock step compare error. Accordingly, such registers must be initialized with the desired settings.

Even if the branch instruction and the subsequent instruction is issued in parallel, the lock step compare error might be occurred by undefined register after the reset. It should be applied as specified below until the register which refer by subsequent instruction is initialized in case of branching in the preceding instruction.

- Insert the SYNCI instruction or the RIE instruction following the branch instruction.
- It has to be added by assembler language. When C language is used, it could be optimized.

Applicable branch instructions: Bcond except BR, JARL, JMP

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### Operating Mode

#### Table 5.1 Selection of Operating Mode

<table>
<thead>
<tr>
<th>Value Set in the Pin</th>
<th>Value Set in the Option Byte Register</th>
<th>Operating Mode</th>
<th>Startup Area</th>
<th>Type of FF*</th>
<th>Remark</th>
</tr>
</thead>
<tbody>
<tr>
<td>M0</td>
<td>D0</td>
<td>User boot mode</td>
<td>User area</td>
<td>User boot</td>
<td>User boot mode</td>
</tr>
<tr>
<td>M1</td>
<td>D1</td>
<td>User boot mode</td>
<td>User area</td>
<td>User boot</td>
<td>User boot mode</td>
</tr>
<tr>
<td>M2</td>
<td>X</td>
<td>Serial program mode</td>
<td>Boot area</td>
<td>Serial programming</td>
<td>Boot area</td>
</tr>
<tr>
<td>M3</td>
<td>X</td>
<td>Serial program mode</td>
<td>Boot area</td>
<td>Serial programming</td>
<td>Boot area</td>
</tr>
</tbody>
</table>

Note: X: Don’t use

Note 1: See Section 2.4.3, Pin Name for the functions and states of pins when each interface is selected.

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### On-Chip Debugging Unit (OCDR)

#### Table 34.2 I/O Pins of AUDR

<table>
<thead>
<tr>
<th>Pin Name</th>
<th>I/O</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>AUDR</td>
<td>I/O</td>
<td>Description</td>
</tr>
</tbody>
</table>

- AUDR reset input pin
- AUDR reset input pin
- When this pin is not connected, it is internally pulled-down.
## 34.4.4.3 Usage Notes on the AUDR Function

- Do not negate the `AUDSYNC` pin until one cycle of AUDCK has elapsed after a command is input to the AUDATA pin and the Ready flag has been returned.
- When initialized memory is accessed through the AUDIR, a bus error may occur due to ECC error detection.

### Additional Description

- Power supply

![Figure 34.3: Timings from power on to data transfer](image)

### Notice Situation

Set the `/DCUTRST` pin to the low level at power on, regardless of whether on-chip debugging is used.

### Additional Description

Set the `/DCUTRST` pin to the low level at power on, regardless of whether on-chip debugging is used.
### Table 39.30 AUD RAM Monitor Timing

<table>
<thead>
<tr>
<th>Error</th>
<th>Correct</th>
<th>Change reason</th>
<th>Notice situation</th>
<th>Note</th>
</tr>
</thead>
<tbody>
<tr>
<td>None</td>
<td>None</td>
<td>None</td>
<td>None</td>
<td>None</td>
</tr>
</tbody>
</table>

#### Table 39.3.12 AUD RAM Monitor

<table>
<thead>
<tr>
<th>Error</th>
<th>Correct</th>
<th>Change reason</th>
<th>Notice situation</th>
<th>Note</th>
</tr>
</thead>
<tbody>
<tr>
<td>None</td>
<td>None</td>
<td>None</td>
<td>None</td>
<td>None</td>
</tr>
</tbody>
</table>

#### Table 1.1 Overview of Products (2/2)

- Motor control
  - Enhanced motor control unit (EMCU): Number of units
  - Enhanced motor control unit (EMCU): SubCPU frequency

#### Table 2.64 Example Handling of Unused Pins (2/2)

<table>
<thead>
<tr>
<th>Error</th>
<th>Correct</th>
<th>Change reason</th>
<th>Notice situation</th>
<th>Note</th>
</tr>
</thead>
<tbody>
<tr>
<td>None</td>
<td>None</td>
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#### Table 1.51 Pins

<table>
<thead>
<tr>
<th>Error</th>
<th>Correct</th>
<th>Change reason</th>
<th>Notice situation</th>
<th>Note</th>
</tr>
</thead>
<tbody>
<tr>
<td>None</td>
<td>None</td>
<td>None</td>
<td>None</td>
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</table>
18. **CPU System**

**Table 3.1 Peripheral Group Configuration (1/4)**

<table>
<thead>
<tr>
<th>Address Offset</th>
<th>Size (byte)</th>
<th>Register Name</th>
<th>Symbol</th>
<th>Format 1</th>
<th>I</th>
<th>O</th>
<th>R</th>
<th>C</th>
<th>Value after Reset</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
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<td></td>
<td></td>
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</tr>
</tbody>
</table>

Note: 1. The value is 0000H, for CPU (CPU), EX60 (CPU), and EX80 (CPU).

19. **CPU**

**Table 3.63 PEG Register Base Address**

<table>
<thead>
<tr>
<th>Address Offset</th>
<th>Size (byte)</th>
<th>Register Name</th>
<th>Symbol</th>
<th>Format 1</th>
<th>I</th>
<th>O</th>
<th>R</th>
<th>C</th>
<th>Value after Reset</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
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<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Description

**TN-RH8-B0281A/E**

20. **RLIN3**

13.9.1. LIN Self-Test Mode

Regardless of the setting of the baud rate related registers, the baud rate operates at the LIN communication clock source/16 [bps].

**TN-RH8-B0258A/E**

21. **RLIN3**

13.9.2 Transmission in LIN Master Self-Test Mode

- Set the baud rate, noise filter, and interrupt output related registers. RSCANnTHLPCTRm register = 0000 xxx

**TN-RH8-B0258A/E**

22. **RLIN3**

13.9.3 Reception in LIN Master Self-Test Mode

- Set the baud rate, noise filter, and interrupt output related registers. RSCANnTHLPCTRm register = 0000 xxx

**TN-RH8-B0258A/E**

23. **RLIN3**

13.9.4 Transmission in LIN Slave Self-Test Mode

- Set the baud rate, noise filter, and interrupt output related registers. RSCANnTHLPCTRm register = 0000 xxx

**TN-RH8-B0258A/E**

24. **RLIN3**

13.9.5 Reception in LIN Slave Self-Test Mode

To execute a self-test on LIN slave reception, perform the procedure below:

**TN-RH8-B0258A/E**

25. **RS-CANFD**

14.3.13.3 RSCANnTHLPCTRm register

At this time, the RSCANnTHLPCTRm register is decremented.

**TN-RH8-B0258A/E**

26. **RS-CANFD**

14.4.14.3 RSCFDnCFDTHLPCTRm register

At this time, the RSCFDnCFDTHLPCTRm register is decremented.
The following block diagram shows the main components of the OSTM.

### 11.2.3 FIFO Buffer Reading Procedure

- When received messages have been stored in one or more receive FIFO buffers or in a transmit/receive FIFO buffer that is set to receive mode or gateway mode, the corresponding message count display counter (RFMC[10:0]) bits in the RSCFDn(CFD)CFSTx register (x = 0 to 7) or CFMC[7:0] bits in the RSCFDn(CFD)CFSTx register (k = 0 to 11) is incremented.

### 14.11.2 FIFO Buffer

- The following block diagram shows the main components of the OSTM.

#### 14.11.4 Receive Rule

- When messages are retransmitted due to an arbitration loss or an error, transmit priority determination is made again according to the TPRI bit.

---

**Figure 20.54 Example**

- Top: For receive FIFO buffers
  - RSCFDnCFDDFL, RSCFDnCFDDFPTR, RSCFDnCFDDFSTS, RSCFDnCFDDFDFd
- For transmit/receive FIFO buffers
  - RSCFDnCFDDFL, RSCFDnCFDDFPTR, RSCFDnCFDDFSTS, RSCFDnCFDDFDFd

- Bottom: For transmit/receive FIFO buffers
  - RSCFDnCFDDFL, RSCFDnCFDDFPTR, RSCFDnCFDDFSTS, RSCFDnCFDDFDFd

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**Figure 20.48 Example of Error Interrupt (INTTSG3nIER) Generation (PWM Mode)**

- For Transmit/PWM Mode
  - 0 to 100% PWM duty cycle output is possible (with possible dead time reduction).
  - The LSB in the compare register can be used to append an additional pulse to the PWM output during count up, thus improving the output resolution without extra load on software.

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**Figure 20.48 Example of Error Interrupt (INTTSG3nIER) Generation (PWM Mode)**

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---

**Figure 20.54 Example of Dead Time Control between TSG3nO1 and TSG3nO2 Outputs (2/2)**

- TSG3nCMP1E + TSG3nDTC1 ≥ TSG3nCMP0E + TSG3nDTC0 (TSG3nO1 remains inactive)
- TSG3nCMP2E + TSG3nDTC2 ≥ TSG3nCMP1E + TSG3nDTC1 (TSG3nO2 remains inactive)
- TSG3nCMP3E + TSG3nDTC3 ≥ TSG3nCMP2E + TSG3nDTC2 (TSG3nO1 remains inactive)

---

**Figure 20.54 Example of Dead Time Control between TSG3nO1 and TSG3nO2 Outputs (2/2)**

- At 1t, the falling edge (inactive) of the TSG3nO1 output is caused by the simultaneous active state detected and the dead time counter starts counting. After the end of the dead time counter operation, the TSG3nO2 output becomes active.
- At 1t, the falling edge (inactive) of the TSG3nO1 output is caused by the simultaneous active state detected and the dead time counter starts counting after a count-up match with the TSG3nCMP1 register. After the end of the dead time counter operation, the TSG3nO2 output becomes active.

---

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- At 1t, the falling edge (inactive) of the TSG3nO1 output is caused by the simultaneous active state detected and the dead time counter starts counting after a count-up match with the TSG3nCMP1 register. After the end of the dead time counter operation, the TSG3nO2 output becomes active.
26.4.5.1 Built-in Self-Test Function

The BISTs are categorized into two groups depending on their execution timing as follows:

- Execution is possible during angle conversion and when starting up the power (short-period BIST): ADBIST, resolver signal error detection BIST, resolver signal disconnect detection BIST, power short error BIST, ground short error BIST, sum-of-squares amplitude error detection BIST (high side), sum-of-squares amplitude error detection BIST (low side)
- Execution is possible when starting up the power: angle conversion BIST, conversion error BIST

Short-period BIST can also be executed at starting up the power. However, if angle conversion BIST or conversion error BIST or both are executed at power-on, they must be executed before short-period BIST.

26.4.6.1 Period Measurement Timer

The period measurement timer measures the cycle of excitation signal (zero-crossing signal). When an edge (selectable from rise edge and fall edge) of the zero-crossing signal is detected, the value of the period measurement counter is captured and stored in the RDC3AnETCAP register. By reading the RDC3AnETCAP register, the cycle of excitation signal can be obtained.

The cycle of excitation signal can be calculated from the following formula: \((RDC3AnETCAP\text{ register value} + 1) \times \text{CCLK cycle (25 ns)}\).

When the IREN bit in the RDC3AnETEN register is set to 1 (enables the interrupt), an excitation timer interrupt request is generated if the value set in the RDC3AnETCAP register matches the period measurement counter value. The excitation signal cycle error can be detected by setting a value of longer duration than the excitation signal cycle to the RDC3AnETCAP register.

26.6 Resolver Interface Circuit

1. \( RH \approx \left( \frac{RVCC - VCOM}{22.0 \times 10^{-6}} \right) - R_{\text{IN}} \), where \( VCOM = \frac{RVCC}{2}\text{[V]}\)

2. \( RH \approx \left( \frac{+V_{\text{EXT}} - VCOM}{22.0 \times 10^{-6}} \right) - R_{\text{IN}} \), where \( VCOM = \frac{RVCC}{2}\text{[V]}\)

**Note:** The equations for calculating the resistance of the resolver are provided in the document. However, there are discrepancies in the mathematical expressions, particularly in the coefficients and the use of variables.
<table>
<thead>
<tr>
<th>No.</th>
<th>PDF page</th>
<th>Section</th>
<th>Chapter title</th>
<th>Error</th>
<th>Correct</th>
<th>Change reason</th>
<th>Notice situation</th>
<th>Note</th>
</tr>
</thead>
<tbody>
<tr>
<td>51</td>
<td>2743</td>
<td>ECM</td>
<td>Table 30.8 List of Error Sources and Safety Processing (1/2)</td>
<td>6 RAM</td>
<td>Local RAM (CPU1, CPU2) 2-bit ECC error and local RAM (CPU1) address parity error&lt;sup&gt;a&lt;/sup&gt;</td>
<td>6 RAM</td>
<td>Local RAM (CPU1, CPU2) 2-bit ECC error and local RAM (CPU1, CPU2) address parity error&lt;sup&gt;a&lt;/sup&gt;</td>
<td>-</td>
</tr>
<tr>
<td>52</td>
<td>2835</td>
<td>Flash Memory</td>
<td>35.10 Notes</td>
<td>Do not perform the following operations during programming and erasure of the flash memory.</td>
<td>(7) Items prohibited during programming, erasure and blank checking</td>
<td>Do not perform the following operations during programming, erasure and blank checking of the flash memory.</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>53</td>
<td>2888</td>
<td>Electrical Characteristics</td>
<td>Table 39.33 RDC Conversion Performance (2/2)</td>
<td>Do not perform the following operations during programming and erasure of the flash memory.</td>
<td>(7) Items prohibited during programming, erasure and blank checking</td>
<td>Do not perform the following operations during programming, erasure and blank checking of the flash memory.</td>
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<td>-</td>
</tr>
</tbody>
</table>

End of the list.