**GENERAL DESCRIPTION**

This document describes specifications for the F1653NLGI I/Q Modulator implementing Zero-Distortion™ technology for low power consumption with improved ACLR. This device interfaces directly to a high performance dual DAC.

**COMPETITIVE ADVANTAGE**

In typical multi-mode, multi-carrier basestation transmitters the modulator has limited linearity and high power consumption which penalizes the system ACLR and system Power consumptions budgets in a Digital-Pre-Distortion environment.

The IDTF1653 is designed to eliminate these penalties by embedding Zero-Distortion™ technology into the device such that very high IP3 and IP2 are achieved with minimal current draw.

- Power consumption ↓45%
- IM3 Distortion ↓14 dB

**FEATURES**

- Power Gain = 3dB
- Direct 100Ω differential drive from Tx DAC
- < 590mW Power Consumption
- -159 dBm/Hz Output Noise
- -161 dBc/Hz Internal LO Path Noise
- IP2o = +64 dBm @ 2GHz
- IP3o = +36 dBm @ 2GHz
- Excellent native LO and image suppression
- 600 MHz input 1dB Bandwidth
- 600 MHz to 2900 MHz RF BW
- Fast Settling for TDD (< 200 nsec)
- 3.3V Single Power Supply
- LO port can be driven single ended or differential
- 4mm x 4mm, 24-pin TQFN package

**PART# MATRIX**

<table>
<thead>
<tr>
<th>Part#</th>
<th>RF freq Range</th>
<th>IP2o</th>
<th>Power Cons.</th>
<th>IP3o</th>
<th>Noise</th>
</tr>
</thead>
<tbody>
<tr>
<td>F1650</td>
<td>600 – 2400</td>
<td>+60 dBm</td>
<td>587 mW</td>
<td>+36 dBm</td>
<td>-158 dBm/Hz</td>
</tr>
<tr>
<td>F1653</td>
<td>600 – 2900</td>
<td>+64 dBm</td>
<td>587 mW</td>
<td>+36 dBm</td>
<td>-159 dBm/Hz</td>
</tr>
</tbody>
</table>

**ORDERING INFORMATION**

- Omit IDT prefix
- 0.8 mm height package
- Tape & Reel
- RF product Line
- Green
- Industrial Temp range

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**Absolute Maximum Ratings**

- **VDD to GND**: -0.3V to +3.6V
- **STBY**: -0.3V to (VDD + 0.3V)
- **BB_I+, BB_I-, BB_Q+, BB_Q-**: -0.3V to 1.8V
- **LO_IN**: -0.3V to 0.3V
- **RF_OUT**: (VDD-0.35V) to (VDD-0.05V)
- **Continuous Power Dissipation**: 1.5W
- **θJA (Junction – Ambient)**: +45°C/W
- **θJC (Junction – Case)**: The Case is defined as the exposed paddle +2.5°C/W
- **Operating Temperature Range (Case Temperature)**: 
  \[ T_{\text{CASE}} = -40°C \text{ to } +105°C \]
  150°C
- **Maximum Junction Temperature**: -65°C to +150°C
- **Lead Temperature (soldering, 10s)**: +260°C

*Stresses above those listed above may cause permanent damage to the device. Functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*
# IDTF1653 Recommended Operation Conditions

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Comment</th>
<th>min</th>
<th>typ</th>
<th>max</th>
<th>units</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply Voltage(s)</td>
<td>V&lt;sub&gt;DD&lt;/sub&gt;</td>
<td>All V&lt;sub&gt;DD&lt;/sub&gt; pins</td>
<td>3.15</td>
<td>3.30</td>
<td>3.45</td>
<td>V</td>
</tr>
<tr>
<td>Operating Temperature</td>
<td>T&lt;sub&gt;CASE&lt;/sub&gt;</td>
<td>Case Temperature</td>
<td>-40</td>
<td>25</td>
<td>+105</td>
<td>deg C</td>
</tr>
<tr>
<td>LO Freq Range</td>
<td>F&lt;sub&gt;LO&lt;/sub&gt;</td>
<td>LO power -3dBm to +5dBm</td>
<td>600</td>
<td>2900</td>
<td>MHz</td>
<td></td>
</tr>
<tr>
<td>BB Common Mode Voltage</td>
<td>V&lt;sub&gt;CM&lt;/sub&gt;</td>
<td>• T&lt;sub&gt;CASE&lt;/sub&gt; = -40C to +105C</td>
<td>0.1</td>
<td>0.25</td>
<td>0.8</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>• V&lt;sub&gt;DD&lt;/sub&gt; = 3.3 V</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>• LO level = 0dBm</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>BB input voltage</td>
<td></td>
<td>compliance range</td>
<td>0</td>
<td>1</td>
<td></td>
<td>Vpeak</td>
</tr>
<tr>
<td>BB Freq Range</td>
<td>F&lt;sub&gt;BB&lt;/sub&gt;</td>
<td>• F&lt;sub&gt;LO&lt;/sub&gt; = 1950 MHz, BB&lt;sub&gt;_IQ&lt;/sub&gt; = 200 mVp-p</td>
<td>DC</td>
<td>600</td>
<td>MHz</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>• P&lt;sub&gt;HR&lt;/sub&gt; degrades &lt; 1 dB</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
**IDT1653 Specification**

See application circuit. Typical values are measured at $V_{DD} = +3.3V$, $F_{LO} = 1950$ MHz, $P_{LO} = 0$ dBm, $T_{CASE} = +25^\circ C$, STBY = GND, BB_IQ frequency = 49, 50 MHz, BB_I&Q levels = 200 mVp-p each (-13dBm and 14 dB backoff from 1V DAC compliance), I & Q = 0.250V common-mode bias unless otherwise noted.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Comment</th>
<th>min</th>
<th>typ</th>
<th>max</th>
<th>units</th>
</tr>
</thead>
<tbody>
<tr>
<td>Logic Input High</td>
<td>$V_{IH}$</td>
<td>For STBY Pin</td>
<td>1.07</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>Logic Input Low</td>
<td>$V_{IL}$</td>
<td>For STBY Pin</td>
<td></td>
<td>0.68</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>Logic Current</td>
<td>$I_{IH}, I_{IL}$</td>
<td>For STBY Pin</td>
<td>-100</td>
<td></td>
<td>+1</td>
<td>μA</td>
</tr>
<tr>
<td>Supply Current (ON)</td>
<td>$I_{SUPP}$</td>
<td>Total $V_{DD}$</td>
<td>178</td>
<td></td>
<td>190</td>
<td>mA</td>
</tr>
<tr>
<td>Supply Current (STBY)</td>
<td>$I_{STBY}$</td>
<td>Total $V_{DD}$, STBY = $V_{IH}$</td>
<td>2.8</td>
<td>5</td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td>LO Power</td>
<td>$P_{LO}$</td>
<td>600MHz to 2900MHz</td>
<td>-3</td>
<td></td>
<td>+5</td>
<td>dBm</td>
</tr>
<tr>
<td>BB Input Resistance (Differential)</td>
<td>$R_{BB}$</td>
<td>Freq = 100 MHz</td>
<td>113</td>
<td></td>
<td></td>
<td>Ω</td>
</tr>
<tr>
<td>LO port Impedance</td>
<td>$Z_{LO}$</td>
<td>Single Ended (RL &lt; -10dB)</td>
<td>50</td>
<td></td>
<td></td>
<td>Ω</td>
</tr>
<tr>
<td>RF port Impedance</td>
<td>$Z_{RF}$</td>
<td>Single Ended (RL &lt; -10dB)</td>
<td>50</td>
<td></td>
<td></td>
<td>Ω</td>
</tr>
<tr>
<td>Power Gain</td>
<td>$G$</td>
<td></td>
<td>2.0</td>
<td>3.0</td>
<td>4.0</td>
<td>dB</td>
</tr>
<tr>
<td>Output IP3 @ 850 MHz</td>
<td>$IP3_{O1}$</td>
<td>LO = 800 MHz</td>
<td>37</td>
<td></td>
<td></td>
<td>dBm</td>
</tr>
<tr>
<td>Output IP3 @ 2.00 GHz</td>
<td>$IP3_{O2}$</td>
<td>LO = 1950 MHz</td>
<td>30</td>
<td>36</td>
<td></td>
<td>dBm</td>
</tr>
<tr>
<td>Output IP3 @ 2.85 GHz</td>
<td>$IP3_{O3}$</td>
<td>LO = 2800 MHz</td>
<td>31</td>
<td></td>
<td></td>
<td>dBm</td>
</tr>
<tr>
<td>Output IP2 @ 850 MHz</td>
<td>$IP2_{O1}$</td>
<td>LO = 800 MHz</td>
<td>65</td>
<td></td>
<td></td>
<td>dBm</td>
</tr>
<tr>
<td>Output IP2 @ 2.00 GHz</td>
<td>$IP2_{O}$</td>
<td>LO = 1950 MHz</td>
<td>64</td>
<td></td>
<td></td>
<td>dBm</td>
</tr>
<tr>
<td>Output IP2 @ 2.85 GHz</td>
<td>$IP3_{O2}$</td>
<td>LO = 2800 MHz</td>
<td>63</td>
<td></td>
<td></td>
<td>dBm</td>
</tr>
<tr>
<td>Turn on time</td>
<td>$P_{ON}$</td>
<td>STBY = low to 90% final output power</td>
<td>175</td>
<td></td>
<td></td>
<td>nsec</td>
</tr>
<tr>
<td>Turn off time</td>
<td>$P_{OFF}$</td>
<td>STBY = high to initial output power -30dB</td>
<td>26</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>LO (Carrier) Suppression</td>
<td>$LO_{supp}$</td>
<td>Native, Uncorrected</td>
<td>-39</td>
<td>-30</td>
<td></td>
<td>dBm</td>
</tr>
<tr>
<td>Sideband (Image) Suppression</td>
<td>$SS$</td>
<td>Native, Uncorrected $F_{LO} = 1950$ MHz</td>
<td>-34</td>
<td>-30</td>
<td></td>
<td>dBc</td>
</tr>
<tr>
<td>Output P1dB</td>
<td>$P1dB_{O}$</td>
<td>Output Compression</td>
<td>15</td>
<td></td>
<td></td>
<td>dBm</td>
</tr>
<tr>
<td>Output Noise</td>
<td>$NSD$</td>
<td>10 MHz offset from LO</td>
<td>-157</td>
<td>-159</td>
<td></td>
<td>dBm/Hz</td>
</tr>
<tr>
<td>LO Path Noise (internal)</td>
<td>$\Phi_{N,LO}$</td>
<td>+10 MHz offset</td>
<td>-161</td>
<td></td>
<td></td>
<td>dBc/Hz</td>
</tr>
</tbody>
</table>

**Specification Notes:**

1 – Items in min/max columns in **bold italics** are Guaranteed by Test
2 – All other Items in min/max columns are Guaranteed by Design Characterization
**TYPICAL OPERATING CONDITIONS graphs**

Unless otherwise noted, the following conditions apply:

- Baseband I&Q levels = 200 mVpp each (-13 dBm / Channel / Tone)
- Baseband I&Q tones = 49, 50 MHz
- Low Side Injection
- $T_{\text{AMB}} = 25^\circ\text{C}$, $V_{\text{CC}} = 3.30$ V, LO Power = 0 dBm
- $V_{\text{CM}} = 0.250$ Volts
- $f_0 = 1.95\text{GHz}$ unless otherwise specified
- EVKit RF output Trace and Connector Losses De-Embedded

**EVkit RF output loss (Trace + Connector)**
TYPICAL OPERATING CONDITIONS (-1-)

OIP3 vs. $T_{\text{AMB}}$

OIP3 vs. $V_{\text{CC}}$

OIP3 vs. LO level

OIP2 vs. $T_{\text{AMB}}$

OIP2 vs. $V_{\text{CC}}$

OIP2 vs. LO level

Zero-Distortion™ Modulator

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**TYPICAL OPERATING CONDITIONS (-2-)**

**I<sub>CC</sub> vs. T<sub>AMB</sub>**

- 45degC / 3.30V / 0dBm
- 25degC / 3.30V / 0dBm
- 85degC / 3.30V / 0dBm
- 100degC / 3.30V / 0dBm

**I<sub>CC</sub> vs. LO level**

- 25degC / 3.30V / 5dBm
- 25degC / 3.30V / 0dBm
- 25degC / 3.30V / -3dBm

**Power Consumption vs. T<sub>AMB</sub>**

- 45degC / 3.30V / 0dBm
- 25degC / 3.30V / 0dBm
- 85degC / 3.30V / 0dBm
- 100degC / 3.30V / 0dBm

**Power Consumption vs. V<sub>CC</sub>**

- 25degC / 3.45V / 0dBm

**Power Consumption vs. LO level**

- 25degC / 3.30V / 5dBm
- 25degC / 3.30V / 0dBm
- 25degC / 3.30V / -3dBm
TYPICAL OPERATING CONDITIONS

Gain vs. $T_{\text{AMB}}$

Gain vs. $V_{\text{CC}}$

Gain vs. LO level

RF Output Power vs. $T_{\text{AMB}}$

RF Output Power vs. $V_{\text{CC}}$

RF Output Power vs. LO level

Zero-Distortion™ Modulator

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TYPICAL OPERATING CONDITIONS (-4-)

Unadjusted LO Suppression vs. T\textsubscript{AMB}

Unadjusted LO Suppression vs. V\textsubscript{CC}

Unadjusted LO Suppression vs. LO level

Unadjusted Sideband Suppression vs. T\textsubscript{AMB}

Unadjusted Sideband Suppression vs. V\textsubscript{CC}

Unadjusted Sideband Suppression vs. LO level
TYPICAL OPERATING CONDITIONS (-5-)

Baseband 2\textsuperscript{nd} Harmonic vs. T\textsubscript{AMB}

Baseband 2\textsuperscript{nd} Harmonic vs. V\textsubscript{CC}

Baseband 2\textsuperscript{nd} Harmonic vs. LO level

Baseband 3\textsuperscript{rd} Harmonic vs. V\textsubscript{CC}

Baseband 3\textsuperscript{rd} Harmonic vs. T\textsubscript{AMB}

Baseband 3\textsuperscript{rd} Harmonic vs. LO level

Zero-Distortion\textsuperscript{TM} Modulator

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**TYPICAL OPERATING CONDITIONS (-6-)**

**Output Noise vs. Frequency**

-46 dBm/Hz to -160 dBm/Hz

**Input Bandwidth (fixed LO = 2.092 GHz)**

Power Gain (dB)

-3 to 20 dB

**LO & RF Port Return Loss**

Return Loss (dB)

-35 dB to 0 dB

**1dB Compression**

Output Power (dBm)

-2 to 2 dB

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Zero-Distortion™ Modulator 11

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RevO, April 2015
Typical Operating Conditions (-7-)

Turn On Time

Polarity: LO = 2.0GHz, BB_I+/- leads BB_Q+/-

Turn Off Time

Polarity: LO = 2.0GHz, BB_I+/- lags BB_Q+/-

Carrier Suppression Nulling Performance

Image Suppression Nulling Performance
**Generic DAC Interface**

- **LCM DAC**: low common mode voltage DAC usually has high output impedance and sourcing current out
- **LPF**: to filter out unwanted harmonics
- **DC common mode voltage on BBP/BBN**: $V_{cm} = IDC \times \frac{R_{dac}}{R_{dc_{IQMOD}}}$
- **$V_{cm}$** is determined by DAC bias current and IQ Mod input DC impedance

DC impedance: 50Ω per side
AC impedance: 100Ω differential
Zero-Distortion™ Modulator

Top View
(looking through the top of the package)

Exposed Pad

Package Drawing

- 4 mm x 4 mm package dimension
- 2.60 mm x 2.60 mm exposed pad
- 0.5 mm pitch
- 24 pins
- 0.75 mm height
- 0.25 mm pad width
- 0.40 mm pad length
## Pin Descriptions

<table>
<thead>
<tr>
<th>Pins</th>
<th>Name</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>STBY</td>
<td>STBY Mode. Pull this pin high for Standby Mode. Pull low or ground for Normal Operation.</td>
</tr>
<tr>
<td>2, 5, 13, 19</td>
<td>GND</td>
<td>Ground these pins.</td>
</tr>
<tr>
<td>6, 7, 8, 11, 12, 14, 15, 17, 20, 23</td>
<td>NC</td>
<td>IDT recommends grounding these pins.</td>
</tr>
<tr>
<td>3, 4</td>
<td>LO+, LO-</td>
<td>Local oscillator (LO) 50 ohm differential or 25ohm each pin single-ended input. Pins must be ac-coupled. For 50 ohm single-ended operation, ac-couple USED Pin to 50 ohm termination and ac-couple UNUSED pin to GND.</td>
</tr>
<tr>
<td>9, 10</td>
<td>BB_Q-, BB_Q+</td>
<td>Quadrature differential baseband input. Internally matched to 100 ohms.</td>
</tr>
<tr>
<td>16</td>
<td>RF_OUT</td>
<td>RF output. Must be ac-coupled.</td>
</tr>
<tr>
<td>18, 24</td>
<td>VDD</td>
<td>Power Supply. Bypass to GND with capacitors as shown in the Typical Application Circuit as close to pin as possible.</td>
</tr>
<tr>
<td>21, 22</td>
<td>BB_I+, BB_I-</td>
<td>In-Phase differential baseband input. Internally matched to 100 ohms.</td>
</tr>
<tr>
<td>— EP</td>
<td>—</td>
<td>Exposed Pad. Internally connected to GND. Solder this exposed pad to a PCB pad that uses multiple ground vias to provide heat transfer out of the device into the PCB ground planes. These multiple via grounds are also required to achieve the specified RF performance.</td>
</tr>
</tbody>
</table>
**POWER SUPPLIES**

All supply pins should be bypassed with external capacitors to minimize noise and fast transients. Supply noise can degrade noise figure and fast transients can trigger ESD clamps and cause them to fail. Supply voltage change or transients should have a slew rate smaller than 1V/20uS. In addition, all control pins should remain at 0V (+/-0.3V) while the supply voltage ramps or while it returns to zero.
With L1, L2, L3, and L4 unpopulated, the common mode voltage is set by VR2 and VR4. The voltage set by VR2 has a DC path through the balun transformer T1 to pins BB_I+ and BB_I-, as highlighted. This also applies for VR4, T2, and pins BB_Q+ and BB_Q-. With this configuration, the same voltage will be applied to BB_I+ and BB_I- and the same voltage will be applied to BB_Q+ and BB_Q-. The I and Q common mode voltages may be different from each other to null LO (carrier) leakage.
Note: VCC connection on evaluation board is VDD Power Supply on the datasheet.

VDD connection on evaluation board is used to set baseband pin common mode (CM) voltage (see schematic)
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