**General Description**

This document describes specifications for the F1653NLGI I/Q Modulator implementing Zero-Distortion™ technology for low power consumption with improved ACLR. This device interfaces directly to a high performance dual DAC.

**Competitive Advantage**

In typical multi-mode, multi-carrier basestation transmitters the modulator has limited linearity and high power consumption which penalizes the system ACLR and system Power consumptions budgets in a Digital-Pre-Distortion environment.

The IDTF1653 is designed to eliminate these penalties by embedding Zero-Distortion™ technology into the device such that very high IP3 and IP2 are achieved with minimal current draw.

- Power consumption ↓45%
- IM3 Distortion ↓14 dB

**Features**

- Power Gain = 3dB
- Direct 100Ω differential drive from Tx DAC
- < 590mW Power Consumption
- -159 dBm/Hz Output Noise
- -161 dBc/Hz Internal LO Path Noise
- IP2 = +64 dBm @ 2GHz
- IP3 = +36 dBm @ 2GHz
- Excellent native LO and image suppression
- 600 MHz input 1dB Bandwidth
- 600 MHz to 2900 MHz RF BW
- **Fast Settling for TDD (< 200 nsec)**
- 3.3V Single Power Supply
- LO port can be driven single ended or differential
- 4mm x 4mm, 24-pin TQFN package

**Part# Matrix**

<table>
<thead>
<tr>
<th>Part#</th>
<th>RF freq Range</th>
<th>IP2o</th>
<th>Power Cons.</th>
<th>IP3o</th>
<th>Noise</th>
</tr>
</thead>
<tbody>
<tr>
<td>F1650</td>
<td>600 – 2400</td>
<td>+60 dBm</td>
<td>587 mW</td>
<td>+36 dBm</td>
<td>-158 dBm/Hz</td>
</tr>
<tr>
<td>F1653</td>
<td>600 – 2900</td>
<td>+64 dBm</td>
<td>587 mW</td>
<td>+36 dBm</td>
<td>-159 dBm/Hz</td>
</tr>
</tbody>
</table>

**Ordering Information**

- Omit IDT prefix
- 0.8 mm height package
- Tape & Reel

**Device Block Diagram**

The Device Block Diagram shows the internal structure of the F1653NLGI, including the key components and connections that enable its high performance and low power consumption.

**Zero-Distortion™ Modulator**

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ABSOLUTE MAXIMUM RATINGS

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Rating</th>
</tr>
</thead>
<tbody>
<tr>
<td>VDD to GND</td>
<td>-0.3V to +3.6V</td>
</tr>
<tr>
<td>STBY</td>
<td>-0.3V to (VDD + 0.3V)</td>
</tr>
<tr>
<td>BB_I+, BB_I-, BB_Q+, BB_Q-</td>
<td>-0.3V to 1.8V</td>
</tr>
<tr>
<td>LO_IN</td>
<td>-0.3V to 0.3V</td>
</tr>
<tr>
<td>RF_OUT</td>
<td>(VDD-0.35V) to (VDD-0.05V)</td>
</tr>
<tr>
<td>Continuous Power Dissipation</td>
<td>1.5W</td>
</tr>
<tr>
<td>$\theta_{JA}$ (Junction – Ambient)</td>
<td>+45°C/W</td>
</tr>
<tr>
<td>$\theta_{JC}$ (Junction – Case)</td>
<td>+2.5°C/W</td>
</tr>
<tr>
<td>Operating Temperature Range (Case Temperature)</td>
<td>$T_{CASE} = -40^\circ C$ to $+105^\circ C$</td>
</tr>
<tr>
<td>Maximum Junction Temperature</td>
<td>150°C</td>
</tr>
<tr>
<td>Storage Temperature Range</td>
<td>-65°C to +150°C</td>
</tr>
<tr>
<td>Lead Temperature (soldering, 10s)</td>
<td>+260°C</td>
</tr>
</tbody>
</table>

Stresses above those listed above may cause permanent damage to the device. Functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
### IDTF1653 Recommended Operation Conditions

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Comment</th>
<th>min</th>
<th>typ</th>
<th>max</th>
<th>units</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply Voltage(s)</td>
<td>V_{DD}</td>
<td>All V_{DD} pins</td>
<td>3.15</td>
<td>3.30</td>
<td>3.45</td>
<td>V</td>
</tr>
<tr>
<td>Operating Temperature</td>
<td>T_{CASE}</td>
<td>Case Temperature</td>
<td>-40</td>
<td>25</td>
<td>+105</td>
<td>deg C</td>
</tr>
<tr>
<td>LO Freq Range</td>
<td>F_{LO}</td>
<td>LO power -3dBm to +5dBm</td>
<td>600</td>
<td>2900</td>
<td></td>
<td>MHz</td>
</tr>
<tr>
<td>BB Common Mode Voltage</td>
<td>V_{CM}</td>
<td>• T_{CASE} = -40C to +105C</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>• V_{DD} = 3.3 V</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>• LO level = 0dBm</td>
<td>0.1</td>
<td>0.25</td>
<td>0.8</td>
<td>V</td>
</tr>
<tr>
<td>BB input voltage compliance range</td>
<td></td>
<td>For each BB pin</td>
<td>0</td>
<td>1</td>
<td></td>
<td>Vpeak</td>
</tr>
<tr>
<td>BB Freq Range</td>
<td>F_{BB}</td>
<td>• F_{LO} = 1950 MHz, BB_{IQ} = 200 mVp-p</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>• P_{BF} degrades &lt; 1 dB</td>
<td>DC</td>
<td>600</td>
<td></td>
<td>MHz</td>
</tr>
</tbody>
</table>
### IDTF1653 SPECIFICATION

See application circuit. Typical values are measured at $V_{DD} = +3.3\,\text{V}$, $F_{LO} = 1950\,\text{MHz}$, $P_{LO} = 0\,\text{dBm}$, $T_{CASE} = +25\,\text{°C}$, $\text{STBY} = \text{GND}$, $\text{BB_IQ}$ frequency = 49, 50 MHz, $\text{BB_IQ}$ levels = 200 mVp-p each (-13dBm and 14 dB backoff from 1V DAC compliance), $\text{I} \& \text{Q} = 0.250\,\text{V}$ common-mode bias unless otherwise noted.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Comment</th>
<th>min</th>
<th>typ</th>
<th>max</th>
<th>units</th>
</tr>
</thead>
<tbody>
<tr>
<td>Logic Input High</td>
<td>$V_{IH}$</td>
<td>For STBY Pin</td>
<td>1.07</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>Logic Input Low</td>
<td>$V_{IL}$</td>
<td>For STBY Pin</td>
<td>0.68</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>Logic Current</td>
<td>$I_{IH}, I_{IL}$</td>
<td>For STBY Pin</td>
<td>-100</td>
<td>+1</td>
<td></td>
<td>$\mu\text{A}$</td>
</tr>
<tr>
<td>Supply Current (ON)</td>
<td>$I_{SUPP}$</td>
<td>Total $V_{DD}$</td>
<td></td>
<td>178</td>
<td>190</td>
<td>mA</td>
</tr>
<tr>
<td>Supply Current (STBY)</td>
<td>$I_{STBY}$</td>
<td>Total $V_{DD}$, $\text{STBY} = V_{IH}$</td>
<td>2.8</td>
<td>5</td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td>LO Power</td>
<td>$P_{LO}$</td>
<td>600MHz to 2900MHz</td>
<td>-3</td>
<td></td>
<td>+5</td>
<td>dBm</td>
</tr>
<tr>
<td>BB Input Resistance (Differential)</td>
<td>$R_{BB}$</td>
<td>Freq = 100 MHz</td>
<td></td>
<td>113</td>
<td></td>
<td>$\Omega$</td>
</tr>
<tr>
<td>LO port Impedance</td>
<td>$Z_{LO}$</td>
<td>Single Ended (RL &lt; -10dB)</td>
<td></td>
<td>50</td>
<td></td>
<td>$\Omega$</td>
</tr>
<tr>
<td>RF port Impedance</td>
<td>$Z_{RF}$</td>
<td>Single Ended (RL &lt; -10dB)</td>
<td></td>
<td>50</td>
<td></td>
<td>$\Omega$</td>
</tr>
<tr>
<td>Power Gain</td>
<td>$G$</td>
<td></td>
<td>2.0</td>
<td>3.0</td>
<td>4.0</td>
<td>dB</td>
</tr>
<tr>
<td>Output IP3 @ 850 MHz</td>
<td>$IP_{3O1}$</td>
<td>LO = 800 MHz</td>
<td></td>
<td>37</td>
<td></td>
<td>dBm</td>
</tr>
<tr>
<td>Output IP3 @ 2.00 GHz</td>
<td>$IP_{3O2}$</td>
<td>LO = 1950 MHz</td>
<td>30</td>
<td>36</td>
<td></td>
<td>dBm</td>
</tr>
<tr>
<td>Output IP3 @ 2.85 GHz</td>
<td>$IP_{3O3}$</td>
<td>LO = 2800 MHz</td>
<td></td>
<td>31</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Output IP2 @ 850 MHz</td>
<td>$IP_{2O1}$</td>
<td>LO = 800 MHz</td>
<td></td>
<td>65</td>
<td></td>
<td>dBm</td>
</tr>
<tr>
<td>Output IP2 @ 2.00 GHz</td>
<td>$IP_{2O}$</td>
<td>LO = 1950 MHz</td>
<td>582</td>
<td>64</td>
<td></td>
<td>dBm</td>
</tr>
<tr>
<td>Output IP2 @ 2.85 GHz</td>
<td>$IP_{3O2}$</td>
<td>LO = 2800 MHz</td>
<td></td>
<td>63</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Turn on time</td>
<td>$P_{ON}$</td>
<td>STBY = low to 90% final output power</td>
<td></td>
<td>175</td>
<td></td>
<td>nsec</td>
</tr>
<tr>
<td>Turn off time</td>
<td>$P_{OFF}$</td>
<td>STBY = high to initial output power -30dB</td>
<td></td>
<td>26</td>
<td></td>
<td></td>
</tr>
<tr>
<td>LO (Carrier) Suppression</td>
<td>$LO_{supp}$</td>
<td>Native, Uncorrected $F_{LO} = 1950,\text{MHz}$</td>
<td>-39</td>
<td>-30</td>
<td></td>
<td>dBm</td>
</tr>
<tr>
<td>Sideband (Image) Suppression</td>
<td>$SS$</td>
<td>Native, Uncorrected $F_{LO} = 1950,\text{MHz}$</td>
<td>-34</td>
<td>-30</td>
<td></td>
<td>dBc</td>
</tr>
<tr>
<td>Output P1dB</td>
<td>$P_{1dBO}$</td>
<td>Output Compression</td>
<td>15</td>
<td></td>
<td></td>
<td>dBm</td>
</tr>
<tr>
<td>Output Noise</td>
<td>$NSD$</td>
<td>10 MHz offset from LO</td>
<td>-157</td>
<td>-159</td>
<td></td>
<td>dBm/Hz</td>
</tr>
<tr>
<td>LO Path Noise (internal)</td>
<td>$\Phi_{N,LO}$</td>
<td>+10 MHz offset</td>
<td>-161</td>
<td></td>
<td></td>
<td>dBc/Hz</td>
</tr>
</tbody>
</table>

### SPECIFICATION NOTES:
1 – Items in min/max columns in *bold italics* are Guaranteed by Test
2 – All other Items in min/max columns are Guaranteed by Design Characterization
TYPICAL OPERATING CONDITIONS GRAPHS

Unless otherwise noted, the following conditions apply:

- Baseband I&Q levels = 200 mVpp each (-13 dBm / Channel / Tone)
- Baseband I&Q tones = 49, 50 MHz
- Low Side Injection
- $T_{\text{AMB}} = 25^\circ\text{C}$, $V_{\text{CC}} = 3.30$ V, LO Power = 0 dBm
- $V_{\text{CM}} = 0.250$ Volts
- $F_0 = 1.95\text{GHz}$ unless otherwise specified
- EVKit RF output Trace and Connector Losses De-Embedded

**EVkit RF output loss (Trace + Connector)**
**TYPICAL OPERATING CONDITIONS (-1-)**

**OIP3 vs. $T_{AMB}$**

![Graph showing OIP3 vs. $T_{AMB}$](image)

**OIP3 vs. $V_{CC}$**

![Graph showing OIP3 vs. $V_{CC}$](image)

**OIP3 vs. LO level**

![Graph showing OIP3 vs. LO level](image)

**OIP2 vs. $T_{AMB}$**

![Graph showing OIP2 vs. $T_{AMB}$](image)

**OIP2 vs. $V_{CC}$**

![Graph showing OIP2 vs. $V_{CC}$](image)

**OIP2 vs. LO level**

![Graph showing OIP2 vs. LO level](image)
TYPICAL OPERATING CONDITIONS (-2-)

**I<sub>CC</sub> vs. T<sub>AMB</sub>**

- 45degC / 3.30V / 0dBm
- 25degC / 3.30V / 0dBm
- 85degC / 3.30V / 0dBm
- 100degC / 3.30V / 0dBm

**I<sub>CC</sub> vs. LO level**

- 25degC / 3.30V / 5dBm
- 25degC / 3.30V / 0dBm
- 25degC / 3.30V / -3dBm

**Power Consumption vs. T<sub>AMB</sub>**

- 45degC / 3.30V / 0dBm
- 25degC / 3.30V / 0dBm
- 85degC / 3.30V / 0dBm
- 100degC / 3.30V / 0dBm

**Power Consumption vs. V<sub>CC</sub>**

- 25degC / 3.45V / 0dBm
- 25degC / 3.30V / 0dBm
- 25degC / 3.15V / 0dBm

**Power Consumption vs. LO level**

- 25degC / 3.45V / 5dBm
- 25degC / 3.30V / 0dBm
- 25degC / 3.30V / -3dBm
**TYPICAL OPERATING CONDITIONS (-3-)**

**Gain vs. T_{AMB}**

![Graph showing Gain vs. T_{AMB} for different temperatures and voltage levels.](image1)

**Gain vs. V_{CC}**

![Graph showing Gain vs. V_{CC} for different voltage levels.](image2)

**Gain vs. LO level**

![Graph showing Gain vs. LO level for different temperatures and voltage levels.](image3)

**RF Output Power vs. T_{AMB}**

![Graph showing RF Output Power vs. T_{AMB} for different temperatures and voltage levels.](image4)

**RF Output Power vs. V_{CC}**

![Graph showing RF Output Power vs. V_{CC} for different voltage levels.](image5)

**RF Output Power vs. LO level**

![Graph showing RF Output Power vs. LO level for different temperatures and voltage levels.](image6)
**TYPICAL OPERATING CONDITIONS (−4−)**

**Unadjusted LO Suppression vs. T\textsubscript{AMB}**

![Graph showing Unadjusted LO Suppression vs. T\textsubscript{AMB}]

**Unadjusted LO Suppression vs. V\textsubscript{CC}**

![Graph showing Unadjusted LO Suppression vs. V\textsubscript{CC}]

**Unadjusted LO Suppression vs. LO level**

![Graph showing Unadjusted LO Suppression vs. LO level]}

**Unadjusted Sideband Suppression vs. T\textsubscript{AMB}**

![Graph showing Unadjusted Sideband Suppression vs. T\textsubscript{AMB}]

**Unadjusted Sideband Suppression vs. V\textsubscript{CC}**

![Graph showing Unadjusted Sideband Suppression vs. V\textsubscript{CC}]

**Unadjusted Sideband Suppression vs. LO level**

![Graph showing Unadjusted Sideband Suppression vs. LO level]
**TYPICAL OPERATING CONDITIONS (-5-)**

**Baseband 2\(^{nd}\) Harmonic vs. T\(_{AMB}\)**

- **25\(^\circ\)C / 3.30V / 0dBm**
- **25\(^\circ\)C / 3.30V / 0dBm**
- **85\(^\circ\)C / 3.30V / 0dBm**
- **100\(^\circ\)C / 3.30V / 0dBm**

**Baseband 2\(^{nd}\) Harmonic vs. V\(_{CC}\)**

- **25\(^\circ\)C / 3.45V / 0dBm**
- **25\(^\circ\)C / 3.30V / 0dBm**
- **25\(^\circ\)C / 3.30V / -3dBm**

**Baseband 2\(^{nd}\) Harmonic vs. LO level**

- **25\(^\circ\)C / 3.30V / 5dBm**
- **25\(^\circ\)C / 3.30V / 0dBm**
- **25\(^\circ\)C / 3.30V / -3dBm**

**Baseband 3\(^{rd}\) Harmonic vs. T\(_{AMB}\)**

- **45\(^\circ\)C / 3.30V / 0dBm**
- **25\(^\circ\)C / 3.30V / 0dBm**
- **85\(^\circ\)C / 3.30V / 0dBm**
- **100\(^\circ\)C / 3.30V / 0dBm**

**Baseband 3\(^{rd}\) Harmonic vs. V\(_{CC}\)**

- **25\(^\circ\)C / 3.45V / 0dBm**
- **25\(^\circ\)C / 3.30V / 0dBm**
- **25\(^\circ\)C / 3.15V / 0dBm**

**Baseband 3\(^{rd}\) Harmonic vs. LO level**

- **25\(^\circ\)C / 3.30V / 5dBm**
- **25\(^\circ\)C / 3.30V / 0dBm**
- **25\(^\circ\)C / 3.30V / -3dBm**
TYPICAL OPERATING CONDITIONS (-6-)

Output Noise vs. Frequency

![Graph showing output noise vs. frequency.]

Input Bandwidth (fixed LO = 2.092 GHz)

![Graph showing input bandwidth.]

I&Q Input Parallel Resistance/Capacitance

![Graph showing I&Q input parallel resistance/capacitance.]

1dB Compression

![Graph showing 1dB compression.]

Output Noise vs. POUT [VCC = 3.3V, TAM = 25C]

![Graph showing output noise vs. output power.]

LO & RF Port Return Loss

![Graph showing return loss.]

Baseband Input Frequency (MHz)

Power Gain (dB)

-35 -30 -25 -20 -15 -10 -5 0 0.5 0.7 0.9 1.1 1.3 1.5 1.7 1.9 2.1 2.3 2.5 2.7 2.9

Baseband Frequency (GHz)

Return Loss (dB)

RF Port
LO Port

-40degC 25degC 105degC

LO Frequency = 1.95 GHz

LO Level (dBm) VSUPPLY

3.15V 3.30V 3.45V

Output P1dB (dBm)

-3 0 5 -3 0 5 -3 0 5

3.15V 3.30V 3.45V

Output P1dB (dBm) vs. LO Frequency

LO Frequency (GHz)

-3 0 5 -3 0 5 -3 0 5

LO Level (dBm) VSUPPLY

3.15V 3.30V 3.45V

Output P1dB (dBm) vs. LO Frequency
TYPICAL OPERATING CONDITIONS (-7-)

Turn On Time

Turn on time <200ns
Flo=2GHz, 3.3V, 25deg

Polarity: LO = 2.0GHz, BB_I+/ leads BB_Q+/

Carrier Suppression Nulling Performance

Image Suppression Nulling Performance

Polarity: LO = 2.0GHz, BB_I+/- lags BB_Q+/-

Typical Operating Conditions

Turn Off Time

Turn off time <30ns
Flo=2GHz, 3.3V, 25deg

Sideband Suppression (dBc)

STBY
RF signal

STBY
RF signal
**GENERIC DAC INTERFACE**

- LCM DAC: low common mode voltage DAC usually has high output impedance and sourcing current out
- LPF: to filter out unwanted harmonics
- DC common mode voltage on BBP/BBN Vcm: \( V_{cm} = IDC \times R_{dac} // R_{dc_{IQMOD}} \)
- \( V_{cm} \) is determined by DAC bias current and IQ Mod input DC impedance

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**Diagram:**

- DAC LCM
- IOUTxP
- IOUTxN
- I_bias + 0.5I_{fs} 0 to 20 mA
- \( R_{dac} \) 50Ω
- \( R_{int} \) 50Ω
- V_{cm}

**Specifications:**

- DC impedance: 50Ω per side
- AC impedance: 100Ω differential

**Equations:**

- \( I_{dc} = I_{bias} + 0.5I_{fs} \)
TOP View
(looking through the top of the package)

Package Drawing

- 4 mm x 4 mm package dimension
- 2.60 mm x 2.60 mm exposed pad
- 0.5 mm pitch
- 24 pins
- 0.75 mm height
- 0.25 mm pad width
- 0.40 mm pad length

Exposed Pad
## Pin Descriptions

<table>
<thead>
<tr>
<th>Pins</th>
<th>Name</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>STBY</td>
<td>STBY Mode. Pull this pin high for Standby Mode. Pull low or ground for Normal Operation.</td>
</tr>
<tr>
<td>2, 5, 13, 19</td>
<td>GND</td>
<td>Ground these pins.</td>
</tr>
<tr>
<td>6, 7, 8, 11, 12, 14, 15, 17, 20, 23</td>
<td>NC</td>
<td>IDT recommends grounding these pins.</td>
</tr>
<tr>
<td>3, 4</td>
<td>LO+, LO-</td>
<td>Local oscillator (LO) 50 ohm differential or 25ohm each pin single-ended input. Pins must be ac-coupled. For 50 ohm single-ended operation, ac-couple USED Pin to 50 ohm termination and ac-couple UNUSED pin to GND.</td>
</tr>
<tr>
<td>9, 10</td>
<td>BB_Q-, BB_Q+</td>
<td>Quadrature differential baseband input. Internally matched to 100 ohms.</td>
</tr>
<tr>
<td>16</td>
<td>RF_OUT</td>
<td>RF output. Must be ac-coupled.</td>
</tr>
<tr>
<td>18, 24</td>
<td>VDD</td>
<td>Power Supply. Bypass to GND with capacitors as shown in the Typical Application Circuit as close to pin as possible.</td>
</tr>
<tr>
<td>21, 22</td>
<td>BB_I+, BB_I-</td>
<td>In-Phase differential baseband input. Internally matched to 100 ohms.</td>
</tr>
<tr>
<td>— EP</td>
<td></td>
<td>Exposed Pad. Internally connected to GND. Solder this exposed pad to a PCB pad that uses multiple ground vias to provide heat transfer out of the device into the PCB ground planes. These multiple via grounds are also required to achieve the specified RF performance.</td>
</tr>
</tbody>
</table>
**POWER SUPPLIES**

All supply pins should be bypassed with external capacitors to minimize noise and fast transients. Supply noise can degrade noise figure and fast transients can trigger ESD clamps and cause them to fail. Supply voltage change or transients should have a slew rate smaller than 1V/20uS. In addition, all control pins should remain at 0V (+/-0.3V) while the supply voltage ramps or while it returns to zero.
EVKit BOM

<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>C2</td>
<td>1</td>
<td>8pF ±0.5pF, 50V, C0G Ceramic Capacitor (0402)</td>
<td>GRM1555C1H8R0D</td>
<td>MURATA</td>
</tr>
<tr>
<td>C4,C6,C8,C10,C17</td>
<td>5</td>
<td>10pF ±10%, 16V, X7R Ceramic Capacitor (0402)</td>
<td>GRM1555C1H103K</td>
<td>MURATA</td>
</tr>
<tr>
<td>C1</td>
<td>1</td>
<td>39pF ±5%, 50V, C0G Ceramic Capacitor (0402)</td>
<td>GRM1555C1H036J</td>
<td>MURATA</td>
</tr>
<tr>
<td>C7,C9</td>
<td>2</td>
<td>100nF ±10%, 16V, X7R Ceramic Capacitor (0402)</td>
<td>GRM155R71C104K</td>
<td>MURATA</td>
</tr>
<tr>
<td>R3,R6,R9,C13-C16,L5</td>
<td>8</td>
<td>0Ω 1/10W Resistor (0402)</td>
<td>ERJ-2GE0R00X</td>
<td>Panasonic</td>
</tr>
<tr>
<td>R5,R12</td>
<td>2</td>
<td>24.9 Ω ±1%, 1/4W Resistor (1206)</td>
<td>RMCP1206F124R9</td>
<td>Stackpole Electronics</td>
</tr>
<tr>
<td>R1</td>
<td>1</td>
<td>47.0KΩ ±1%, 1/16W Resistor (0402)</td>
<td>RC0402FAR-0747KL</td>
<td>Yageo</td>
</tr>
<tr>
<td>VR2,VR4</td>
<td>2</td>
<td>1KΩ ±10%, 1/4W Resistor Trimmer</td>
<td>TS63Y102KR10</td>
<td>Vishay/Sfernice</td>
</tr>
<tr>
<td>J2,J5,J6,J9</td>
<td>4</td>
<td>CONN HEADER VERT SGL 2 X 1 POS GOLD</td>
<td>961102-6404-AR</td>
<td>3M</td>
</tr>
<tr>
<td>J3,J4,J7,J10</td>
<td>4</td>
<td>Edge Launch SMA (0.250 inch width, round center contact)</td>
<td>142-0711-821</td>
<td>Emerson Johnson</td>
</tr>
<tr>
<td>J1,J6</td>
<td>2</td>
<td>Edge Launch SMA (0.500 inch width, flat center contact)</td>
<td>142-0701-851</td>
<td>Emerson Johnson</td>
</tr>
<tr>
<td>T1,T2</td>
<td>2</td>
<td>2:1 Center Tap Balun</td>
<td>AD12-11+</td>
<td>Minn Circuits</td>
</tr>
<tr>
<td>U1</td>
<td>1</td>
<td>IQ MOD</td>
<td>F1653</td>
<td>IDT</td>
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<td></td>
<td></td>
<td>Printed Circuit Board</td>
<td>F1650 SE EVKIT REV (02)</td>
<td>Coastal Circuits</td>
</tr>
<tr>
<td>VR1,VR3</td>
<td></td>
<td>DNP</td>
<td></td>
<td></td>
</tr>
<tr>
<td>C3,C5,C11,C12,C18</td>
<td></td>
<td>DNP</td>
<td></td>
<td></td>
</tr>
<tr>
<td>L1,L2,L3,L4</td>
<td></td>
<td>DNP</td>
<td></td>
<td></td>
</tr>
<tr>
<td>R2,R4,R6,R7,R10,R11</td>
<td></td>
<td>DNP</td>
<td></td>
<td></td>
</tr>
<tr>
<td>R13,R14,R16,R18</td>
<td></td>
<td>DNP</td>
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</tr>
</tbody>
</table>

APPLYING $V_{CM}$ AT THE BASEBand Inputs

With L1, L2, L3, and L4 unpopulated, the common mode voltage is set by VR2 and VR4. The voltage set by VR2 has a DC path through the balun transformer T1 to pins BB_I+ and BB_I-, as highlighted. This also applies for VR4, T2, and pins BB_Q+ and BB_Q-. With this configuration, the same voltage will be applied to BB_I+ and BB_I- and the same voltage will be applied to BB_Q+ and BB_Q-. The I and Q common mode voltages may be different from each other to null LO (carrier) leakage.
Note: VCC connection on evaluation board is VDD
Power Supply on the datasheet.

VDD connection on evaluation board is used to set baseband pin common mode (CM) voltage (see schematic)
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