Description

The F1490 is a high gain, two-stage RF Amplifier designed to operate within the 1.8GHz to 6.4GHz frequency range. Using a single 5V power supply, the F1490 provides two selectable gain modes (35.5dB and 39.5dB), 2.5dB of Noise Figure and 24dBm OP1dB at 2.6GHz.

The F1490 is packaged in a 3 × 3 mm, 16-pin VFQFPN package, with matched 50Ω input and output impedances for ease of integration into the signal path.

Competitive Advantage

- Combines a two-stage RF amplifier in a single, compact 3 × 3 mm QFN package
- Excellent performance over exceptionally wide bandwidths
- Two selectable gain modes
- Low current consumption

Features

- RF range: 1.8GHz to 6.4GHz
- 39.5dB typical gain at 2.6GHz in high gain mode
- 35.5dB typical gain at 2.6GHz in low gain mode
- 2.5dB NF at 2.6GHz
- 50Ω single-ended input and output impedances
- 5V power supply
- 75mA quiescent current consumption
- 1.8V logic compatible Standby Mode for power savings
- Operating temperature (T_{EPA}) range: -40°C to +115°C
- 3 × 3 mm 16-VFQFPN package

Typical Applications

- 5G Sub-6GHz massive MIMO
- Wireless infrastructure base stations
- FDD or TDD systems
- Point-to-point infrastructure
- Public safety infrastructure
- Military handhelds
- Repeaters and DAS
- General purpose RF

Block Diagram

Figure 1. Block Diagram
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Pin Assignments

Figure 2. Pin Assignments – Top View
## Pin Descriptions

### Table 1. Pin Descriptions

<table>
<thead>
<tr>
<th>Number</th>
<th>Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1, 5, 6, 7, 8, 9, 12</td>
<td>NC</td>
<td>No internal connection. These pins can be left unconnected, or be connected to ground (recommended). Use a via as close to the pin as possible if grounded.</td>
</tr>
<tr>
<td>2</td>
<td>RFIN</td>
<td>RF input internally matched to 50Ω. Must use an external DC block.</td>
</tr>
<tr>
<td>3</td>
<td>GND</td>
<td>Internally grounded. This pin can be left unconnected, or it can be connected to ground (recommended).</td>
</tr>
<tr>
<td>4</td>
<td>VDD</td>
<td>Pull up to VDD through inductor and use bypass capacitors as close to the pin as possible. In addition to supplying the device with a DC voltage, there is also an RF signal present.</td>
</tr>
<tr>
<td>10, 11</td>
<td>RFOUT</td>
<td>RF output. Pull up to VDD through inductor. Must use external DC block.</td>
</tr>
<tr>
<td>13</td>
<td>BIAS_2</td>
<td>Connect via resistor to a common VDD and use bypass capacitors. Place network as close to the pin as possible.</td>
</tr>
<tr>
<td>14</td>
<td>BIAS_1</td>
<td>Connect via resistor to a common VDD and use bypass. Place network as close to the pin as possible.</td>
</tr>
<tr>
<td>15</td>
<td>GAIN_SEL</td>
<td>Gain Selection pin. Logic HIGH selects High Gain Mode operation. Logic LOW (or if the pin is left unconnected or grounded) selects Low Gain Mode operation. Pin is 1.8V logic compatible.</td>
</tr>
<tr>
<td>16</td>
<td>STBY</td>
<td>Standby pin. With Logic LOW applied to this pin, the amplifier is powered off. With Logic HIGH applied to this pin (or if the pin is left unconnected), the part is in full operation mode. Pin is 1.8V logic compatible.</td>
</tr>
<tr>
<td>—</td>
<td>EPAD</td>
<td>Exposed Pad. Internally connected to ground. Solder this exposed pad to a PCB pad that uses multiple ground vias to provide heat transfer out of the device into the PCB ground planes. These multiple ground vias are also required to achieve the noted RF performance.</td>
</tr>
</tbody>
</table>
**Absolute Maximum Ratings**

Stresses above those listed below may cause permanent damage to the device. Functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**Table 2. Absolute Maximum Ratings**

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Minimum</th>
<th>Maximum</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>VDD to GND</td>
<td>VDD</td>
<td>-0.3</td>
<td>+6.0</td>
<td>V</td>
</tr>
<tr>
<td>STBY</td>
<td>VCTL</td>
<td>-0.3</td>
<td>Lower of (5.0, VDD + 0.25)</td>
<td>V</td>
</tr>
<tr>
<td>BIAS_1 (into pin)</td>
<td>IBIAS_1</td>
<td>1.5 mA</td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td>BIAS_2 (out of pin)</td>
<td>IBIAS_2</td>
<td>3 mA</td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td>RFIN externally applied DC voltage</td>
<td>VRFIN</td>
<td>-0.5</td>
<td>+0.5</td>
<td>V</td>
</tr>
<tr>
<td>RFOUT externally applied DC voltage</td>
<td>VRFOUT</td>
<td>-0.5</td>
<td>+8</td>
<td>V</td>
</tr>
<tr>
<td>Maximum CW Input Power applied for 24 hours. VDD = 5V, TEPAD = 115°C, input / output VSWR &lt; 2:1 based on a 50Ω system. Standby = logic HIGH: ON state.</td>
<td>PMAX_IN_ON</td>
<td>22 dBm</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Maximum CW Input Power applied for 24 hour. VDD = 5V, TEPAD = 115°C, input / output VSWR &lt; 2:1 based on a 50Ω system. Standby = logic LOW: OFF state.</td>
<td>PMAX_IN_OFF</td>
<td>22 dBm</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Junction Temperature</td>
<td>TMAX</td>
<td>150</td>
<td></td>
<td>°C</td>
</tr>
<tr>
<td>Storage Temperature Range</td>
<td>Tst</td>
<td>-65</td>
<td>150</td>
<td>°C</td>
</tr>
<tr>
<td>Lead Temperature (soldering, 10s)</td>
<td></td>
<td></td>
<td>260</td>
<td>°C</td>
</tr>
<tr>
<td>ElectroStatic Discharge – HBM (JEDEC/ESDA JS-001-2012)</td>
<td>VESDHBM</td>
<td>1000</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>ElectroStatic Discharge – CDM (JEDEC 22-C101F)</td>
<td>VESDCDM</td>
<td>500</td>
<td></td>
<td>V</td>
</tr>
</tbody>
</table>

[a] Exposure to these maximum RF levels can result in significantly higher Idd current draw due to overdriving the amplifier stages.
### Recommended Operating Conditions

Table 3. Recommended Operating Conditions

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Condition</th>
<th>Minimum</th>
<th>Typical</th>
<th>Maximum</th>
<th>Unit</th>
</tr>
</thead>
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<tr>
<td>Power Supply Voltage</td>
<td>$V_{DD}$</td>
<td></td>
<td>4.75</td>
<td>5</td>
<td>5.25</td>
<td>V</td>
</tr>
<tr>
<td>Operating Temperature Range</td>
<td>$T_{EPAD}$</td>
<td>Exposed Paddle</td>
<td>-40</td>
<td>+115</td>
<td></td>
<td>°C</td>
</tr>
<tr>
<td>RF Frequency Range</td>
<td>$f_{RF}$</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>GHz</td>
</tr>
<tr>
<td></td>
<td></td>
<td>2GHz Tuning Set</td>
<td>1.8</td>
<td>2.2</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>2.5GHz Tuning Set</td>
<td>2.3</td>
<td>2.7</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>3.55GHz Tuning Set</td>
<td>3.3</td>
<td>3.8</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>4.0GHz Tuning Set</td>
<td>3.8</td>
<td>4.2</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>4.7GHz Tuning Set</td>
<td>4.4</td>
<td>5.0</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>6.0GHz Tuning Set</td>
<td>5.92</td>
<td>6.26</td>
<td></td>
<td></td>
</tr>
<tr>
<td>RFIN Port Impedance</td>
<td>$Z_{RFI}$</td>
<td>Single Ended</td>
<td>50</td>
<td></td>
<td></td>
<td>Ω</td>
</tr>
<tr>
<td>RFIN Port Impedance</td>
<td>$Z_{RFO}$</td>
<td>Single Ended</td>
<td>50</td>
<td></td>
<td></td>
<td>Ω</td>
</tr>
</tbody>
</table>

[a] Using external matching, gain flatness is optimized from 1.8GHz to 2.2GHz (2GHz Tuning Set), 2.3GHz to 2.7GHz (2.5GHz Tuning Set), 3.3GHz to 3.8GHz (3.55GHz Tuning Set), 3.8GHz to 4.2GHz (4.0GHz Tuning Set), 4.4GHz to 5.0GHz (4.7GHz Tuning Set), and 5.92GHz to 6.26GHz (6.0GHz Tuning Set).

### Electrical Characteristics – General

Specifications apply when operated as a TX amplifier with tuning optimized for desired band of interest, $V_{DD} = +5.0V$, $T_{EPAD} = +25°C$, STBY = HIGH, $Z_S = Z_L = 50\Omega$, Evaluation Kit trace and connector losses are de-embedded, unless otherwise stated.

Table 4. Electrical Characteristics – General

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Condition</th>
<th>Minimum</th>
<th>Typical</th>
<th>Maximum</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Logic Input High</td>
<td>$V_{IH}$</td>
<td></td>
<td></td>
<td>$V_{DD}$</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>Logic Input Low</td>
<td>$V_{IL}$</td>
<td></td>
<td>$1.17[^a]$</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Logic Current</td>
<td>$I_{IH, IL}$</td>
<td>STBY pin, $V_{CTL} = 1.8 , V$</td>
<td>40</td>
<td></td>
<td></td>
<td>µA</td>
</tr>
<tr>
<td>Quiescent Current[^b]</td>
<td>$I_{DD, QH}$</td>
<td>High Gain Mode</td>
<td>75</td>
<td>98</td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td></td>
<td>$I_{DD, QL}$</td>
<td>Low Gain Mode</td>
<td>75</td>
<td>98</td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td>Standby Current</td>
<td>$I_{DD, STBY}$</td>
<td>STBY = LOW</td>
<td>2.5</td>
<td></td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td>Standby Switching Time</td>
<td>$t_{ON}$</td>
<td>50% STBY control to within 0.5dB of the on-state final gain value</td>
<td>250</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td>$t_{OFF}$</td>
<td>50% STBY control to $I_{DD} &lt; 10mA$</td>
<td>250</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

[^a] Specifications in the minimum/maximum columns that are shown in **bold italics** are confirmed by test. Specifications in these columns that are not shown in bold italics are confirmed by design characterization.

[^b] $I_{DD}$ refers to the nominal small signal bias current.
# Electrical Characteristics – 1.8GHz to 2.2GHz

Specifications apply when operated as a TX amplifier with tuning optimized for the 1.8GHz to 2.2GHz band, $V_{DD} = +5.0V$, $f_{RF} = 2.0GHz$, $T_{EPA} = +25°C$, $GAIN\_SEL = LOW$, $STBY = HIGH$, $Z_S = Z_L = 50\Omega$, Evaluation Kit trace and connector losses are de-embedded, unless otherwise stated.

## Table 5. Electrical Characteristics – 1.8GHz to 2.2GHz (Low Gain Mode unless Otherwise Specified)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Condition</th>
<th>Minimum</th>
<th>Typical</th>
<th>Maximum</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Gain</td>
<td>$G$</td>
<td>Low Gain Mode</td>
<td>35</td>
<td></td>
<td></td>
<td>dB</td>
</tr>
<tr>
<td></td>
<td></td>
<td>High Gain Mode</td>
<td>39</td>
<td></td>
<td></td>
<td>dB</td>
</tr>
<tr>
<td>Gain Flatness</td>
<td>$G_{FLAT}$</td>
<td>$f_{RF} = 1.8GHz to 2.2GHz$</td>
<td>1.3</td>
<td></td>
<td></td>
<td>dB</td>
</tr>
<tr>
<td>Gain Variation Over Temperature</td>
<td>$G_{TEMP}$</td>
<td>$T_{EPA} = -40°C to +115°C,$</td>
<td>$+0.8 / -0.3$</td>
<td></td>
<td></td>
<td>dB</td>
</tr>
<tr>
<td>STBY Mode Gain</td>
<td>$G_{STBY}$</td>
<td>$STBY = logic LOW$</td>
<td>-40</td>
<td></td>
<td></td>
<td>dB</td>
</tr>
<tr>
<td>RF Input Return Loss</td>
<td>$RL_{FIN}$</td>
<td>$f_{RF} = 1.8GHz to 2.2GHz$</td>
<td>21</td>
<td></td>
<td></td>
<td>dB</td>
</tr>
<tr>
<td>RF Output Return Loss</td>
<td>$RL_{OUT}$</td>
<td>$f_{RF} = 1.8GHz to 2.2GHz$</td>
<td>8</td>
<td></td>
<td></td>
<td>dB</td>
</tr>
<tr>
<td>Reverse Isolation</td>
<td>$ISO_{REV}$</td>
<td></td>
<td>55</td>
<td></td>
<td></td>
<td>dB</td>
</tr>
<tr>
<td>Noise Figure</td>
<td>$NF$</td>
<td></td>
<td>2.5</td>
<td></td>
<td></td>
<td>dB</td>
</tr>
<tr>
<td>Output Third Order Intercept Point</td>
<td>$OIP3$</td>
<td>$P_{OUT} = +4dBm / tone$ 1MHz tone separation</td>
<td>37</td>
<td></td>
<td></td>
<td>dBm</td>
</tr>
<tr>
<td>Output 1dB Compression Point</td>
<td>$OP1dB$</td>
<td></td>
<td>24</td>
<td></td>
<td></td>
<td>dBm</td>
</tr>
</tbody>
</table>
Electrical Characteristics – 2.3GHz to 2.7GHz

Specifications apply when operated as a TX amplifier with tuning optimized for the 2.3GHz to 2.7GHz band, \( V_{DD} = +5.0V \), \( f_{RF} = 2.6GHz \), \( T_{EPAD} = +25°C \), \( \text{GAIN\_SEL} = \text{LOW} \), \( \text{STBY} = \text{HIGH} \), \( Z_S = Z_L = 50\Omega \), Evaluation Kit trace and connector losses are de-embedded, unless otherwise stated.

Table 6. Electrical Characteristics – 2.3GHz to 2.7GHz (Low Gain Mode unless Otherwise Specified)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Condition</th>
<th>Minimum</th>
<th>Typical</th>
<th>Maximum</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Gain</td>
<td>G</td>
<td>Low Gain Mode</td>
<td>33[^a]</td>
<td>35.5</td>
<td></td>
<td>dB</td>
</tr>
<tr>
<td></td>
<td></td>
<td>High Gain Mode</td>
<td></td>
<td>39.5</td>
<td></td>
<td>dB</td>
</tr>
<tr>
<td>Gain Flatness</td>
<td>G_FLAT</td>
<td>( f_{RF} = 2.3GHz ) to ( 2.7GHz )</td>
<td>0.7</td>
<td></td>
<td></td>
<td>dB</td>
</tr>
<tr>
<td>Gain Variation Over Temperature</td>
<td>G_TEMP</td>
<td>( T_{EPAD} = -40°C ) to ( +115°C ), referenced to ( T_{EPAD} = 25°C )</td>
<td>+1.5 / -1.0</td>
<td></td>
<td></td>
<td>dB</td>
</tr>
<tr>
<td>STBY Mode Gain</td>
<td>G_STBY</td>
<td>STBY = logic LOW</td>
<td>-39</td>
<td></td>
<td></td>
<td>dB</td>
</tr>
<tr>
<td>RF Input Return Loss</td>
<td>R_L_FIN</td>
<td>( f_{RF} = 2.3GHz ) to ( 2.7GHz )</td>
<td>18</td>
<td></td>
<td></td>
<td>dB</td>
</tr>
<tr>
<td>RF Output Return Loss</td>
<td>R_L_FOUT</td>
<td>( f_{RF} = 2.3GHz ) to ( 2.7GHz )</td>
<td>12</td>
<td></td>
<td></td>
<td>dB</td>
</tr>
<tr>
<td>Reverse Isolation</td>
<td>ISO_REV</td>
<td></td>
<td>55</td>
<td></td>
<td></td>
<td>dB</td>
</tr>
<tr>
<td>Noise Figure</td>
<td>NF</td>
<td></td>
<td>2.5</td>
<td></td>
<td></td>
<td>dB</td>
</tr>
<tr>
<td>Output Third Order Intercept Point</td>
<td>OIP3</td>
<td>( P_{OUT} = +4dBm ) / tone 1MHz tone separation</td>
<td></td>
<td>38</td>
<td></td>
<td>dBm</td>
</tr>
<tr>
<td></td>
<td></td>
<td>( P_{OUT} = +4dBm ) / tone 1MHz tone separation ( V_{DD} = 4.75V ) to ( 5.25V ) ( T_{EPAD} = -40°C ) to ( +115°C )</td>
<td></td>
<td>30</td>
<td></td>
<td>dBm</td>
</tr>
<tr>
<td>Output 1dB Compression Point</td>
<td>OP_1dB</td>
<td>( V_{DD} = 4.75V ) to ( 5.25V ) ( T_{EPAD} = -40°C ) to ( +115°C )</td>
<td></td>
<td>24</td>
<td></td>
<td>dBm</td>
</tr>
</tbody>
</table>

[^a]: Specifications in the minimum/maximum columns that are shown in bold italics are confirmed by test. Specifications in these columns that are not shown in bold italics are confirmed by design characterization.
Electrical Characteristics – 3.3GHz to 3.8GHz

Specifications apply when operated as a TX amplifier with tuning optimized for the 3.3GHz to 3.8GHz band, \( V_{DD} = +5.0\text{V} \), \( f_{\text{ref}} = 3.55\text{GHz} \), \( T_{\text{E PAD}} = +25^\circ\text{C} \), GAIN_SEL = LOW, STBY = HIGH, \( Z_S = Z_L = 50\Omega \), Evaluation Kit trace and connector losses are de-embedded, unless otherwise stated.

Table 7. Electrical Characteristics – 3.3GHz to 3.8GHz (Low Gain Mode unless Otherwise Specified)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Condition</th>
<th>Minimum</th>
<th>Typical</th>
<th>Maximum</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Gain</td>
<td>G</td>
<td>Low Gain Mode</td>
<td>36</td>
<td></td>
<td></td>
<td>dB</td>
</tr>
<tr>
<td></td>
<td></td>
<td>High Gain Mode</td>
<td>40</td>
<td></td>
<td></td>
<td>dB</td>
</tr>
<tr>
<td>Gain Flatness</td>
<td>G_{FLAT}</td>
<td>( f_{RF} = 3.3\text{GHz to 3.8GHz} )</td>
<td>0.7</td>
<td></td>
<td></td>
<td>dB</td>
</tr>
<tr>
<td>Gain Variation Over Temperature</td>
<td>G_{TEMP}</td>
<td>( T_{\text{E PAD}} = -40^\circ\text{C to } +115^\circ\text{C, referenced to } T_{\text{E PAD}} = 25^\circ\text{C} )</td>
<td>+1.9 / -1.7</td>
<td></td>
<td></td>
<td>dB</td>
</tr>
<tr>
<td>STBY Mode Gain</td>
<td>G_{STBY}</td>
<td>STBY = logic LOW</td>
<td>-43</td>
<td></td>
<td></td>
<td>dB</td>
</tr>
<tr>
<td>RF Input Return Loss</td>
<td>RL_{FIN}</td>
<td>( f_{RF} = 3.3\text{GHz to 3.8GHz} )</td>
<td>11</td>
<td></td>
<td></td>
<td>dB</td>
</tr>
<tr>
<td>RF Output Return Loss</td>
<td>RL_{RFOUT}</td>
<td>( f_{RF} = 3.3\text{GHz to 3.8GHz} )</td>
<td>10</td>
<td></td>
<td></td>
<td>dB</td>
</tr>
<tr>
<td>Reverse Isolation</td>
<td>ISO_{REV}</td>
<td></td>
<td>55</td>
<td></td>
<td></td>
<td>dB</td>
</tr>
<tr>
<td>Noise Figure</td>
<td>NF</td>
<td></td>
<td>2.8</td>
<td></td>
<td></td>
<td>dB</td>
</tr>
<tr>
<td>Output Third Order Intercept Point</td>
<td>OIP3</td>
<td>( P_{\text{OUT}} = +4\text{dBm} / \text{tone} ) ( 1\text{MHz} ) \text{tone separation}</td>
<td>34</td>
<td></td>
<td></td>
<td>dBm</td>
</tr>
<tr>
<td>Output 1dB Compression Point</td>
<td>OP1dB</td>
<td></td>
<td>23</td>
<td></td>
<td></td>
<td>dBm</td>
</tr>
</tbody>
</table>
## Electrical Characteristics – 3.8GHz to 4.2GHz

Specifications apply when operated as a TX amplifier with tuning optimized for the 3.8GHz to 4.2GHz band, VDD = +5.0V, fREF = 4GHz, TEPAD = +25°C, GAIN_SEL = LOW, STBY = HIGH, ZS = ZL = 50Ω, Evaluation Kit trace and connector losses are de-embedded, unless otherwise stated.

### Table 8. Electrical Characteristics – 3.8GHz to 4.2GHz (Low Gain Mode unless Otherwise Specified)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Condition</th>
<th>Minimum</th>
<th>Typical</th>
<th>Maximum</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Gain</td>
<td>G</td>
<td>Low Gain Mode</td>
<td>35</td>
<td></td>
<td></td>
<td>dB</td>
</tr>
<tr>
<td></td>
<td></td>
<td>High Gain Mode</td>
<td>40</td>
<td></td>
<td></td>
<td>dB</td>
</tr>
<tr>
<td>Gain Flatness</td>
<td>GFLAT</td>
<td>fREF = 3.8GHz to 4.2GHz</td>
<td>2.4</td>
<td></td>
<td></td>
<td>dB</td>
</tr>
<tr>
<td>Gain Variation Over Temperature</td>
<td>GTEMP</td>
<td>TEPAD = -40°C to +115°C, referenced to TEPAD = 25°C</td>
<td>+2.6 / -2.2</td>
<td></td>
<td></td>
<td>dB</td>
</tr>
<tr>
<td>STBY Mode Gain</td>
<td>GSTBY</td>
<td>STBY = logic LOW</td>
<td>-45</td>
<td></td>
<td></td>
<td>dB</td>
</tr>
<tr>
<td>RF Input Return Loss</td>
<td>RLFIN</td>
<td>fREF = 3.8GHz to 4.2GHz</td>
<td>8</td>
<td></td>
<td></td>
<td>dB</td>
</tr>
<tr>
<td>RF Output Return Loss</td>
<td>RLRFOUT</td>
<td>fREF = 3.8GHz to 4.2GHz</td>
<td>7</td>
<td></td>
<td></td>
<td>dB</td>
</tr>
<tr>
<td>Reverse Isolation</td>
<td>ISOREV</td>
<td></td>
<td>51</td>
<td></td>
<td></td>
<td>dB</td>
</tr>
<tr>
<td>Noise Figure</td>
<td>NF</td>
<td></td>
<td>3.5</td>
<td></td>
<td></td>
<td>dB</td>
</tr>
<tr>
<td>Output Third Order Intercept Point</td>
<td>OIP3</td>
<td>POUT = +4dBm / tone 1MHz tone separation</td>
<td>35</td>
<td></td>
<td></td>
<td>dBm</td>
</tr>
<tr>
<td>Output 1dB Compression Point</td>
<td>OP1dB</td>
<td></td>
<td>24</td>
<td></td>
<td></td>
<td>dBm</td>
</tr>
</tbody>
</table>
Electrical Characteristics – 4.4GHz to 5GHz

Specifications apply when operated as a TX amplifier with tuning optimized for the 4.4GHz to 5GHz band, \( V_{DD} = +5.0\text{V}, f_{RF} = 4.7\text{GHz}, T_{EPAD} = +25\text{°C}, \text{GAIN\_SEL} = \text{LOW}, \text{STBY} = \text{HIGH}, Z_S = Z_L = 50\text{Ω}, \) Evaluation Kit trace and connector losses are de-embedded, unless otherwise stated.

Table 9. Electrical Characteristics – 4.4GHz to 5GHz (Low Gain Mode unless Otherwise Specified)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Condition</th>
<th>Minimum</th>
<th>Typical</th>
<th>Maximum</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Gain</td>
<td>G</td>
<td>Low Gain Mode</td>
<td>34</td>
<td></td>
<td></td>
<td>dB</td>
</tr>
<tr>
<td></td>
<td></td>
<td>High Gain Mode</td>
<td>40</td>
<td></td>
<td></td>
<td>dB</td>
</tr>
<tr>
<td>Gain Flatness</td>
<td>G_FLAT</td>
<td>( f_{RF} = 4.4\text{GHz} ) to 5GHz</td>
<td>2.5</td>
<td></td>
<td></td>
<td>dB</td>
</tr>
<tr>
<td>Gain Variation Over Temperature</td>
<td>G_TEMP</td>
<td>( T_{EPAD} = -40\text{°C} ) to +115\text{°C}, referenced to ( T_{EPAD} = 25\text{°C} )</td>
<td>+2.6 / -2.3</td>
<td></td>
<td></td>
<td>dB</td>
</tr>
<tr>
<td>STBY Mode Gain</td>
<td>G_STBY</td>
<td>STBY = logic LOW</td>
<td>-40</td>
<td></td>
<td></td>
<td>dB</td>
</tr>
<tr>
<td>RF Input Return Loss</td>
<td>R_LFIN</td>
<td>( f_{RF} = 4.4\text{GHz} ) to 5GHz</td>
<td>7</td>
<td></td>
<td></td>
<td>dB</td>
</tr>
<tr>
<td>RF Output Return Loss</td>
<td>R_LRFOUT</td>
<td>( f_{RF} = 4.4\text{GHz} ) to 5GHz</td>
<td>5</td>
<td></td>
<td></td>
<td>dB</td>
</tr>
<tr>
<td>Reverse Isolation</td>
<td>ISO_REV</td>
<td></td>
<td>49</td>
<td></td>
<td></td>
<td>dB</td>
</tr>
<tr>
<td>Noise Figure</td>
<td>NF</td>
<td></td>
<td>3.4</td>
<td></td>
<td></td>
<td>dB</td>
</tr>
<tr>
<td>Output Third Order Intercept Point</td>
<td>O_I_P3</td>
<td>( P_{OUT} = +4\text{dBm} / \text{tone} ) 1MHz tone separation</td>
<td>34</td>
<td></td>
<td></td>
<td>dBm</td>
</tr>
<tr>
<td>Output 1dB Compression Point</td>
<td>O_P1_dB</td>
<td></td>
<td>24</td>
<td></td>
<td></td>
<td>dBm</td>
</tr>
</tbody>
</table>
Electrical Characteristics – 5.92GHz to 6.26GHz

Specifications apply when operated as a TX amplifier with tuning optimized for the 5.92GHz to 6.26GHz band, V\text{DD} = +5.0V, f\text{RF} = 6.0GHz, T\text{EPAD} = +25°C, GAIN\_SEL = HIGH, STBY = HIGH, Z\text{S} = Z\text{L} = 50\Omega, Evaluation Kit trace and connector losses are deembedded, unless otherwise stated. Specifications shown for 5.92GHz to 6.26GHz require accommodating additional shunt component at RFIN (pin 2 port). See Figure 95. Electrical Schematic for 5.92GHz - 6.26GHz BOM.

**Table 10. Electrical Characteristics – 5.92GHz to 6.26GHz (High Gain Mode unless Otherwise Specified)**

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Condition</th>
<th>Minimum</th>
<th>Typical</th>
<th>Maximum</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Gain</td>
<td>G</td>
<td>High Gain Mode</td>
<td>33</td>
<td></td>
<td></td>
<td>dB</td>
</tr>
<tr>
<td>Gain Flatness</td>
<td>G_FLAT</td>
<td>f\text{RF} = 5.92GHz to 6.26GHz</td>
<td>2.8</td>
<td></td>
<td></td>
<td>dB</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Each 100MHz subrange within the specified frequency range</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Gain Variation Over Temperature</td>
<td>G_TEMP</td>
<td>T\text{EPAD} = -40°C to +115°C, referenced to T\text{EPAD} = 25°C</td>
<td>+2.2</td>
<td>-2.1</td>
<td></td>
<td>dB</td>
</tr>
<tr>
<td>STBY Mode Gain</td>
<td>G_STBY</td>
<td>STBY = logic LOW</td>
<td>-34</td>
<td></td>
<td></td>
<td>dB</td>
</tr>
<tr>
<td>RF Input Return Loss</td>
<td>RL_RFIN</td>
<td>f\text{RF} = 5.92GHz to 6.26GHz</td>
<td>10</td>
<td></td>
<td></td>
<td>dB</td>
</tr>
<tr>
<td>RF Output Return Loss</td>
<td>RL_RFOUT</td>
<td>f\text{RF} = 5.92GHz to 6.26GHz</td>
<td>12</td>
<td></td>
<td></td>
<td>dB</td>
</tr>
<tr>
<td>Reverse Isolation</td>
<td>ISO_REV</td>
<td></td>
<td>44</td>
<td></td>
<td></td>
<td>dB</td>
</tr>
<tr>
<td>Noise Figure</td>
<td>NF</td>
<td></td>
<td>4.6</td>
<td></td>
<td></td>
<td>dB</td>
</tr>
<tr>
<td>Output Third Order Intercept Point</td>
<td>O_IP3</td>
<td>P\text{OUT} = +4dBm / tone 1MHz tone separation</td>
<td>33.5</td>
<td></td>
<td></td>
<td>dBm</td>
</tr>
<tr>
<td>Output 1dB Compression Point</td>
<td>OP_1dB</td>
<td></td>
<td>22.5</td>
<td></td>
<td></td>
<td>dBm</td>
</tr>
</tbody>
</table>

**Thermal Characteristics**

**Table 11. Package Thermal Characteristics**

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Value</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Junction to Ambient Thermal Resistance</td>
<td>\theta_{\text{JA}}</td>
<td>55.2</td>
<td>°C/W</td>
</tr>
<tr>
<td>Junction to Case Thermal Resistance. (Case is defined as the exposed paddle)</td>
<td>\theta_{\text{JC_BOT}}</td>
<td>8.175</td>
<td>°C/W</td>
</tr>
<tr>
<td>Moisture Sensitivity Rating (Per J-STD-020)</td>
<td></td>
<td>MSL 1</td>
<td></td>
</tr>
</tbody>
</table>
Typical Operating Conditions

Unless otherwise stated the typical operating graphs were measured under the following conditions:

- $V_{DD} = 5.0V$
- STBY = HIGH
- GAIN_SEL = LOW
- $T_{EPAD} = +25^\circ C$
- $f_{RF} = 2.0GHz$
- $f_{RF} = 2.6GHz$
- $f_{RF} = 3.55GHz$
- $f_{RF} = 4.0GHz$
- $f_{RF} = 4.7GHz$
- $f_{RF} = 6.0GHz$
- $Z_S = Z_L = 50\Omega$ Single Ended
- $P_{out} = 4dBm/tone$ and $1MHz$ Tone Spacing for OIP3
Typical Performance Characteristics (Band 2p0 – 1.8GHz to 2GHz)

Figure 3. Gain - Low Gain Mode

![Gain - Low Gain Mode](image1)

Figure 4. Gain - High Gain Mode

![Gain - High Gain Mode](image2)

Figure 5. Input Return Loss - Low Gain Mode

![Input Return Loss - Low Gain Mode](image3)

Figure 6. Input Return Loss - High Gain Mode

![Input Return Loss - High Gain Mode](image4)

Figure 7. Output Return Loss - Low Gain Mode

![Output Return Loss - Low Gain Mode](image5)

Figure 8. Output Return Loss - High Gain Mode

![Output Return Loss - High Gain Mode](image6)
Figure 15. Output IP3 - Low Gain Mode

Figure 16. Output IP3 - High Gain Mode

Figure 17. Output P1dB - Low Gain Mode

Figure 18. Output P1dB - High Gain Mode
Typical Performance Characteristics (Band 2p5 – 2.3GHz to 2.7GHz)

Figure 19. Gain - Low Gain Mode

Figure 20. Gain - High Gain Mode

Figure 21. Input Return Loss - Low Gain Mode

Figure 22. Input Return Loss - High Gain Mode

Figure 23. Output Return Loss - Low Gain Mode

Figure 24. Output Return Loss - High Gain Mode
Figure 25. Reverse Isolation - Low Gain Mode

Figure 26. Reverse Isolation - High Gain Mode

Figure 27. Standby Mode Gain

Figure 28. Current versus Power Supply Voltage

Figure 29. Noise Figure - Low Gain Mode

Figure 30. Noise Figure - High Gain Mode
Figure 31. Output IP3 - Low Gain Mode

Figure 32. Output IP3 - High Gain Mode

Figure 33. Output P1dB - Low Gain Mode

Figure 34. Output P1dB - High Gain Mode
Typical Performance Characteristics (Band 3p55 – 3.3GHz to 3.8GHz)

Figure 35. Gain - Low Gain Mode

Figure 36. Gain - High Gain Mode

Figure 37. Input Return Loss - Low Gain Mode

Figure 38. Input Return Loss - High Gain Mode

Figure 39. Output Return Loss - Low Gain Mode

Figure 40. Output Return Loss – High Gain Mode
Figure 47. Output IP3 - Low Gain Mode

Figure 48. Output IP3 - High Gain Mode

Figure 49. Output P1dB - Low Gain Mode

Figure 50. Output P1dB - High Gain Mode
Typical Performance Characteristics (Band 3p8 – 3.8GHz to 4.2GHz)

Figure 51. Gain - Low Gain Mode

Figure 52. Gain - High Gain Mode

Figure 53. Input Return Loss - Low Gain Mode

Figure 54. Input Return Loss - High Gain Mode

Figure 55. Output Return Loss - Low Gain Mode

Figure 56. Output Return Loss – High Gain Mode
Figure 57. Reverse Isolation - Low Gain Mode

Figure 58. Reverse Isolation - High Gain Mode

Figure 59. Standby Mode Gain

Figure 60. Current versus Power Supply Voltage

Figure 61. Noise Figure - Low Gain Mode

Figure 62. Noise Figure - High Gain Mode
Figure 63. Output IP3 - Low Gain Mode

Figure 64. Output IP3 - High Gain Mode

Figure 65. Output P1dB - Low Gain Mode

Figure 66. Output P1dB - High Gain Mode
Typical Performance Characteristics (Band 4p7 – 4.4GHz to 5GHz)

Figure 67. Gain - Low Gain Mode

Figure 68. Gain - High Gain Mode

Figure 69. Input Return Loss - Low Gain Mode

Figure 70. Input Return Loss - High Gain Mode

Figure 71. Output Return Loss - Low Gain Mode

Figure 72. Output Return Loss – High Gain Mode
Figure 73. Reverse Isolation - Low Gain Mode

Figure 74. Reverse Isolation - High Gain Mode

Figure 75. Standby Mode Gain

Figure 76. Current versus Power Supply Voltage

Figure 77. Noise Figure - Low Gain Mode

Figure 78. Noise Figure - High Gain Mode
Typical Performance Characteristics (Band 6p0 – 5.92GHz to 6.26GHz)

Figure 83. Gain - High Gain Mode

Figure 84. Input Return Loss - High Gain Mode

Figure 85. Output Return Loss – High Gain Mode

Figure 86. Reverse Isolation - High Gain Mode

Figure 87. Standby Mode Gain

Figure 88. Current versus Power Supply Voltage
Figure 89. Noise Figure - High Gain Mode

Figure 90. Output IP3 - High Gain Mode

Figure 91. Output P1dB - High Gain Mode
Functional Description

Standby
The F1490 can be turned off for low current consumption. This is done by applying a logic voltage to pin 16 using the following table.

Table 12. Standby Truth Table

<table>
<thead>
<tr>
<th>STBY</th>
<th>Condition</th>
</tr>
</thead>
<tbody>
<tr>
<td>Logic HIGH / NC</td>
<td>Full operation</td>
</tr>
<tr>
<td>Logic LOW</td>
<td>Amplifier OFF</td>
</tr>
</tbody>
</table>

Gain Selection
The F1490 can be selected to be in a High Gain Mode or Low Gain Mode operation. This is done by applying a logic voltage to pin 15 using the following table.

Table 13. Gain Selection Truth Table

<table>
<thead>
<tr>
<th>GAIN_SEL</th>
<th>Condition</th>
</tr>
</thead>
<tbody>
<tr>
<td>Logic HIGH</td>
<td>High Gain Mode</td>
</tr>
<tr>
<td>Logic LOW / NC</td>
<td>Low Gain Mode</td>
</tr>
</tbody>
</table>
Evaluation Kit Picture

Figure 92. Evaluation Kit: Top View

Figure 93. Evaluation Kit: Bottom View
Evaluation Board Schematic

Figure 94. Electrical Schematic
# Evaluation Kit BOM – 1.8GHz to 2.2GHz

Table 14. 1.8GHz to 2.2GHz Evaluation Kit Bill of Materials (BOM)\([a]\)

<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>C1</td>
<td>1</td>
<td>1.2pF ±0.1pF, 50V, COG Surface Mount Capacitor</td>
<td>GJM1555C1H1R2BB01</td>
<td>Murata</td>
</tr>
<tr>
<td>C6</td>
<td>1</td>
<td>1.8pF ±0.1pF, 50V, COG Surface Mount Capacitor</td>
<td>GJM1555C1H1R8BB01</td>
<td>Murata</td>
</tr>
<tr>
<td>C2</td>
<td>1</td>
<td>10pF ±0.25pF, 50V, COG Surface Mount Capacitor</td>
<td>GJM1555C1H100JB01</td>
<td>Murata</td>
</tr>
<tr>
<td>C3, C7, C10, C9</td>
<td>4</td>
<td>33pF ±5%, 25V, COG Surface Mount Capacitor</td>
<td>GRM1555C1H330J</td>
<td>Murata</td>
</tr>
<tr>
<td>C4</td>
<td>1</td>
<td>0.1uF ±10%, 16V, X7R Surface Mount Capacitor</td>
<td>GRM155R71C104KA88D</td>
<td>Murata</td>
</tr>
<tr>
<td>C8</td>
<td>1</td>
<td>0.1uF ±10%, 50V, H8L Surface Mount Capacitor</td>
<td>GCM188L81H104KA57D</td>
<td>Murata</td>
</tr>
<tr>
<td>C11</td>
<td>1</td>
<td>1uF ±10%, 25V, X5R Surface Mount Capacitor</td>
<td>GRM188R61E105KA12</td>
<td>Murata</td>
</tr>
<tr>
<td>C5</td>
<td>1</td>
<td>6.8pF ±0.5pF, 50V, COG Surface Mount Capacitor</td>
<td>GJM1555C1H6R8DB01</td>
<td>Murata</td>
</tr>
<tr>
<td>C12, C13</td>
<td>2</td>
<td>DNI</td>
<td></td>
<td></td>
</tr>
<tr>
<td>R1</td>
<td>1</td>
<td>1.5kΩ ±5%, 1/10W</td>
<td>ERJ2GEJJ152</td>
<td>Panasonic</td>
</tr>
<tr>
<td>R2</td>
<td>1</td>
<td>1kΩ ±5%, 1/16W</td>
<td>ERJ2GEJJ102</td>
<td>Panasonic</td>
</tr>
<tr>
<td>R8, R9, R10</td>
<td>3</td>
<td>0Ω, 1/10W</td>
<td>ERJ2GE0R00X</td>
<td>Panasonic</td>
</tr>
<tr>
<td>L2</td>
<td>1</td>
<td>2.2nH ±0.3nH, 300mA, Surface Mount Inductor</td>
<td>LQG15HS2N2S02</td>
<td>Murata</td>
</tr>
<tr>
<td>L1</td>
<td>1</td>
<td>1.5nH ±0.3nH, 1A 100mΩ, Surface Mount Inductor</td>
<td>LQG15HN1N5S02D</td>
<td>Murata</td>
</tr>
<tr>
<td>J1, J2, J3, J4, J5</td>
<td>5</td>
<td>Connector SMA Jack STR 50ohm Edge Mount</td>
<td>142-0701-851</td>
<td>Cinch Connectivity</td>
</tr>
<tr>
<td>J6</td>
<td>1</td>
<td>DNI Headerstrip 1x2</td>
<td></td>
<td></td>
</tr>
<tr>
<td>J7</td>
<td>1</td>
<td>Headerstrip 1x10</td>
<td>0022284103</td>
<td>Molex</td>
</tr>
<tr>
<td>TP1</td>
<td>1</td>
<td>Loop, Black, Phosphor Bronze Wire Loop</td>
<td>5001</td>
<td>Keystone electronics</td>
</tr>
<tr>
<td>U1</td>
<td>1</td>
<td>F1490, GaAs Pre-Driver Amplifier</td>
<td>F1490</td>
<td>Renesas</td>
</tr>
</tbody>
</table>

\[a\] This BOM is optimized for low gain mode performance. Refer to application note for recommended high gain BOM.
## Evaluation Kit BOM – 2.3GHz to 2.7GHz

### Table 15. 2.3GHz to 2.7GHz Evaluation Kit Bill of Materials (BOM)[a]

<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>C1</td>
<td>1</td>
<td>0.8pF ±0.1pF, 50V, COG Surface Mount Capacitor</td>
<td>GJM1555C1HR80BB01D</td>
<td>Murata</td>
</tr>
<tr>
<td>C6</td>
<td>1</td>
<td>0.7pF ±0.1pF, 50V, COG Surface Mount Capacitor</td>
<td>GJM1555C1HR70BB01D</td>
<td>Murata</td>
</tr>
<tr>
<td>C2</td>
<td>1</td>
<td>10pF ±0.25pF, 50V, COG Surface Mount Capacitor</td>
<td>GJM1555C1H100JB01</td>
<td>Murata</td>
</tr>
<tr>
<td>C3, C7, C10, C9</td>
<td>4</td>
<td>33pF ±5%, 25V, COG Surface Mount Capacitor</td>
<td>GRM1555C1H330J</td>
<td>Murata</td>
</tr>
<tr>
<td>C4</td>
<td>1</td>
<td>0.1uF ±10%, 16V, X7R Surface Mount Capacitor</td>
<td>GRM155R71C104KA88D</td>
<td>Murata</td>
</tr>
<tr>
<td>C8</td>
<td>1</td>
<td>0.1uF ±10%, 50V, H8L Surface Mount Capacitor</td>
<td>GCM188L81H104KA57D</td>
<td>Murata</td>
</tr>
<tr>
<td>C11</td>
<td>1</td>
<td>1uF ±10%, 25V, X5R Surface Mount Capacitor</td>
<td>GRM188R61E105KA12</td>
<td>Murata</td>
</tr>
<tr>
<td>C5</td>
<td>1</td>
<td>22pF ±5%, 50V, COG Surface Mount Capacitor</td>
<td>GRM1555C1H220J</td>
<td>Murata</td>
</tr>
<tr>
<td>C12, C13</td>
<td>2</td>
<td>DNI</td>
<td></td>
<td></td>
</tr>
<tr>
<td>R1</td>
<td>1</td>
<td>1.5kΩ ±5%, 1/10W</td>
<td>ERJ2GEJJ152</td>
<td>Panasonic</td>
</tr>
<tr>
<td>R2</td>
<td>1</td>
<td>1kΩ ±5%, 1/16W</td>
<td>ERJ2GEJJ102</td>
<td>Panasonic</td>
</tr>
<tr>
<td>R8, R9, R10</td>
<td>3</td>
<td>0Ω, 1/10W</td>
<td>ERJ2GE0R00X</td>
<td>Panasonic</td>
</tr>
<tr>
<td>L2</td>
<td>1</td>
<td>2.2nH ±0.3nH, 300mA, Surface Mount Inductor</td>
<td>LQG15HS2N2S02</td>
<td>Murata</td>
</tr>
<tr>
<td>L1</td>
<td>1</td>
<td>1.5nH ±0.3nH, 1A 100mΩ, Surface Mount Inductor</td>
<td>LQG15HN1N5S02D</td>
<td>Murata</td>
</tr>
<tr>
<td>J1, J2, J3, J4, J5</td>
<td>5</td>
<td>Connector SMA Jack STR 50ohm Edge Mount</td>
<td>142-0701-851</td>
<td>Cinch Connectivity</td>
</tr>
<tr>
<td>J6</td>
<td>1</td>
<td>DNI Headerstrip 1x2</td>
<td></td>
<td></td>
</tr>
<tr>
<td>J7</td>
<td>1</td>
<td>Headerstrip 1x10</td>
<td>0022284103</td>
<td>Molex</td>
</tr>
<tr>
<td>TP1</td>
<td>1</td>
<td>Loop, Black, Phosphor Bronze Wire Loop</td>
<td>5001</td>
<td>Keystone Electronics</td>
</tr>
<tr>
<td>U1</td>
<td>1</td>
<td>F1490, GaAs Pre-Driver Amplifier</td>
<td>F1490</td>
<td>Renesas</td>
</tr>
</tbody>
</table>

[a] This BOM is optimized for low gain mode performance. Refer to application note for recommended high gain BOM.
## Evaluation Kit BOM – 3.3GHz to 3.8GHz

### Table 16. 3.3GHz to 3.8GHz Evaluation Kit Bill of Materials (BOM)\[a]\[

<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>C1</td>
<td>1</td>
<td>0.8pF ±0.1pF, 50V, COG Surface Mount Capacitor</td>
<td>GJM1555C1HR80BB01D</td>
<td>Murata</td>
</tr>
<tr>
<td>C6 (inductor)</td>
<td>1</td>
<td>4.3nH ±0.3nH, COG Surface Mount Capacitor</td>
<td>LQG15HS4N3S02D</td>
<td>Murata</td>
</tr>
<tr>
<td>C2</td>
<td>1</td>
<td>6pF ±5%, 50V, COG Surface Mount Capacitor</td>
<td>GJM1555C1H6R0BB01</td>
<td>Murata</td>
</tr>
<tr>
<td>C3, C7, C10, C9</td>
<td>4</td>
<td>33pF ±5%, 25V, COG Surface Mount Capacitor</td>
<td>GRM1555C1H330J</td>
<td>Murata</td>
</tr>
<tr>
<td>C4</td>
<td>1</td>
<td>0.1uF ±10%, 16V, X7R Surface Mount Capacitor</td>
<td>GRM155R71C104KA88D</td>
<td>Murata</td>
</tr>
<tr>
<td>C8</td>
<td>1</td>
<td>0.1uF ±10%, 25V, X5R Surface Mount Capacitor</td>
<td>GCM188R71C104KA37D</td>
<td>Murata</td>
</tr>
<tr>
<td>C11</td>
<td>1</td>
<td>1uF ±10%, 25V, X5R Surface Mount Capacitor</td>
<td>GRM188R61E105KA12D</td>
<td>Murata</td>
</tr>
<tr>
<td>C5</td>
<td>1</td>
<td>1.1pF ±0.1pF, 16V, COG Surface Mount Capacitor</td>
<td>GJM1555C1H1R1BB01D</td>
<td>Murata</td>
</tr>
<tr>
<td>C12</td>
<td>1</td>
<td>DNI</td>
<td></td>
<td></td>
</tr>
<tr>
<td>C13</td>
<td>1</td>
<td>33pF ±5%, 25V, COG Surface Mount Capacitor</td>
<td>GRM0335C1E330JA01D</td>
<td>Murata</td>
</tr>
<tr>
<td>R1</td>
<td>1</td>
<td>1.8kΩ ±5%, 1/10W</td>
<td>ERJ2GEJ182</td>
<td>Panasonic</td>
</tr>
<tr>
<td>R2</td>
<td>1</td>
<td>150Ω ±5%, 1/16W</td>
<td>ERJ2GEJ151</td>
<td>Panasonic</td>
</tr>
<tr>
<td>R8, R9, R10, L1</td>
<td>3</td>
<td>0Ω, 1/10W</td>
<td>ERJ2GE0R00X</td>
<td>Panasonic</td>
</tr>
<tr>
<td>L2</td>
<td>1</td>
<td>1.8nH ±0.3nH, 300mA, Surface Mount Inductor</td>
<td>LQG15HS1N8S02</td>
<td>Murata</td>
</tr>
<tr>
<td>J1, J2, J3</td>
<td>3</td>
<td>Connector SMA Jack STR 50ohm Edge Mount</td>
<td>142-0701-851</td>
<td>Cinch Connectivity</td>
</tr>
<tr>
<td>J4, J5</td>
<td>2</td>
<td>DNI</td>
<td></td>
<td></td>
</tr>
<tr>
<td>J6</td>
<td>1</td>
<td>DNI Headerstrip 1x2</td>
<td></td>
<td></td>
</tr>
<tr>
<td>J7</td>
<td>1</td>
<td>Headerstrip 1x10</td>
<td>0022284103</td>
<td>Molex</td>
</tr>
<tr>
<td>TP1</td>
<td>1</td>
<td>Loop, Black, Phosphor Bronze Wire Loop</td>
<td>5001</td>
<td>Keystone electronics</td>
</tr>
<tr>
<td>U1</td>
<td>1</td>
<td>F1490, GaAs Pre-Driver Amplifier</td>
<td>F1490</td>
<td>Renesas</td>
</tr>
</tbody>
</table>

\[a\] This BOM is optimized for low gain mode performance. Refer to application note for recommended high gain BOM.
## Evaluation Kit BOM – 3.8GHz to 4.2GHz

Table 17. 3.8GHz to 4.2GHz Evaluation Kit Bill of Materials (BOM)[a]

<table>
<thead>
<tr>
<th></th>
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<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>C1</td>
<td>1</td>
<td>0.8pF ±0.1pF, 50V, COG Surface Mount Capacitor</td>
<td>GJM1555C1HR80B001D</td>
<td>Murata</td>
</tr>
<tr>
<td>C6</td>
<td>1</td>
<td>0.7pF ±0.1pF, 50V, COG Surface Mount Capacitor</td>
<td>GJM1555C1HR70B001D</td>
<td>Murata</td>
</tr>
<tr>
<td>C2</td>
<td>1</td>
<td>6pF ±5%, 50V, COG Surface Mount Capacitor</td>
<td>GJM1555C1H6R00B001</td>
<td>Murata</td>
</tr>
<tr>
<td>C3, C7, C10, C9</td>
<td>4</td>
<td>33pF ±5%, 25V, COG Surface Mount Capacitor</td>
<td>GRM1555C1H330J</td>
<td>Murata</td>
</tr>
<tr>
<td>C4</td>
<td>1</td>
<td>0.1uF ±10%, 16V, X7R Surface Mount Capacitor</td>
<td>GRM155R71C104KA88D</td>
<td>Murata</td>
</tr>
<tr>
<td>C8</td>
<td>1</td>
<td>0.1uF ±10%, 25V, X5R Surface Mount Capacitor</td>
<td>GCM188R71C104KA37D</td>
<td>Murata</td>
</tr>
<tr>
<td>C11</td>
<td>1</td>
<td>1uF ±10%, 25V, X5R Surface Mount Capacitor</td>
<td>GRM188R61E105KA12D</td>
<td>Murata</td>
</tr>
<tr>
<td>C5</td>
<td>1</td>
<td>22pF ±5%, 50V, COG Surface Mount Capacitor</td>
<td>GJM1555C1H20J001</td>
<td>Murata</td>
</tr>
<tr>
<td>C12</td>
<td>1</td>
<td>DNI</td>
<td></td>
<td></td>
</tr>
<tr>
<td>C13</td>
<td>1</td>
<td>33pF ±5%, 25V, COG Surface Mount Capacitor</td>
<td>GRM0335C1E330J0A1D</td>
<td>Murata</td>
</tr>
<tr>
<td>R1</td>
<td>1</td>
<td>1kΩ ±5%, 1/10W</td>
<td>ERJ2GEJ102</td>
<td>Panasonic</td>
</tr>
<tr>
<td>R2</td>
<td>1</td>
<td>150Ω ±5%, 1/16W</td>
<td>ERJ2GEJ151</td>
<td>Panasonic</td>
</tr>
<tr>
<td>R8, R9, R10, L1</td>
<td>3</td>
<td>0Ω, 1/10W</td>
<td>ERJ2GE0R00X</td>
<td>Panasonic</td>
</tr>
<tr>
<td>L2</td>
<td>1</td>
<td>1.8nH ±0.3nH, 300mA, Surface Mount Inductor</td>
<td>LQG15HS1N8S02</td>
<td>Murata</td>
</tr>
<tr>
<td>J1, J2, J3</td>
<td>3</td>
<td>Connector SMA Jack STR 50ohm Edge Mount</td>
<td>142-0701-851</td>
<td>Cinch Connectivity</td>
</tr>
<tr>
<td>J4, J5</td>
<td>2</td>
<td>DNI</td>
<td></td>
<td></td>
</tr>
<tr>
<td>J6</td>
<td>1</td>
<td>DNI Headerstrip 1x2</td>
<td></td>
<td></td>
</tr>
<tr>
<td>J7</td>
<td>1</td>
<td>Headerstrip 1x10</td>
<td>0022284103</td>
<td>Molex</td>
</tr>
<tr>
<td>TP1</td>
<td>1</td>
<td>Loop, Black, Phosphor Bronze Wire Loop</td>
<td>5001</td>
<td>Keystone electronics</td>
</tr>
<tr>
<td>U1</td>
<td>1</td>
<td>F1490, GaAs Pre-Driver Amplifier</td>
<td>F1490</td>
<td>Renesas</td>
</tr>
</tbody>
</table>

[a] This BOM is optimized for low gain mode performance. Refer to application note for recommended high gain BOM.
**Evaluation Kit BOM – 4.4GHz to 5GHz**

### Table 18. 4.4GHz to 5GHz Evaluation Kit Bill of Materials (BOM)\(^{[a]}\)

<table>
<thead>
<tr>
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</tr>
</thead>
<tbody>
<tr>
<td>C1</td>
<td>1</td>
<td>0.6pF ±0.1pF, 50V, COG Surface Mount Capacitor</td>
<td>GJM1555C1HR60BB01</td>
<td>Murata</td>
</tr>
<tr>
<td>C6</td>
<td>1</td>
<td>0.6pF ±0.1pF, 50V, COG Surface Mount Capacitor</td>
<td>GJM1555C1HR60BB01</td>
<td>Murata</td>
</tr>
<tr>
<td>C2</td>
<td>1</td>
<td>1.7pF ±0.25pF, 50V, COG Surface Mount Capacitor</td>
<td>GJM1555C1H1R7BB01</td>
<td>Murata</td>
</tr>
<tr>
<td>C3, C7, C10, C9</td>
<td>4</td>
<td>33pF ±5%, 25V, COG Surface Mount Capacitor</td>
<td>GRM1555C1H330J</td>
<td>Murata</td>
</tr>
<tr>
<td>C4</td>
<td>1</td>
<td>0.1uF ±10%, 16V, X7R Surface Mount Capacitor</td>
<td>GRM155R71C104KA88D</td>
<td>Murata</td>
</tr>
<tr>
<td>C8</td>
<td>1</td>
<td>0.1uF ±10%, 25V, X5R Surface Mount Capacitor</td>
<td>GCM188R71C104KA37D</td>
<td>Murata</td>
</tr>
<tr>
<td>C11</td>
<td>1</td>
<td>1uF ±10%, 25V, X5R Surface Mount Capacitor</td>
<td>GRM188R61E105KA12D</td>
<td>Murata</td>
</tr>
<tr>
<td>C5</td>
<td>1</td>
<td>100pF ±0.1pF, 50V, COG Surface Mount Capacitor</td>
<td>GRM1555C1H101J</td>
<td>Murata</td>
</tr>
<tr>
<td>C12</td>
<td>1</td>
<td>DNI</td>
<td></td>
<td></td>
</tr>
<tr>
<td>C13</td>
<td>1</td>
<td>1.8pF ±0.1dB, 50V, COG Surface Mount Capacitor</td>
<td>GJM1555C1H1R8BB01</td>
<td>Murata</td>
</tr>
<tr>
<td>R1</td>
<td>1</td>
<td>1.8kΩ ±5%, 1/10W</td>
<td>ERJ2GEJ182</td>
<td>Panasonic</td>
</tr>
<tr>
<td>R2</td>
<td>1</td>
<td>150Ω ±5%, 1/16W</td>
<td>ERJ2GEJ151</td>
<td>Panasonic</td>
</tr>
<tr>
<td>R8, R9, R10</td>
<td>3</td>
<td>0Ω, 1/10W</td>
<td>ERJ2GEOR00X</td>
<td>Panasonic</td>
</tr>
<tr>
<td>L1</td>
<td>1</td>
<td>10nH ±5%, 300mA, Surface Mount Inductor</td>
<td>LQG15HS10NJ02</td>
<td>Murata</td>
</tr>
<tr>
<td>L2</td>
<td>1</td>
<td>1.0nH ±0.3nH, 300mA, Surface Mount Inductor</td>
<td>LQG15HS10NS02</td>
<td>Murata</td>
</tr>
<tr>
<td>J1, J2, J3</td>
<td>3</td>
<td>Connector SMA Jack STR 50ohm Edge Mount</td>
<td>142-0701-851</td>
<td>Cinch Connectivity</td>
</tr>
<tr>
<td>J4, J5</td>
<td>2</td>
<td>DNI</td>
<td></td>
<td></td>
</tr>
<tr>
<td>J6</td>
<td>1</td>
<td>DNI Headerstrip 1x2</td>
<td></td>
<td></td>
</tr>
<tr>
<td>J7</td>
<td>1</td>
<td>Headerstrip 1x10</td>
<td>0022284103</td>
<td>Molex</td>
</tr>
<tr>
<td>TP1</td>
<td>1</td>
<td>Loop, Black, Phosphor Bronze Wire Loop</td>
<td>5001</td>
<td>Keystone electronics</td>
</tr>
<tr>
<td>U1</td>
<td>1</td>
<td>F1490, GaAs Pre-Driver Amplifier</td>
<td>F1490</td>
<td>Renesas</td>
</tr>
</tbody>
</table>

\(^{[a]}\) This BOM is optimized for low gain mode performance. Refer to application note for recommended high gain BOM.
Evaluation Board Schematic for 5.92GHz – 6.26GHz BOM

Figure 95. Electrical Schematic for 5.92GHz - 6.26GHz BOM

Note: Specifications shown for 5.92GHz to 6.26GHz require accommodating additional shunt component C14 that is not included in the F1490 Evaluation Kit.
### Evaluation Kit BOM – 5.92GHz to 6.26GHz

**Table 19. 5.92GHz to 6.26GHz Evaluation Kit Bill of Materials (BOM)**

<table>
<thead>
<tr>
<th></th>
<th></th>
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</tr>
</thead>
<tbody>
<tr>
<td>C1</td>
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<td>0.4pF ±0.1pF, 50V, COG Surface Mount Capacitor</td>
<td>GJM1555C1HR40BB01</td>
<td>Murata</td>
</tr>
<tr>
<td>C6</td>
<td>1</td>
<td>0.5pF ±0.1pF, 50V, COG Surface Mount Capacitor</td>
<td>GJM1555C1HR50BB01</td>
<td>Murata</td>
</tr>
<tr>
<td>C2</td>
<td>1</td>
<td>0.6pF ±0.1pF, 50V, COG Surface Mount Capacitor</td>
<td>GJM1555C1HR60BB01</td>
<td>Murata</td>
</tr>
<tr>
<td>C3, C7, C10, C9</td>
<td>4</td>
<td>33pF ±5%, 25V, COG Surface Mount Capacitor</td>
<td>GRM1555C1H330J</td>
<td>Murata</td>
</tr>
<tr>
<td>C4</td>
<td>1</td>
<td>0.1μF ±10%, 16V, X7R Surface Mount Capacitor</td>
<td>GRM155R71C104KA88D</td>
<td>Murata</td>
</tr>
<tr>
<td>C8</td>
<td>1</td>
<td>0.1μF ±10%, 25V, X5R Surface Mount Capacitor</td>
<td>GCM188R71C104KA37D</td>
<td>Murata</td>
</tr>
<tr>
<td>C11</td>
<td>1</td>
<td>1μF ±10%, 25V, X5R Surface Mount Capacitor</td>
<td>GRM188R61E105KA12D</td>
<td>Murata</td>
</tr>
<tr>
<td>C5</td>
<td>1</td>
<td>2.5pF ±0.1pF, 50V, COG Surface Mount Capacitor</td>
<td>GRM1555C1H2R5BB01</td>
<td>Murata</td>
</tr>
<tr>
<td>C12</td>
<td>1</td>
<td>0.3pF ±0.1pF, 50V, COG Surface Mount Capacitor</td>
<td>GJM1555C1HR30BB01</td>
<td>Murata</td>
</tr>
<tr>
<td>C13</td>
<td>1</td>
<td>DNI</td>
<td></td>
<td></td>
</tr>
<tr>
<td>C14</td>
<td>1</td>
<td>1.0kΩ ±5%, 1/10W</td>
<td>ERJ2GEJ102</td>
<td>Panasonic</td>
</tr>
<tr>
<td>R1</td>
<td>1</td>
<td>1.8kΩ ±5%, 1/10W</td>
<td>ERJ2GEJ182</td>
<td>Panasonic</td>
</tr>
<tr>
<td>R2</td>
<td>1</td>
<td>150Ω ±5%, 1/16W</td>
<td>ERJ2GEJ151</td>
<td>Panasonic</td>
</tr>
<tr>
<td>R8, R9, R10</td>
<td>3</td>
<td>0Ω, 1/10W</td>
<td>ERJ2GE0R00X</td>
<td>Panasonic</td>
</tr>
<tr>
<td>L1</td>
<td>1</td>
<td>68nH ±5%, 300mA, Surface Mount Inductor</td>
<td>L-07C68NJ6V6S</td>
<td>Johanson Technology</td>
</tr>
<tr>
<td>L2</td>
<td>1</td>
<td>1.0nH ±0.3nH, 300mA, Surface Mount Inductor</td>
<td>L-07C100NSV6S</td>
<td>Johanson Technology</td>
</tr>
<tr>
<td>J1, J2, J3</td>
<td>3</td>
<td>Connector SMA Jack STR 50ohm Edge Mount</td>
<td>142-0701-851</td>
<td>Cinch Connectivity</td>
</tr>
<tr>
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<tr>
<td>J6</td>
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<td>DNI Headerstrip 1x2</td>
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<td>1</td>
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<td>F1490</td>
<td>Renesas</td>
</tr>
</tbody>
</table>

[a] This BOM is optimized for High gain mode performance.
Power Supplies

A common VDD power supply should be used for all power supply pins. To minimize noise and fast transients, add de-coupling capacitors to all supply pins. Supply noise can degrade noise figure. In addition, all control pins should remain at 0V (±0.3V) while the supply voltage ramps or while it returns to zero.

If control signal integrity is a concern and clean signals cannot be guaranteed due to overshoot, undershoot, ringing, etc., the following circuit is recommended at the input of each control pin. This applies to the GAIN_SEL pin (15) and STBY pin (16) as shown below. Note the recommended resistor and capacitor values do not necessarily match the EV Kit BOM for the case of poor control signal integrity. For multiple devices driven by a single control line, the component values will need to be adjusted accordingly so as not to load down the control line.

Figure 96. Control Pin Interface for Signal Integrity
Package Outline Drawings

The package outline drawings are located at the end of this document and are accessible from the Renesas website. The package information is the most current data available and is subject to change without revision of this document.

Ordering Information

<table>
<thead>
<tr>
<th>Orderable Part Number</th>
<th>Package</th>
<th>MSL Rating</th>
<th>Shipping Packaging</th>
<th>Temperature</th>
</tr>
</thead>
<tbody>
<tr>
<td>F1490NLGA</td>
<td>3 × 3 × 0.9 mm 16-VFQFPN</td>
<td>MSL 1</td>
<td>Tray</td>
<td>-40° to +115°C</td>
</tr>
<tr>
<td>F1490NLGA8</td>
<td>3 × 3 × 0.9 mm 16-VFQFPN</td>
<td>MSL 1</td>
<td>Tape and Reel</td>
<td>-40° to +115°C</td>
</tr>
<tr>
<td>F1490EVB-2P0</td>
<td>Evaluation Board for 1.8GHz to 2.2GHz Band</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>F1490EVB-2P5</td>
<td>Evaluation Board for 2.3GHz to 2.7GHz Band</td>
<td></td>
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<tr>
<td>F1490EVB-3P6</td>
<td>Evaluation Board for 3.3GHz to 3.8GHz Band</td>
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<tr>
<td>F1490EVB-4P0</td>
<td>Evaluation Board for 3.8GHz to 4.2GHz Band</td>
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<tr>
<td>F1490EVB-4P7</td>
<td>Evaluation Board for 4.4GHz to 5GHz Band</td>
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</tr>
<tr>
<td>F1490EVB-6P0</td>
<td>Evaluation Board for 5.92GHz to 6.26GHz Band</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Marking Diagram

- Line 1: “XXX” represents the last three digits of the lot number.
- Line 2: “YWW” has one digit for the year and two digits for week that the part was assembled. “$$” denotes the assembly site.
- Line 3: “F1490” is the part number.

Revision History

<table>
<thead>
<tr>
<th>Revision Date</th>
<th>Description of Change</th>
</tr>
</thead>
<tbody>
<tr>
<td>November 15, 2021</td>
<td>▪ Added specifications for 2GHz, 4 GHz, 4.7GHz, and 6GHz bands.</td>
</tr>
<tr>
<td></td>
<td>▪ Operating frequency range extended to 1.8GHz – 6.4GHz.</td>
</tr>
<tr>
<td>August 17, 2020</td>
<td>Updated pins 1 and 3 descriptions in Table 1.</td>
</tr>
<tr>
<td>May 1, 2020</td>
<td>Added Application Information for Power Supplies.</td>
</tr>
<tr>
<td>April 9, 2020</td>
<td>Updated MSL rating.</td>
</tr>
<tr>
<td>February 18, 2020</td>
<td>Initial release.</td>
</tr>
</tbody>
</table>
Notes:

1. JEDEC compatible.
2. All dimensions are in mm. and angle are in degrees.
3. Use ±0.50 mm for the non-toleranced dimensions.
4. Numbers in ( ) are for references only.
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