Application note

RH850/E2UH
Example of capacitor placement BGA373

Abstract
This document describes the example of capacitor placement of RH850/E2UH FBGA-373 package.

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1. Decoupling capacitors

1.1 Capacitor placement and number of capacitors

➢ Please refer “2. Example of capacitor placement E2UH BGA373” and “3. PCB layout guidelines E2UH BGA373”.

➢ Capacitors has been kept as close as feasible to the related supply pin.

1.2 Types of capacitors

➢ 0.1μF, 0.22μF, 10μF or higher*1 ceramic capacitor (Low ESR/ESL is required)

➢ 10μF 3-terminal ceramic capacitor*2 (Very low ESR/ESL is required)

*1: This is expected value. Please follow the Power IC specification.

*2: 3-terminal capacitor is recommended for reduction of radiation noise.
2. Example of capacitor placement E2UH BGA373

Example capacitor connection for BGA373 package.

Legend
- Capacitor (The capacitance is 0.1μF)
- Capacitor (Expected value is 10μF or higher. Please follow the Power IC specification.)
- 3-terminal capacitor

E2UH

- ADSVCC (D24)
- ADSVREFH (D23)
- ADSVCL (C23)
- ADSVREFL (E23)
- ADSVSS (E24)
- A0VCC (D18)
- A0VREFH (C18)
- A0VSS (D19)
- A1VCC (D14)
- A1VREFH (C14)
- A1VSS (D13)
- A2VCC (J22)
- A2VREFH (J23)
- A2VSS (K22)
- A3VCC (N22)
- A3VREFH (N23)
- A3VSS (M22)

- E0VCC (B1, C2)
- VSS (A1, A2, B2, C3)
- LVDVCC (N1)
- VSS (L1, N2)
- E0VCC (AD23, AE24)
- E1VCC (AC22)
- VSS (AC23, AD24, AE25)
- RAMSVCL (W2)
- E2VCC (AB3)
- SYSVCC (Y4)
- VCC (AD1, AC2)
- VSS (AE1, AD2, AC3)

- VDD (Thermal ball)
- VSS (Thermal ball)

10μF feed-through capacitor as decoupling (Recommended)

10μF feed-through capacitor as filter (Recommended)

It is recommended that the capacitor for A^VREFH is closer to related pin than the capacitor for A^VCC.
3. PCB layout guidelines E2UH BGA373

Example capacitor placement for BGA373 package

Legend
- Capacitor (analog, Digital IO)
  (The capacitance is 0.1uF if not specified.)
- Capacitor (system)
  (Expected value is 10uF or higher.
  Please follow the Power IC specification.)
- Capacitor (Core voltage)
  (Expected value is 10uF or higher.
  Please follow the Power IC specification.)
- Capacitor (Core voltage)
  (The capacitance is 0.1uF if not specified.)
- 3-terminal capacitor (analog, Digital IO)
  (Expected value is 10uF or higher.
  Please follow the Power IC specification.)
- 3-terminal capacitor (Core voltage)

Digital IO
- Digital 5V
- VDD

Core voltage

Analog

Top Layer
### Bottom Layer

The diagram illustrates the bottom layer of the RH850/E2x- FCC2, E2UH, and E2H. The components and connections are highlighted in various colors to indicate different voltage levels and signal paths. The diagram includes
- **VDD** and **VSS** connections for power supply
- **SYSVCC** for system voltage
- **ADSVCC**, **ADSVCL**, **ADSVREFH**, and **ADSVRE** for ADC supply and references
- **A0VCC** and **A0VREFH** for general analog supply and reference
- **E0VCC** and **A2VCC** for external and analog power

The diagram is designed to help visualize the layout and connectivity of the analog components and their power supply requirements. The annotations and labels are critical for understanding the optimal placement and functionality for the SAR-ADC application note.
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General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Handling of Unused Pins
   — Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.

   The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal becomes possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on
   — The state of the product is undefined at the moment when power is supplied.

   The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.

   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.

   In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses
   — Access to reserved addresses is prohibited.

   The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals
   — After applying a reset, only release the reset line after the operating clock signal has become stable.

   When switching the clock signal during program execution, wait until the target clock signal has stabilized. When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products
   — Before changing from one product to another, i.e. to one with a different type number, confirm that the change will not lead to problems.

   The characteristics of MPU/MCU in the same group but having different type numbers may differ because of the differences in internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to products of different type numbers, implement a system-evaluation test for each of the products.
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