R-Car Series, 3rd Generation
DRAM Refresh Rate Setting

Introduction
This application note describes the DRAM refresh rate setting for third-generation R-Car series products.

Target Devices
- Versions 1.x, 2.0, 3.0 of the R-Car H3
- Version 1.0 of the R-Car H3-N
- Version 1.x, R-Car M3-W
- R-Car M3-W+
- Version 1.x of the R-Car M3-N
- R-Car V3H
- Version 1.x of the R-Car E3
- Version 1.x of the R-Car D3
- R-Car V3M
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1. **DRAM Refresh**

DRAM keeps information [0] and [1] by the presence or absence of charge in the internal capacitor. Because charge in the capacitor decreases by leakage current over time, it must be recharged at certain time intervals (refresh operation). Because leakage current increases exponentially with increasing temperature, recharging time interval (refresh interval) should be shorter in higher temperature environment.

Almost DDR3 / DDR3L and LPDDR4 SDRAM needs shorter refresh interval above 85 deg.C, the maximum operating temperature for standard DDR3/DDR3L and LPDDR4 is 85 deg.C. DDR3 / DDR3L and LPDDR4 SDRAM with maximum operating temperature over 85 deg.C is temperature expansion product, and almost such a DRAM needs less than half of standard interval refresh. And DDR3 / DDR3L and LPDDR4 SDRAM with maximum operating temperature over 95 deg.C needs further shorter, less than quarter of standard interval refresh. In addition, operation over 85 deg.C may affect signal access timing, AC timing derating in higher temperature environment is defined in LPDDR4 specification.

During the refresh operation, normal DRAM access is not possible, therefore, if the refresh interval becomes short, the bandwidth that can be used for normal access is reduced.

1.1 **The DBSC register for refresh interval setting**

There are two register for adjusting refresh interval in the DBSC of the third-generation R-Car series device, and a suitable refresh interval that DRAM needs is configured by these register setting.

<table>
<thead>
<tr>
<th>DBSC register</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>DBSC DBRFCNF1 register REFINT bit</td>
<td>It defines clock count for refresh interval (average)</td>
</tr>
<tr>
<td>DBSC DBRFCNF2 register REFINTS bit</td>
<td>It defines whether refresh interval (average) is be set 1/1 of REFINT or 1/2 of REFINT</td>
</tr>
</tbody>
</table>

Changing of REFINT setting needs stopping of the refresh operation, therefore, it is usually set during DRAM initialization. REFINTS setting can be changed during refresh operation.

1.2 **Adjustment of the refresh interval setting**

The refresh interval should be set so that there is no lack of refresh depending on the DRAM specification and its operating temperature. Renesas recommends the static refresh interval for the maximum operating temperature of DRAM assumed in the system. Dynamic changing of refresh interval depends on the DRAM temperature should be used after sufficient evaluation in your system.

1.2.1 **Setting value of the REFINT**

There are two value in the S/W development environment or sample DRAM initialization program. One is for standard refresh interval for under 85 deg.C operation, and the other is about half of standard refresh interval (*). For the REFINT setting value which is defined in the S/W development environment or sample DRAM initialization program Renesas provided should not be changed in principle. Because the QoS system works on the basis of the refresh interval, if REFINT is set to inappropriate value, the system may not work correctly.

If required refresh interval cannot be matched including changing of the REFINTS setting, contact to Renesas about changing REFINT setting.
Renesas sample code of R-Car V3H supports standard refresh interval x 1/2 only for REFINT configuration. Supported refresh interval setting by the R-Car V3H sample code by combination of REFINT and REFINTS Configuration is standard refresh interval x 1/2 or 1/4.

### 1.2.2 Setting value of the REFINTS
Set ‘1/1’ or ‘1/2’ rate according to the refresh interval the DRAM requires.

### 1.2.3 Setting of QoS
Renesas provides the QoS configuration set which are adjusted to match the refresh interval. The QoS configuration set has two patterns, one is for standard refresh interval for under 85 deg.C operation, and the other is for a half or quarter of standard refresh interval.

### 1.2.4 Combination of REFINT and REFINTS
The four combinations are possible by setting REFINT and REFINTS shown in following table, when a half of standard refresh interval is required, REFINT: Standard refresh interval x 1/2 and REFINTS: 1/1 rate should be selected.

<table>
<thead>
<tr>
<th>REFINT</th>
<th>REFINTS</th>
<th>Refresh interval</th>
<th>Setting</th>
</tr>
</thead>
<tbody>
<tr>
<td>Standard refresh interval (*)</td>
<td>1/1 rate</td>
<td>Standard refresh interval x 1/1</td>
<td>Available</td>
</tr>
<tr>
<td>Standard refresh interval (*) x 1/2</td>
<td>1/2 rate</td>
<td>Standard refresh interval x 1/2</td>
<td>Prohibit</td>
</tr>
<tr>
<td>Standard refresh interval (*)</td>
<td>1/1 rate</td>
<td>Standard refresh interval x 1/2</td>
<td>Available</td>
</tr>
<tr>
<td>Standard refresh interval (*)</td>
<td>1/2 rate</td>
<td>Standard refresh interval x 1/4</td>
<td>Available</td>
</tr>
</tbody>
</table>

**Note:** Standard refresh interval under 85 deg.C

The reason of prohibit setting is the QoS configuration set is switched by referring to REFINT setting in SW development environment which Renesas provides. When REFINT: Standard refresh interval and REFINTS: 1/2 rate is selected, QoS configuration set becomes for standard refresh interval instead of for half or quarter of standard refresh interval.

### 1.2.5 Confirmation of bus bandwidth
Conform whether bus bandwidth is insufficient according to selected refresh interval by the QoS tool. If bus bandwidth is insufficient due to selected short refresh interval, it is necessary to adjust the bus usage.

**Note:**
Suppressing heat generation by limitation of R-Car operation load and / or strong heat dissipation mechanism may be able to achieve the system which does not need shorter DRAM refresh interval.
1.3 Adjustment of the refresh interval setting for LPDDR4

In the LPDDR4 JEDEC standard, there are three types of definition for high-temperature expansion including AC timing derating. From the refresh interval point of view, half and quarter of standard refresh interval are for high-temperature expansion.

**Figure 1-3 Part of JEDEC Standard (JESD209-4B) MR4 register explanation**

<table>
<thead>
<tr>
<th>LPDDR4 JEDEC Specification</th>
<th>Data</th>
</tr>
</thead>
<tbody>
<tr>
<td>MR4 register OP [2:0]</td>
<td>000B: SDRAM Low temperature operating limit exceeded</td>
</tr>
<tr>
<td>Refresh rate</td>
<td>001B: 4x refresh</td>
</tr>
<tr>
<td></td>
<td>010B: 2x refresh</td>
</tr>
<tr>
<td></td>
<td>011B: 1x refresh (default)</td>
</tr>
<tr>
<td></td>
<td>100B: 0.5x refresh</td>
</tr>
<tr>
<td></td>
<td>101B: 0.25x refresh, no de-rating</td>
</tr>
<tr>
<td></td>
<td>110B: 0.25x refresh, with de-rating</td>
</tr>
<tr>
<td></td>
<td>111B: SDRAM High temperature operating limit exceeded</td>
</tr>
</tbody>
</table>

Hatching setting = For high-temperature expansion

LPDDR4 has a mechanism that allows the system can detect which refresh interval is required through the MR4 register read at over 85 deg.C. However, the threshold temperature for switching refresh interval is DRAM vendor depended, it may be different for the kind of DRAM of the same DRAM vendor. In order to know required refresh interval for high-temperature expansion, it is necessary to contact the DRAM vendor. And then, the shortest refresh interval that is assumed by the system should be set.

And also, according to used refresh interval, confirm shortage of the bandwidth and calculation of QoS settings by the QoS tool.

1.3.1 Dynamic refresh interval switching by the MR4 register reading

By polling the LPDDR4 MR4 OP [2:0] value at a certain interval, dynamic refresh interval switching which uses shorter refresh interval at high-temperature range only. By the changing REFINTS setting from 1/1 rate to 1/2 rate at high temperature. However, following issue will appear, and it should be used after sufficient evaluation in your system.

- When QoS setting applied to 1/1 rate refresh interval, switching 1/2 rate refresh interval by REFINTS may causes lack of bus bandwidth.
- The 1/2 rate refresh interval by REFINTS causes performance degradation of CPU, GPU and similar modules which uses bus bandwidth with best-effort, and then it causes inconvenience situation for use-case
- The interval time of polling MR4 register is defined by the trend of DRAM temperature changing after sufficient evaluation of actual use-case.
- There is MR4 register every LPDDR4 R–Car CH, every LPDDR4 rank ever LPDDR4 Ch (a / b). On the other hand, the REFINTS setting is one for R-Car device, therefore, if the system detects one MR4 reports requirement of shorter refresh interval, all refresh interval should be switched.
1.4 Adjustment of the refresh interval setting for DDR3 / DDR3L

According to the JEDEC standard ‘4.9 Extend Temperature Usage’, it defines from 85 deg.C to 95 deg.C as ‘Extend Temperature Range’. Its support and refresh operation (the word ‘Double Refresh’ is used) depends on DRAM vendor. As can be seen from the word ‘Double Refresh’, a half of refresh interval is assumed at the ‘Extend Temperature Range’, in fact, almost DRAM which supports 95 deg.C operation requires 1/2 refresh interval at from 85 deg.C to 95 deg.C operation. Some DRAM supports further high temperature environment (to 105 deg.C), it requires shorter refresh interval than 95deg.C supported product (for example, quarter of standard refresh interval).

DDR3 / DDR3L has no mechanism to report required refresh interval in DRAM side, therefore the refresh interval setting is depended on the system side. The shortest refresh interval that is assumed by the system should be set.
2. Appendix

In this chapter, modifying point of REFINT and REFINTS setting for each R-Car device are illustrated. The information may not be the latest. When the version of the document or the sample program is not same, refer to the similar point of the latest one.

2.1 Modifying point of REFINT setting

- R-Car H3 Ver.1.x, Ver.2.0, Ver.3.0, R-Car M3-W Ver.1.x, R-Car M3-W+, R-Car M3-N Ver.1.x, R-Car E3 Ver.1.x

How to modify REFINT setting for IPL (Initial Program Loader) is shown in following.

Initial Program Loader User’s Manual: Software (Rev.2.0.4, May 2019)
RENESAS_RCH3M3M3NE3_IPL_UME_v2.0.4.pdf

- **RCAR_REF_INT**

  Select DRAM refresh interval. If this option is not set, the value is set 0 internally.

<table>
<thead>
<tr>
<th>RCAR_REF_INT</th>
<th>DRAM refresh interval</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>Default setting (H3, M3, M3N 1.95us / E3 3.90us)</td>
</tr>
<tr>
<td>1</td>
<td>Optional setting (H3, M3, M3N 3.90us / E3 7.80us)</td>
</tr>
</tbody>
</table>

  **Note:** The option is available with R-Car H3 Ver 3.0/Ver 2.0, M3 Ver 3.0/Ver 1.3/Ver 1.2/Ver 1.1, M3N and E3. Note) Except for the above chips, the value must not be set 1. Note) If MD pin selection is other than MD7=0, MD6=0 or MD7=0, MD6=1, this option has been no effect.

- R-Car V3H

  Fixed setting is used in IPL (Initial Program Loader) source code which is provided from Renesas. It is only for standard refresh interval x 1/2. The REFINT value should not be changed.

- R-Car M3-N+ DDR3/DDR3L

  The setting exists in IPL (Initial Program Loader) source code which is provided from Renesas. Detail is not opened.
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DRAM Refresh Rate Setting

- **R-Car D3**

  The REFINT setting is defined in the sample DRAM initialization program. As the comment shown in source, the REFINT setting should be selected from 7800 (standard refresh interval) or 3900 (standard refresh interval x 1/2), and the other REFINT setting is prohibit. The QoS configuration set which is matched selected refresh interval should be used.

  Sample DRAM initialization program (ddr_init_d3.h)

  ```c
  #define RCAR_DDR_VERSION "rev.0.02"
  #define REFRESH_RATE 3900  // Average periodic refresh interval[ns]. Support 3900,7800
  ```

- **R-Car V3M**

  The REFINT is set in the sample DRAM initialization program. The REFINT should be selected from tREFI=7.8us (standard refresh interval) or tREFI=3.9us (standard refresh interval x 1/2). The immediate value set to DBRFCNF1 (0x00081860 and 0x00080C30) should not be changed. The QoS configuration set which is matched selected refresh interval should be used.

  Sample DRAM initialization program (ddr_init_v3m_20190619.c)

  ```c
  //WriteReg_32(DBSC_V3M_DBRFCNF1,0x00081860); //tREFI=7.8us
  WriteReg_32(DBSC_V3M_DBRFCNF1,0x00080C30); //tREFI=3.9us
  ```
2.2 Modifying point of REFINTS setting

- R-Car H3 Ver.1.x, Ver.2.0, Ver.3.0, R-Car M3-W Ver.1.x, R-Car M3-W+, R-Car M3-N Ver.1.x, R-Car V3H

The REFINTS setting is defined in the DRAM initialization program. Select suitable one for your system. When the REFINT is set for standard refresh interval, the REFINT setting should be set to standard refresh interval x1/2 instead of REFINTS is set to 1/2 rate.

DRAM initialization program (boot_init_dram_regdef.h)

```c
/* refresh mode */
/* 0: Average interval is REFINT. / 1: Average interval is 1/2 REFINT. */
#define DBSC_REFINTS 0x0
```

- R-Car E3

The REFINTS is set as immediate value in the sample DRAM initialization program, it is necessary for modification to edit source code. When the REFINT is set for standard refresh interval, the REFINT setting should be set to standard refresh interval x1/2 instead of REFINTS is set to 1/2 rate.

Sample DRAM initialization program (ddr_init_e3.c)

```c
WriteReg_32(DBSC_E3_DBRFCNF2, 0x00010000);
WriteReg_32(DBSC_E3_DBDFICUPDCNF, 0x40100001);
WriteReg_32(DBSC_E3_DBRFEN, 0x00000001);
WriteReg_32(DBSC_E3_DBACEN, 0x00000001);
```

When the REFINTS setting to 1/2 rate, modify source code which has yellow hating in above to following.

- WriteReg_32(DBSC_E3_DBRFCNF2, 0x00010001);
- **R-Car D3**
  The REFINTS is set as immediate value in the sample DRAM initialization program, it is necessary for modification to edit source code. When the REFINT is set for standard refresh interval, the REFINT setting should be set to standard refresh interval x1/2 instead of REFINTS is set to 1/2 rate.

Sample DRAM initialization program (ddr_init_d3_rev0.02.c)

```c
WriteReg_32(DBSC_D3_DBRFCNF2,0x00010000);
WriteReg_32(DBSC_D3_DBDFICUPDCNF,0x40100001);
WriteReg_32(DBSC_D3_DBRFEN,0x00000001);
WriteReg_32(DBSC_D3_DBACEN,0x00000001);
```

When the REFINTS setting to 1/2 rate, modify source code which has yellow hating in above to following.

- ➢ WriteReg_32(DBSC_D3_DBRFCNF2,0x00010001);

- **R-Car V3M**
  The REFINTS is set as immediate value in the sample DRAM initialization program, it is necessary for modification to edit source code. When the REFINT is set for standard refresh interval, the REFINT setting should be set to standard refresh interval x1/2 instead of REFINTS is set to 1/2 rate.

Sample DRAM initialization program (ddr_init_v3m_20190619.c)

```c
WriteReg_32(DBSC_V3M_DBRFCNF2,0x00010000);
WriteReg_32(DBSC_V3M_DBDFICUPDCNF,0x40100001);
WriteReg_32(DBSC_V3M_DBRFEN,0x00000001);
WriteReg_32(DBSC_V3M_DBACEN,0x00000001);
```

When the REFINTS setting to 1/2 rate, modify source code which has yellow hating in above to following.

- ➢ WriteReg_32(DBSC_V3M_DBRFCNF2,0x00010001);
## Revision History

<table>
<thead>
<tr>
<th>Rev.</th>
<th>Date</th>
<th>Page</th>
<th>Description</th>
<th>Summary</th>
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<tr>
<td>1.00</td>
<td>October, 2019</td>
<td>—</td>
<td>First edition issued</td>
<td></td>
</tr>
<tr>
<td>1.01</td>
<td>November, 2019</td>
<td>10</td>
<td>Modified Sample DRAM initialization program name of R-Car V3M</td>
<td></td>
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<tr>
<td>1.02</td>
<td>February, 2020</td>
<td>4</td>
<td>Updated the description of “Note” in Section 1.2.1.</td>
<td></td>
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</table>
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2. Processing at power-on
   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.

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   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.

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   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extraneous electromagnetic noise is induced in the vicinity of the LSI, and associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.

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