R-Car S4 Series
DRAM Backup Function

Introduction
This application note explains how to use the function of R-Car S4 series products for backing up the contents of connected DRAM (mainly intended for use with LPDDR4X SDRAM).

This document describes a circuit configuration and processing sequences required to back up DRAM in terms of the hardware. Refer to the separate specifications and application notes regarding the use of software to implement the "suspend to RAM" function in Linux.

Backing up DRAM requires coordination of control between an R-Car S4 series device and external system controllers (such as a microcontroller and power management IC). This document gives an example of a general backup sequence. This is followed by an example of the implementation (hardware and software) of DRAM backup on a Renesas evaluation board for reference.

Target Devices
- R-Car S4-8
- R-Car S4-4
- R-Car S4N-8
- R-Car S4N-4
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1. DRAM Backup Function

DRAM devices have a function called self-refresh, which automatically refreshes the memory contents without being controlled by other devices while there is no need to access DRAM. In this document, making DRAM enter the self-refresh mode is called the DRAM backup function.

While DRAM is being backed up, DRAM cannot be accessed but the DRAM controller does not need to control DRAM refresh operations; the power supply to the controller can be turned off and the entire system can enter a low-power state.

To shift DRAM to the self-refresh mode, the DRAM controller should issue a self-refresh command to the target DRAM. Driving the CKE signal high or driving the RESET# signal low makes DRAM exit the self-refresh mode and cancels the DRAM backup mode.

1.1 DRAM backup in R-Car S4 Series Products

While DRAM is being backed up for an R-Car S4 series product, the IO power supplies and the logic power supplies to application domains other than those to the DDR IO interface and control domains can be turned off.

The CKE signal should be held low and the RESET# signal should be held high while DRAM is being backed up.

The R-Car S4 series product is retained in the backup state by externally controlling the MxBKUP signal while the power supply to the logic circuits is off.

Table 1-1  Operation of the M0BKUP Signal

<table>
<thead>
<tr>
<th>M0BKUP Signal</th>
<th>Operation</th>
</tr>
</thead>
<tbody>
<tr>
<td>Low</td>
<td>The M0CKE and M0RESET# signals are controlled by the DRAM controller in the SoC.</td>
</tr>
<tr>
<td>High</td>
<td>The M0CKE and M0RESET# signals retain their state when the M0BKUP signal has been driven high. After issuing a self-refresh command to DRAM, the DRAM controller drives the M0CKE signal low and the M0RESET# signal high.</td>
</tr>
</tbody>
</table>

An example of a circuit configuration for backing up LPDDR4X SDRAM with the R-Car S4 is shown in Figure 1-1.
1.2 Example of a Circuit Configuration for Backing up LPDDR4X SDRAM with the R-Car S4

![Diagram of circuit configuration]

**Normal Operation**

**Backing up DRAM**

Note: * These signals are used for handshaking to manipulate the MxBKUP signal with the appropriate timing. Instead of GPIO pins, a communications interface such as I2C can be used to implement similar control. For details, refer to section 1.3.

*Figure 1-1 Example of a Circuit Configuration for Backing up LPDDR4X SDRAM with the R-Car S4*
1.3 Example of Backing up DRAM with the R-Car S4: Handshake Signals

To control the M0BKUP signal with the appropriate timing, the handshake signals shown in Figure 1-1 (an example of a circuit configuration for backing up LPDDR4X SDRAM with the R-Car S4) are assumed to work as shown in Table 1-2 and Figure 1-2 to Figure 1-4.

In the figure of an example circuit configuration, GPIO pins are used for the handshake signals, but implementation is not limited to this approach. Handshaking with the use of a communications interface such as I2C can implement similar control.

Table 1-2 Example of Handshake Signals for Backing up DRAM

<table>
<thead>
<tr>
<th>Signal</th>
<th>Input/Output Setting in R-Car S4 Series Products</th>
<th>Operation</th>
</tr>
</thead>
<tbody>
<tr>
<td>I2C</td>
<td>Input/output</td>
<td>Requests the external system controller (PMIC) to execute the processing for backing up DRAM. Control of the BKUP_Reg signal from the R-Car S4 to the PMIC is through an I2C interface. Requests to drive the BKUP signal high.</td>
</tr>
<tr>
<td>BKUP</td>
<td>Input</td>
<td>When the R-Car S4 is placed in the deep stop mode. The signal notifies the R-Car S4 of the backup state of the DDR4X SDRAM. High level: The DDR4X SDRAM is backed up. Low level: The DDR4X SDRAM is not backed up.</td>
</tr>
</tbody>
</table>

When GPIO pins are used to implement these signals, note that the input and output should be at the same voltage levels as those of the IO power supply for the GPIO pins and a high level must not be applied to the GPIO pins while the power supplies to the R-Car S4 are off (using GPIO pins which belong to the control domains is recommended).
1.4 Example of Backing up DRAM with the R-Car S4: Sequence Example (Full RUN -> RT (DDR Backup Mode) -> Full RUN)

Notes:
1. The DDR backup return sequence is complete; write 0 to reg_DDR_BKUP.
2. This timing includes the timing for the following power supplies, see the relevant descriptions for details.
   - (8) Period for Power Fall 2, (6) Period for Power Rise 2
   - VDDQ18, VDD18_CPGPLLx (x = 1, 2, 3, 5, 6), VDD18_OCO, VDD18_TRNG, VDD, VDD_DDRPLL
   - VDDQ33, VDDQ18_33TSN, VDDQ18_33_SDHI, VDDQ18_33_SPI, VDDQ18_33_I2C as all IO power supplies

Figure 1-2  Example of Backing up DRAM with the R-Car S4: Sequence Example (Full RUN -> RT (DDR Backup Mode) -> Full RUN)
1.5 Processing for Entering DRAM Self-Refresh (Backup) Mode for an R-Car S4 Series Device

<table>
<thead>
<tr>
<th>Step</th>
<th>Action</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.</td>
<td>Stop DRAM access.</td>
<td>Stop execution of all programs that access the target DRAM to be shifted to the self-refresh mode because the system may hang if an attempt is made to access the DRAM area after access to it is disabled. In order to write to registers of the DBSC, write the key value to DBSC system register 0 (DBSYSCNT0).</td>
</tr>
<tr>
<td>2.</td>
<td>Enable DRAM register writing.</td>
<td></td>
</tr>
<tr>
<td>3.</td>
<td>DBDFIPMSTRCNF register setting</td>
<td>Clear the PMSTREN bit to 0 in the DFI PHY master control register (DBDFIPMSTRCNF).</td>
</tr>
<tr>
<td>4.</td>
<td>Disable DRAM access.</td>
<td>Clear the ACCEN bit to 0 (disabling access to the SDRAM) in the SDRAM access enable register (DBACEN).</td>
</tr>
<tr>
<td>5.</td>
<td>Flush the DBSC buffer.</td>
<td>Flush the DBSC’s internal buffer by writing 1 to the CAM control register 0 (DBCAM0CTRL0).</td>
</tr>
<tr>
<td>6.</td>
<td>Disable SDRAM calibration.</td>
<td>Wait until the DBSC’s internal buffer has been flushed. Do so by polling the CAMn unit status register 0 (DBCAMnSTAT0) until its value becomes 1. The register to use in confirming this depends on the number of the DRAM channel in use (n = 0 or 1).</td>
</tr>
<tr>
<td>7.</td>
<td>Precharge all DRAM banks (PREA).</td>
<td>Write 0 to the CAM control register 0 (DBCAM0CTRL0) then clear the CALEN bit in the SDRAM calibration configuration register (DBCALCNF) to disable SDRAM calibration.</td>
</tr>
<tr>
<td>8.</td>
<td>Set up DRAM mode registers.</td>
<td>Use the manual command-issuing register (DBCMD) to issue the self-refresh entry (SRE) command.</td>
</tr>
<tr>
<td>9.</td>
<td>Issue the self-refresh entry (SRE) command to DRAM.</td>
<td>Poll the operation completion waiting register (DBWAIT) to wait until the WAIT bit becomes 0.</td>
</tr>
<tr>
<td>10.</td>
<td>Disable ODT for the DRAM via mode register 11 (MR11).</td>
<td>Use the manual command-issuing register (DBCMD) to set mode register 11 (MR11) to 0 in order to disable the DRAM’s internal ODT.</td>
</tr>
<tr>
<td>11.</td>
<td>Issue the power-down (PD) command to DRAM.</td>
<td>Poll the operation completion waiting register (DBWAIT) to wait until the WAIT bit becomes 0.</td>
</tr>
<tr>
<td>12.</td>
<td>Stop or modify the clock supply to DBSC and turn off the power.</td>
<td>Clear ARFEN bit in the auto-refresh enable register (DBRFEN) to stop the auto-refresh function. Perform a dummy read to the operation completion waiting register (DBWAIT), for example, and the tCKELPD period will elapse.</td>
</tr>
</tbody>
</table>

Figure 1-3 Procedure for Entering Self-Refresh Mode for an R-Car S4 Series Device
Notes:
1. When the DRAM contains an exception vector table which includes the reset exception vector for the CPU, an exception occurring during the backup sequence after DRAM access has been disabled may lead to unexpected DRAM read access due to exception vector access by the CPU. Ensure that this does not occur. Also ensure that DRAM access by MMU page table walk does not occur after DRAM access has been disabled.
2. To only issue a command to the target channel of DRAM for self-refresh (backup), the CH bits in the manual command-issuing register (DBCMD) can be used to select the channel to which the command is to be issued. Note that issuing the command for channels other than the target channel does not create a problem because the supplies of power to the channels other than the target channel will finally be turned off during the process of backup.

1.6 Processing for Release from DRAM Self-Refresh (Backup) Mode for an R-Car S4 Series Device

1.6.1 Processing for Release from Backup Mode for an R-Car S4 Series Device: In Transitions from RT (DDR Backup Mode) to Full RUN

When the PMIC enters the RT state (DDR backup mode) and then returns to the Full RUN state while the DRAM is backed up, the DRAM controller and PHY units should be initialized and the MxBKUP signal level should be controlled with the correct timing. Renesas plans to provide firmware for this initialization and control processing; refer to the implementation guide and application note for the firmware and execute the processing correctly.
1.6.2 Processing for Release from Backup Mode: Not Involving Turning off the Power Supplies or Applying a Reset to an R-Car S4 Series Device

Figure 1-4 shows the procedure for release from the backup mode when the clock for the DRAM is stopped to reduce power consumption and DRAM is placed in the self-refresh mode during operation of an R-Car S4 series device.

The use of this procedure is limited to cases where initialization of the DRAM controller or PHY units is not necessary, such as for repeated training. To determine whether initialization is necessary, consult Renesas and provide specific information regarding the usage or situation of the user system, and we will examine the information and respond.

![Procedure for Release from Self-Refresh Mode for an R-Car S4 Series Device](image)

**Figure 1-4 Procedure for Release from Self-Refresh Mode for an R-Car S4 Series Device**

Note: * If ODT was disabled during self-refresh, enable ODT again after issuing the power-down exit (PDX) command.
2. Estimating Power Consumption in DRAM Backup Mode

The power consumed while DRAM is backed up is the sum of the self-refresh current in the DRAM, the dark current from the power supply for the DDR IO interface in the R-Car S4 series device, and the operation standby current for the control domains. The self-refresh current in the DRAM depends on the capacity and temperature of the DRAM; a larger current flows as the capacity increases or the temperature rises. For the self-refresh current in the DRAM, contact the manufacturer of the DRAM.

Table 2-1 shows the reference values of power consumption in R-Car S4 series products while DRAM is backed up.

Table 2-1  Power Consumption in R-Car S4 Series Products While DRAM is Backed up (Typ.)

(VDDQVA_DDRx = 1.1 V, VDDQ18_DDRx = 1.8 V, Ta = Tc = Tj = 25°C)

<table>
<thead>
<tr>
<th></th>
<th>4-Gbyte DRAM</th>
</tr>
</thead>
<tbody>
<tr>
<td>VDDQX_DDR</td>
<td>T.B.D. mW</td>
</tr>
<tr>
<td>VDDQVA_DDR</td>
<td>T.B.D. mW</td>
</tr>
<tr>
<td>Other power supplies for the control domains</td>
<td>T.B.D. mW</td>
</tr>
</tbody>
</table>

Note: The current flowing while DRAM is backed up strongly depends on the DRAM device used. Table 2-1 shows the values calculated according to the specifications of the DRAM used with the R-Car S4.
Appendix

A1 Example of Backing up DRAM on the R-Car S4 Evaluation Board (Reference Information)

On the R-Car S4 evaluation board from Renesas, the DRAM backup function is implemented through cooperation with the on-board power management IC (PMIC). This section shows implementation of the DRAM backup function on the Spider evaluation board from Renesas as an example of the necessary circuits and sequences for the DRAM backup function.
Figure A1-1  Block Diagram of Circuits for Backing up DRAM on the R-Car S4 Evaluation Board

- **Power switch on the board**: Turn off: RSTB = Low
- **Region where power supplies are turned off while DRAM is backed up**
- **Power supply while DRAM is backed up**: Low or High: Signal level while DRAM is backed up

**Components**:
- **VDDQVA_DDR**
- **VDD_DDRPLL**
- **I2C**
- **LPDDR4X SDRAM**
- **PMIC**
- **R-Car S4**

**Signals**:
- **M0: CLK, ADDR, CMD**
- **M0: DOS, DQ, DM**
- **M0RESET#**
- **M0CKE**
- **VDDQ**
- **VDD2**
- **VDD1**
- **ZQ**
- **CLK, ADDR, CMD**
- **DOS, DQ, DM**
- **RESET**
- **CKE**
- **VDDQVA_DDR**
- **VDD_DDRPLL**
- **GPIO (3.3 V)**
- **I2C**
- **LPDDR4X_SDRAM**
- **VDDQVA_DDR**
- **VDD_DDRPLL**
- **GPIO (3.3 V)**
- **I2C**

**Power Supplies**:
- **1.1 V**
- **1.8 V**
- **3.3 V**
- **0.6 V**
- **1.8 V**

**Other power supplies** for the control domains and other power supplies.
## A1.2 Signals and Power Supplies in the Block Diagram of Circuits for Backing up DRAM on the R-Car S4 Evaluation Board

### Table A1-1 Signals and Power Supplies in the Block Diagram of Circuits for Backing up DRAM on the R-Car S4 Evaluation Board

<table>
<thead>
<tr>
<th>Signal</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>BKUP</td>
<td>Connected to the M0BKUP pin of the R-Car S4</td>
</tr>
<tr>
<td>PRESET#</td>
<td>Cold reset input to the R-Car S4 (1.8 V)</td>
</tr>
<tr>
<td>RSTB</td>
<td>Power switch input to the PMIC</td>
</tr>
<tr>
<td>I2C</td>
<td>I2C is used (1.8 V).</td>
</tr>
<tr>
<td>0.6 V</td>
<td>Power supply for LPDDR4X SDRAM and DDR IO interface in the R-Car S4</td>
</tr>
<tr>
<td>1.1 V</td>
<td>Power supply for LPDDR4X SDRAM and DDR IO interface in the R-Car S4</td>
</tr>
<tr>
<td>1.8 V</td>
<td>Power supply for LPDDR4X SDRAM</td>
</tr>
<tr>
<td>VDD_DDRPLL</td>
<td>Power supply for the PLL in the DDR IO interface in the R-Car S4</td>
</tr>
<tr>
<td>Other power supplies for the application domains</td>
<td>0.8-V logic, 2.5-V IO, and 3.3-V IO power supplies for the application domains in the R-Car S4</td>
</tr>
<tr>
<td>Other power supplies for the control domains</td>
<td>0.8-V logic, 2.5-V IO, and 3.3-V IO power supplies for the control domains in the R-Car S4</td>
</tr>
<tr>
<td>VSYS, 3.3 V (IN)</td>
<td>Power supplies for the PMIC (always supplied while DRAM is backed up)</td>
</tr>
</tbody>
</table>
A1.3 Operation Control Register in the PMIC

The power management IC (PMIC: RAA271005) mounted on the Spider board from Renesas has a register for controlling the DRAM backup function, and this can be read from and written to through the I2C interface. Table A1-2 shows the functions of the main control register in the PMIC. For detailed specifications, refer to the manual or datasheet for the PMIC.

Table A1-2 Operation Control Register in the PMIC

<table>
<thead>
<tr>
<th>Register Name</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>reg_DDR_BKUP</td>
<td>Monitors and controls the output from the BKUP pin.</td>
</tr>
</tbody>
</table>

Note: In this table, for conciseness, the name has been adjusted and only the most important functions are stated. For detailed specifications, refer to the manual or datasheet for the PMIC.
A1.4  State Transitions of PMIC on the R-Car S4 Evaluation Board

Figure A1-2 shows state transitions related to control of the DRAM backup function in the power management IC (PMIC: RAA271005) mounted on the Spider board from Renesas. For detailed specifications, refer to the manual or datasheet for the PMIC.

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**Note:** This state transition diagram is simplified for concise description. For detailed specifications, refer to the manual or datasheet for the PMIC.

---

**Figure A1-2  State Transitions of PMIC on the R-Car S4 Evaluation Board**
A1.5 Sequence of Entering DRAM Backup Mode on the R-Car S4 Evaluation Board

Figure A1-3 shows the sequence of entering DRAM backup mode.

---

**Figure A1-3** State Transitions of PMIC on the R-Car S4 Evaluation Board
1. Writing to the PMIC register by the R-Car S4 in <1> drives the BKUP signal from the PMIC high as shown in <3>, which drives the M0BKUP and GPIO signals of the R-Car S4 high.

2. The R-Car S4 drives its PWRCTL_SOCISO signal low in <2> to instruct the PMIC to turn off the power supplies to the application domains.

3. The PMIC then turns off the power supplies to the application domains in <4>.

4. The PMIC drives the PWRGD signal low in <5>.

5. The R-Car S4 drives the PWECTL_MCUPLL signal low in <6> to instruct the PMIC to turn off the power supply to the PLL.

6. The PMIC turns off VDD18_MUCPLL in <7>.

7. Power supplies to the control domains in <8> and the signals in the reset system in <9> are kept in the current states.
A1.6 Sequence of Release from the DRAM Backup Mode on the R-Car S4 Evaluation Board

Figure A1-4 shows the sequence of release from the DRAM backup mode.

---

**Figure A1-4 State Transitions of PMIC on the R-Car S4 Evaluation Board**

---
1. The R-Car S4 detects a wake-up trigger in <1>.
2. The R-Car S4 drives the PWECTL_MCUPLL signal high in <2> to instruct the PMIC to turn on the power supply to the PLL.
3. The PMIC turns on VDD18_MUCPLL in <3>.
4. The R-Car S4 drives its PWRCTL_SOCIS0 signal high in <4> to instruct the PMIC to turn on the power supplies to the application domains.
5. The PMIC turns on the power supplies to the application domains in <5>.
6. The PMIC drives the PWRGD signal high in <6>.
7. The R-Car S4 uses a GPIO signal to confirm that the DRAM is being backed up in <7> and executes the processing for release from the DRAM backup mode.
8. Writing to the PMIC register by the R-Car S4 in <8> drives the BKUP signal from the PMIC low as shown in <7>. The necessary processing for release from the DRAM backup mode is complete at this point.
A1.7 Supplementary Information: Failure to Retain Data While DRAM is Backed up

Although the DRAM device is responsible for preserving correct data in the self-refresh mode, the user should also take care about the correctness of data because a serious problem may arise in the system if DRAM fails to retain some data. Even when a correct sequence is executed to enter the backup mode, some data may be lost or corrupted due to unexpected fluctuations in power supplies, signals, or temperature.

As a way of detecting a failure to retain data, the user can write dummy data to an empty memory area that can be used without causing any problem in the system before entering the backup mode, check whether the data is correct after release from the backup mode, and if the data is not correct, discard the retained data and restart execution with a cold boot.

As the DRAM device stores electronic charges in capacitors, a failure to retain data is usually found as a value of "0" being read instead of the correct value of "1".
## Revision History

<table>
<thead>
<tr>
<th>Rev.</th>
<th>Date</th>
<th>Description</th>
<th>Page</th>
<th>Summary</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.00</td>
<td>January, 2022</td>
<td>—</td>
<td></td>
<td>Newly created.</td>
</tr>
</tbody>
</table>
General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)
   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.

2. Processing at power-on
   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.

3. Input of signal during power-off state
   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.

4. Handling of unused pins
   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.

5. Clock signals
   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.

6. Voltage application waveform at input pin
   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between $V_{IL}$ (Max.) and $V_{IH}$ (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between $V_{IL}$ (Max.) and $V_{IH}$ (Min.).

7. Prohibition of access to reserved addresses
   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.

8. Differences between products
   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.
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