RX62N, H8SX1668

ADC Migration Guide: H8SX/1668 to RX62N

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Introduction

The following document describes the differences between the A/D converter modules found on the RX62N and H8SX/1668 devices.

Target Device

RX62N

H8SX/1668

Contents

1. Features 2
2. General Notes 3
3. References 3
4. Hardware Details 4
5. Register Details 5
6. Usage Notes 13

1. Features

Table 1.1 lists the features of the A/D Converters found on the RX62N and H8SX/1668 devices. Differences are highlighted.

Table 1.1 - 10-Bit A/D Converter Features

	Specification	
Item	**RX62N**	**H8SX/1668**
Resolution	10-bit *1	10-bit
Number of units	2 Units – Unit 0 & Unit 1	2 Units – Unit 0 & Unit 1
Input Channels	8 in total 4 – Unit 0 4 – Unit 1	8 in total 4 – Unit 0 4 – Unit 1 OR 8 – Unit 0 0 – Unit 1
Conversion Time/channel	1.0us (at 50MHz Peripheral Clock, PCLK)	2.7us (at 35MHz Peripheral Clock, PLCK)
Maximum signal source impedance for full-speed conversion	1.0k ohm	5.0k ohm
A/D Conversion Clock	4 types: PCLK PCLK / 2 PCLK / 4 PCLK / 8	
Operating Modes	Single Mode Scan Mode – Continuous (1 to 4 channels) Scan Mode – One-Cycle then Stop (1 to 4 channels)	Single Mode Scan Mode – Continuous (1 to 4 channels) OR (1 to 8 channels) Scan Mode – One-Cycle then Stop (1 to 4 channels) – Unit 1 only
Conversion Start	Software Start Trigger by MTU or 8-bit TMR External Trigger - #ADTRG pin	Software Start Trigger by TPU or 8-bit TMR External Trigger - #ADTRG pin
Function	Sample & Hold	Sample & Hold
Interrupt Source	A/D Conversion End Interrupt (ADI) Can trigger DMAC Can trigger DTC	A/D Conversion End Interrupt (ADI) Can trigger DMAC Can trigger DTC (Unit 0 only)
Power-down function	Module Stop Mode can be set	Module Stop Mode can be set

Notes:
1. The RX62N also has a 12-bit ADC that can be used in place of the 10-bit ADC.

2. General Notes

- Increased conversion speed means that changes to external signal conditioning circuitry may be required; new clocking and conversion options may minimize or eliminate the necessity of such changes in some cases.
- Result registers can be left or right justified for compatibility with existing software. On the RX62N, results are right justified by default placing the reading in the least significant 10 bits of the 16-bit register. Application code ported from the H8SX expects A/D results to be left justified. Use the A/D Data Placement Register (ADDRPR) to force the data to be left justified: set the Data Placement Select (DPSEL) bit high to make the A/D results left justified so that they match the H8SX/1668.
- A new diagnostics register allows reading of internal reference voltages to verify proper function of the ADC.
- One-cycle scan mode is available on both Unit 0 and Unit 1 on the RX62N; it is available only on Unit 1 of the H8SX/1668.

3. References

The hardware manual for the RX62N is:

REJ09B0552: RX62N Group, RX621 Group Hardware Manual

The software manual for the RX62N is:

REJ09B0435: RX Family Software Manual

3.1 Hardware Manual Relevant Chapters

Clock Generation Circuit – for details on how to setup the peripheral clock used by the ADC

I/O Registers – provides a complete listing of all registers

Low Power Consumption – for details on the Module Stop Control registers

Interrupt Control Unit - for details on the enabling interrupts from the ADC to the interrupt controller

I/O Ports – for details on ICR and Port Function Control registers relevant to pins associated with the ADC

10-Bit A/D Converter – for details on ADC-specific registers and operating modes

3.2 Associated Registers

Table 3.1 - Registers Associated with ABR Operation

Name	Description	H/W Manual Chapter(s)
SYSTEM.SCKR	System Clock Control Register	Clock Generation Circuit
SYSTEM.MSTPCRA	Module Stop Control Register A	Low Power Consumption
ICU.IRx	Interrupt Request Register	Interrupt Control Unit
ICU.IERx	Interrupt Request Enable Register	Interrupt Control Unit
ICU.IPRx	Interrupt Priority Register	Interrupt Control Unit
PORTx.DDR	Port Data Direction Registers	I/O Ports
PORTx.ICR	Input Buffer Control Registers	I/O Ports
IOPORT.PFAADC	Port Function Control Register A	I/O Ports
ADx.ADDRA	A/D data register A	10-bit AD Converter
ADx.ADDRB	A/D data register B	10-bit AD Converter
ADx.ADDRC	A/D data register C	10-bit AD Converter
ADx.ADDRD	A/D data register D	10-bit AD Converter
ADx.ADCSR	A/D Control/Status Register	10-bit AD Converter
ADx.ADCR	A/D Control Register	10-bit AD Converter
ADx.ADPR	A/D Data Placement Register	10-bit AD Converter
ADx.ADSSTR	A/D Sampling State Register	10-bit AD Converter
ADx.ADDIAGR	A/D Diagnostic Register	10-bit AD Converter

4. Hardware Details

The RX62N has an additional pin associated with the A/D converter relative to the H8SX/1668: VREFL. This pin should be tied to analog ground pin AVSS. Refer to the data sheet for the RX62N for complete details on connection of grounds, supplies, and bypassing. Valid voltages for VREFH are from 2.7 V to AVCC on parts with low voltage spec, and 3.0 V to AVCC on parts with standard voltage spec.

To take advantage of the increased speed of the RX62N's ADC, signal-conditioning circuitry connected to the analog inputs must meet a lower impedance requirement:

	RX62N	H8SX/1668
Maximum peripheral clock (PCLK)	50 MHz	35 MHz
Maximum conversion speed	1.0 uS/channel	2.7 uS/channel
Maximum source impedance	1.0k Ohm	5.0k Ohm

New clocking and conversion options may minimize or eliminate the necessity of hardware changes to external circuitry. See Section 6.3 - A/D timing differences between RX8S/1668 and RX62N.

5. Register Details

Table 5.1 - A/D Registers lists the registers of the A/D Converters found on the RX62N and H8SX/1668 devices.

Table 5.1 - A/D Registers

RX62N	H8SX/1668
Unit 0	**Unit 0**
A/D Data Register A – ADDRA	A/D Data Register A – ADDRA
A/D Data Register B – ADDRB	A/D Data Register B – ADDRB
A/D Data Register C – ADDRC	A/D Data Register C – ADDRC
A/D Data Register D – ADDRD	A/D Data Register D – ADDRD
	A/D Data Register E – ADDRE
	A/D Data Register F – ADDRF
	A/D Data Register G – ADDRG
	A/D Data Register H – ADDRH
A/D Control/ Status Register – ADCSR	A/D Control/ Status Register – ADCSR
A/D Control Register – ADCR	A/D Control Register – ADCR
A/D Data Placement Register – ADDPR	
A/D Sampling State Register – ADSSTR	
A/D Self-Diagnostic Register – ADDIAGR	
Unit 1	**Unit 1**
A/D Data Register A – ADDRA	
A/D Data Register B – ADDRB	
A/D Data Register C – ADDRC	
A/D Data Register D – ADDRD	
	A/D Data Register E – ADDRE
	A/D Data Register F – ADDRF
	A/D Data Register G – ADDRG
	A/D Data Register H – ADDRH
A/D Control/ Status Register – ADCSR	A/D Control/ Status Register – ADCSR
A/D Control Register – ADCR	A/D Control Register – ADCR
A/D Data Placement Register – ADDPR	
A/D Sampling State Register – ADSSTR	
A/D Self-Diagnostic Register – ADDIAGR	

5.1 A/D Data Register: ADDRn

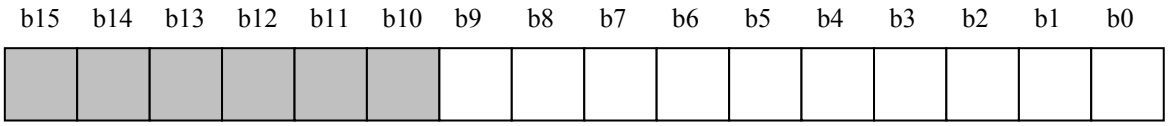
The ADDRn registers are 16 bit Read Only Registers that store the result of the A/D Conversion.

On the RX62N it can be specified where the 10-bit data is stored: ADDRn[15:6] or ADDRn[9:0].

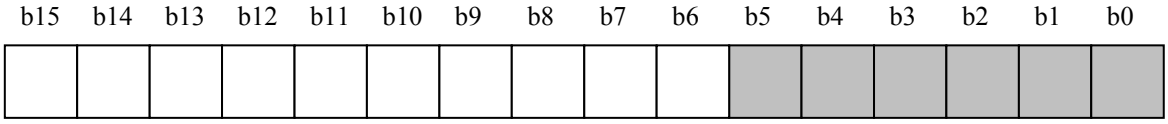
On the H8SX/1668 the 10-bit data is stored: ADDRn[15:6].

5.1.1 RX62N

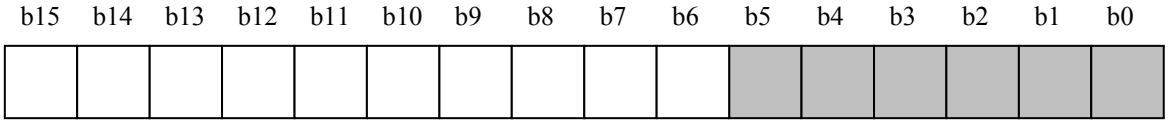
ADDPR.DPSEL = 0



ADDPR.DPSEL = 1

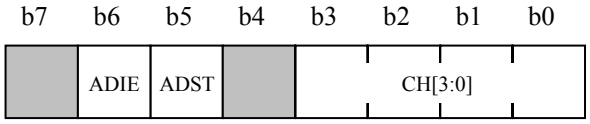


5.1.2 H8SX/1668



5.2 A/D Control/ Status Register: ADCSR

5.2.1 RX62N



Bit	Description
7	Reserved
6	A/D Interrupt Enable Enables/disables the A/D conversion end interrupt
5	A/D Start Starts/stops the A/D Conversion
4	Reserved
[3:0]	Channel Select: Select the analog channels for A/D conversion. In single mode (ADCR.MODE[1:0] = 00b), these bits select a single channel to perform a conversion on. In scan mode (ADCR.MODE[1:0] = 10b or 11b), these bits set the range of channels to perform conversions on.

	Single Mode (ADCR.MODE[1:0] = 00b)	Scan Mode (ADCR.MODE[1:0] = 10b or 11b)
Unit 0	0 0 0 0 – AN0 0 0 0 1 – AN1 0 0 1 0 – AN2 0 0 1 1 – AN3 All other settings prohibited	0 0 0 0 – AN0 0 0 0 1 – AN0 to AN1 0 0 1 0 – AN0 to AN2 0 0 1 1 – AN0 to AN3 All other settings prohibited
Unit 1	0 0 0 0 – AN4 0 0 0 1 – AN5 0 0 1 0 – AN6 0 0 1 1 – AN7 All other settings prohibited	0 0 0 0 – AN4 0 0 0 1 – AN4 to AN5 0 0 1 0 – AN4 to AN6 0 0 1 1 – AN4 to AN7 All other settings prohibited

5.2.2 H8SX/1668

Bit	Description	
7	A/D End Flag Status Flag that indicates the end of A/D conversion	
6	A/D Interrupt Enable Enables/disables the A/D conversion end interrupt	
5	A/D Start Starts/stops the A/D Conversion	
4	Reserved Clock Extension Select Specifies the A/D conversion time in combination with the CKS and CKS0 bits in ADCR	Unit 0 Unit 1
[3:0]	Channel Select: Select the analog channels for A/D conversion. In single mode (ADCR.SCANE = 0), these bits select a single channel to perform a conversion on. In scan mode (ADCR.SCANE = 1), these bits set the range of channels to perform conversions on.	

	Single Mode (ADCR.SCANE = 0)	Scan Mode – four channels (ADCR.SCANE = 1, ADCR.SCANS = 0)
Unit 0	0 0 0 0 – AN0 0 0 0 1 – AN1 0 0 1 0 – AN2 0 0 1 1 – AN3 0 1 0 0 – AN4 0 1 0 1 – AN5 0 1 1 0 – AN6 0 1 1 1 – AN7 All other settings prohibited	0 0 0 0 – AN0 0 0 0 1 – AN0 to AN1 0 0 1 0 – AN0 to AN2 0 0 1 1 – AN0 to AN3 0 1 0 0 – AN4 0 1 0 1 – AN4 to AN5 0 1 1 0 – AN4 to AN6 0 1 1 1 – AN4 to AN7 All other settings prohibited

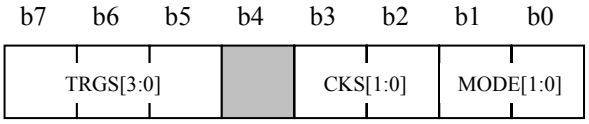
Scan Mode – eight channels (ADCR.SCANE = 1, ADCR.SCANS = 1)

0 0 0 0 – AN0
0 0 0 1 – AN0 to AN1
0 0 1 0 – AN0 to AN2
0 0 1 1 – AN0 to AN3
0 1 0 0 – AN0 to AN4
0 1 0 1 – AN0 to AN5
0 1 1 0 – AN0 to AN6
0 1 1 1 – AN0 to AN7
All other settings prohibited

		Single Mode (ADCR.SCANE = 0)	Scan Mode – four channels (ADCR.SCANE = 1, ADCR.SCANS = 0)
	Unit 1	0 1 0 0 – AN4 0 1 0 1 – AN5 0 1 1 0 – AN6 0 1 1 1 – AN7 All other settings prohibited	0 1 0 0 – AN4 0 1 0 1 – AN4 to AN5 0 1 1 0 – AN4 to AN6 0 1 1 1 – AN4 to AN7 All other settings prohibited Scan Mode – eight channels (ADCR.SCANE = 1, ADCR.SCANS = 1) Mode not prohibited

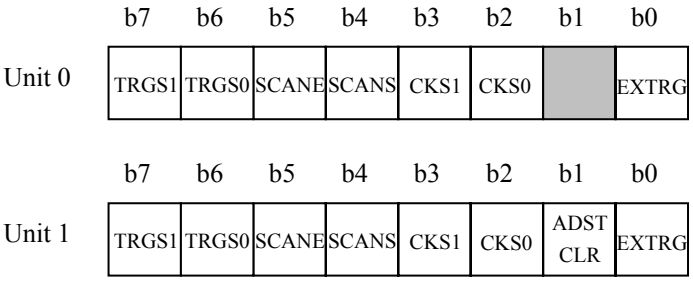
5.3 A/D Control Register: ADCR

5.3.1 RX62N



Bit	Description
[7:5]	Trigger Select 0 0 0 – Software Trigger 0 0 1 – Compare-Match / Input-Capture A Interrupt from MTU0, MTU1, MTU2, MTU3 or MTU4 0 1 0 – Compare-Match A from TMR0 0 1 1 – Trigger from ADTRG0 (ADC Unit 0) – Trigger from ADTRG1 (ADC Unit 1) 1 0 0 – Compare-Match / Input-Capture A Interrupt from MTU0 (ADC Unit 0) – Compare-Match / Input-Capture B Interrupt from MTU0 (ADC Unit 1) 1 0 1 – Compare-Match / Input-Capture A Interrupt from MTU6, MTU7, MTU8, MTU9 or MTU10 1 1 0 – Compare-Match / Input-Capture A Interrupt from MTU4 1 1 1 – Compare-Match / Input-Capture A Interrupt from MTU10
4	Reserved
[3:2]	Clock Select 0 0 – PCLK / 8 0 1 – PCLK / 4 1 0 – PCLK / 2 1 1 – PCLK
[1:0]	Mode Select 0 0 – Single Mode 0 1 – Reserved 1 0 – Continuous Scan Mode 1 1 – One-Cycle Scan Mode

5.3.2 H8SX/1668



Bit	Description	
[7:6] : 0	Trigger Select 0 0 0 – Disables A/D conversion by External Trigger 0 1 0 – Enables A/D conversion by External Trigger from TPU Unit 0 – Reserved 1 0 0 – Enables A/D conversion by External Trigger from TMR Units 0 & 1 – Reserved 1 1 0 – Enables A/D conversion by ADTRG0 pin – Enables A/D conversion by ADTRG1 pin 0 0 1 – External Trigger Disabled – Reserved 0 1 1 – Reserved – External Trigger Disabled 1 0 1 – Reserved – Enables A/D conversion by External Trigger from TMR Units 2 & 3 1 1 1 – Enables A/D conversion by ADTRG0 pin (Units 0 & 1 start Simultaneously)	 Unit 0 Unit 1 Unit 0 Unit 1 Unit 0 Unit 1 Unit 0 Unit 1 Unit 0 Unit 1 Unit 0 Unit 1
[5:4]	Scan Mode 0 0 – Single Mode 0 1 – Single Mode 1 0 – Scan Mode – Channels 1 to 4 1 1 – Scan Mode – Channels 1 to 8 – Reserved	 Unit 0 Unit 1
[3:2]	Clock Select 0 0 – A/D conversion = 528 States 0 1 – A/D conversion = 268 States 1 0 – A/D conversion = 138 States 1 1 – A/D conversion = 73 States EXCKS Bit ↓ 1 0 0 – A/D conversion = 336 States 1 0 1 – A/D conversion = 172 States 1 1 0 – A/D conversion = 90 States 1 1 1 – A/D conversion = 49 States	 Unit 0 Unit 1 Unit 1
1	Reserved A/D Start Clear This bit enables or Disables automatic clearing of the ADST bit in Scan Mode	Unit 0 Unit 1
0	Used in conjunction with bits [7:6]	

5.4 A/D Data Placement Register: ADDPR

5.4.1 RX62N

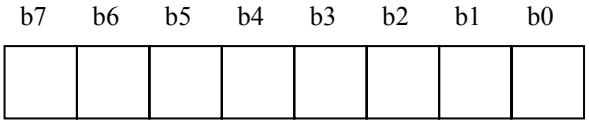
Bit	Description
7	Data Placement Select Selects whether the data in the A/D Data Registers are padded to the LSB or MSB
[6:0]	Reserved

5.4.2 H8SX/1668

The H8SX/1668 does not have an A/D Data Displacement Register; data always appears in ADDRn[15:6].

5.5 A/D Sampling State Register: ADSSTR

5.5.1 RX62N



Bit	Description
[7:0]	

8-bit read/ write register that is used to set the sampling time for analog inputs.
Can be used to adjust the sampling time, when the PCLK is slow or when the signal source impedance is high.

Set a value such that the sampling time ≥ 0.5μs.

The relationship between sampling time, ADSSTR & PCLK is given by:

$$\text{Sampling Time} = \frac{\text{ADSSTR Value}}{\text{ADCLK (MHz)}}$$

5.5.2 H8SX/1668

The H8SX/1668 does not have an A/D Sampling State Register.

6. Usage Notes

6.1 I/O Register Macros

New macros in the iodefine.h for RX family parts make it easier to refer to ICU control registers, module stop registers, DTC enable registers, and interrupt vector numbers by the logical names associated with the peripherals. These macros allow portability across RX family members by hiding specific register and vector numbers. See the documentation contained in iodefine.h for details.

Some examples:

Macro	Usage example
`IR("module name", "bit name")`	`if ( IR(AD0,ADI0) == 1)…`
`IEN("module name", "bit name")`	`IEN(AD0,ADI0) = 1 ;`
`IPR("module name", "bit name")`	`IPR(AD0,ADI0) = 0x02 ;`
`MSTP("module name")`	`MSTP(AD0) = 0 ;`
`VECT("module name", "bit name")`	`#pragma interrupt (MySciTxIsr(vect=VECT(AD0,ADI0))`

6.2 Polling for end of A/D conversion

On the H8SX it is possible to monitor and wait for the end of A/D conversion by waiting for the ADF bit to be set in the A/D Control/Status Register. This allowed software to poll for the end of A/D conversion instead of using interrupts.

On the RX62N, the ADF bit has been removed; however, polled mode is possible using the following method:

- Enable the A/D Interrupt Enable in the A/D converter by setting the ADIE bit in ADCSR. This gates the setting of the IR flag in the Interrupt Control Unit (ICU)
- In the ICU, do not enable the A/D interrupt (leave corresponding bit in the IER register cleared)
- Before starting A/D conversion, clear the interrupt request flag in the ICU by writing a zero to the proper Interrupt Request Register (IRn) in the ICU.
- Start the A/D conversion
- When the A/D conversion finishes the interrupt request will be sent to the ICU, setting the IR bit in the Interrupt Request Register. No interrupt will be generated.
- Software can wait for the IR bit to change to a 1, indicating that the A/D conversion is complete and the results are stored in the A/D Data Registers (ADDRn).

Therefore, it is possible to poll for the end of A/D conversion without using the A/D conversion end interrupt.

6.3 A/D timing differences between RX8S/1668 and RX62N

Analog conversion speed is dictated by:

1. Signal source impedance
2. Peripheral clock (PCLK) speed setting
3. Configuration settings in the ADC subsystem

When moving applications from the H8SX/1668 to the RX62N the effects of each of these must be considered. In general terms, as the peripheral clock speed increases conversion time decreases; as conversion time decreases the source impedance must also decrease.

Conversion time on the H8SX/1668 is specified at 2.7 uS/channel when running with the peripheral clock at its specified maximum of 35 MHz. The RX62N increases the maximum PCLK frequency to 50 MHz. The higher PCLK frequency coupled with the reduced internal capacitance of the ADC results in an improved conversion time of 1.0 uS/channel on the RX62N. This improvement, however, requires that external signal conditioning circuitry meets

certain design criteria. The impedance of the input source signal must be 1k Ohm or less to achieve the 1.0 uS/channel conversion speed of the RX62N.

	RX62N	H8SX/1668
Maximum peripheral clock (PCLK)	50 MHz	35 MHz
Maximum conversion speed	1.0 uS/channel	2.7 uS/channel
Maximum source impedance	1.0k Ohm	5.0k Ohm

As an alternative to modifying the signal conditioning circuitry driving the analog inputs, it is possible adjust the RX62N's ADC timing through software so that legacy hardware remains unaffected. ADC timing may be adjusted by changing the Peripheral Clock (PCLK) base frequency, by using a post-scaled PCLK as the AD timing reference, and by changing the number of timing states that make up an ADC sample.

The base PCLK frequency is set in the Clock Generation Circuit's System Clock Control Register (SCKCR). An optional post-scaler for PCLK may be selected for the ADC using the CKS[1:0] bits of the A/D Control Register, ADCR. The A/D Sampling State Register (ADSSTR) offers a final adjustment over the AD sampling time, allowing the sampling time to grow to accommodate higher impedance circuits or to shrink to account for slow PCLK settings.

For example:

A legacy application is running on an H8SX/1668 using a 12 MHz crystal with a bus speed of 48 MHz and a peripheral clock (PCLK) of 24 MHz. The hardware circuit requires at least 5uS settling time between analog samples.

To move this application to the RX62N using a 12 MHz crystal with a bus speed of 96 MHz and a PCLK of 48 MHz, the registers in the RX62N would be set as follows:

```
SYSTEM.SCKCR.LONG = 0x00020100 ;  /* PCLK=(XTAL x 4)=48 MHz, ICLK=96 MHz, BCLK=24 MHz */
AD0.ADCR.BYTE = 0x0C;             /* AD clock = PCLK = 48 MHz */
AD0.ADSSTR = 240;                 /* Sampling time = (240/48) = 5.0 uS */
```

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Revision Record

Rev.	Date	Description	
		Page	Summary
1.00	Feb.16.2010	—	First edition issued
1.10	Apr.09.2010	—	Update to new Renesas Electronics template
1.15	Sep.30.2010	13	Added section 6.1

General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Handling of Unused Pins

   Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.

   — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

   The state of the product is undefined at the moment when power is supplied.

   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.
   In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

   Access to reserved addresses is prohibited.

   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

   Before changing from one product to another, i.e. to a product with a different part number, confirm that the change will not lead to problems.

   — The characteristics of an MPU or MCU in the same group but having a different part number may differ in terms of the internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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