Introduction

Xilinx® 7 Series FPGAs need a reference clock with relatively stringent requirements. The phase noise requirement is most notable with maximum phase noise levels at 10KHz, 100KHz and 1MHz offsets from the clock carrier frequency. This application note describes how the VersaClock 6 meets all the requirements for the Xilinx 7 Series reference clock.

Phase Noise

The phase noise specification for the Xilinx 7 Series reference clock is stringent enough that not just any clock generator can meet this spec. In the table below, the phase noise requirements are listed, together with the actual performance of VersaClock 6.

The reference clock is used for the Channel PLL's (CPLL) and Quad PLL's (QPLL) inside the FPGA. The QPLL is an LC based PLL that is used for communication channels with the highest line rates. The CPLL is a ring oscillator based PLL that is used for the lower line rates that don't require "LC" noise performance.

Table 1: QPLL and CPLL Requirements

Ref Clock (MHz)	QPLL Phase Noise (dBc)			CPLL Phase Noise (dBc)		
	@10kHz	@100kHz	@1MHz	@10kHz	@100kHz	@1MHz
100	-126	-130	-134	-126	-132	-136
125	-123	-129	-133	-123	-131	-135
156.25	-122	-127	-132	-121	-129	-133
250	-119	-126	-131	-119	-126	-132
312.5	-115	-124	-130	-116	-124	-131
625	-110	-116	-120	-110	-119	-127

VersaClock 6 can generate all the frequencies above except 625MHz.

Table 2: VersaClock 6 Performance. For convenience the QPLL and CPLL requirements are also added to the table.

Ref Clock (MHz)	Xtal (MHz)	VersaClock 6 Phase Noise (dBc) (QPLL (dBc) / CPLL (dBc))		
		@10kHz	@100kHz	@1MHz
100	25.00	-128.1 (-126 / -126)	-133.9 (-130 / -132)	-140.5 (-134 / -136)
125	25.00	-125.9 (-123 / -123)	-131.8 (-129 / -131)	-138.2 (-133 / -135)
156.25	25.00	-123.8 (-122 / -121)	-130.0 (-127 / -129)	-136.3 (-132 / -133)
250	25.00	-120.3 (-119 / -119)	-126.2 (-126 / -126)	-132.2 (-131 / -132)
312.5	31.25	-118.2 (-115 / -116)	-124.2 (-124 / -124)	-131.5 (-130 / -131)

VersaClock 6 meets all the phase noise requirements so it can be used with Xilinx 7 Series FPGAs.

For 100MHz to 250MHz output frequencies a 25MHz crystal is good enough to meet the QPLL and CPLL requirements. For 312.5MHz output frequency a 31.25MHz crystal is needed to achieve the required phase noise levels. A crystal frequency higher than 31.25MHz can be used to improve the phase noise margins.

Table 3: Additional Set of Phase Noise Test Results when using a 39.0625MHz Crystal.

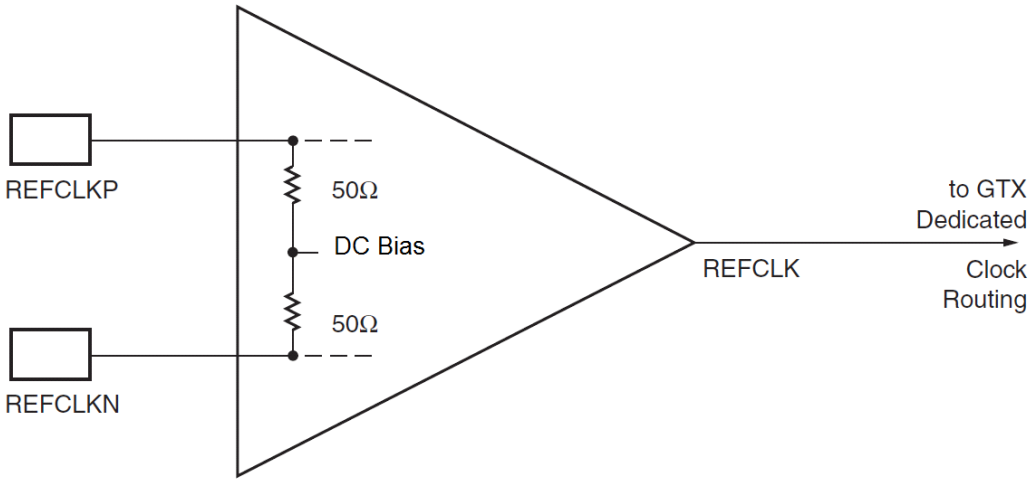
Ref Clock (MHz)	Xtal (MHz)	VersaClock 6 Phase Noise (dBc) (QPLL (dBc) / CPLL (dBc))		
		@10kHz	@100kHz	@1MHz
100	39.0625	-128.5 (-126 / -126)	-135.3 (-130 / -132)	-140.2 (-134 / -136)
125	39.0625	-126.8 (-123 / -123)	-133.4 (-129 / -131)	-138.5 (-133 / -135)
156.25	39.0625	-124.0 (-122 / -121)	-131.2 (-127 / -129)	-137.3 (-132 / -133)
250	39.0625	-120.5 (-119 / -119)	-127.3 (-126 / -126)	-134.9 (-131 / -132)
312.5	39.0625	-118.6 (-115 / -116)	-125.4 (-124 / -124)	-133.0 (-130 / -131)

The CLKIN differential input on VersaClock 6 can also be used to bring in a reference clock. To meet the phase noise requirements when using the CLKIN differential input, it is advised to use a reference clock frequency of 50MHz or higher.

See “Appendix A: Phase Noise Plots” for example phase noise plots, measured with VersaClock 6.

See “Appendix B: Full VersaClock 6 Configuration, Multiple Outputs” for a study with multiple outputs at different frequencies.

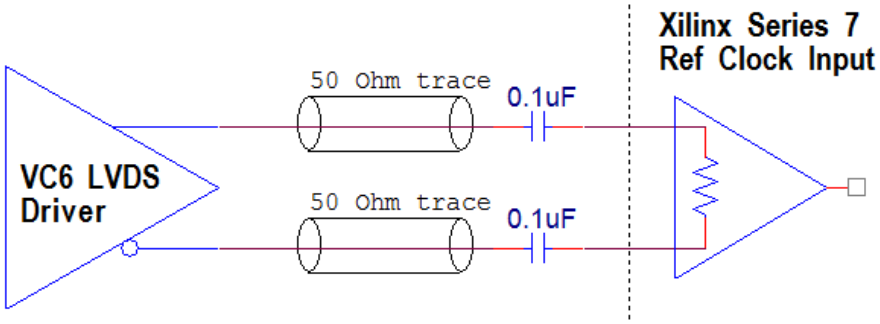
Xilinx FPGA Reference Clock Input



The reference clock input on the Xilinx FPGA has on-chip 100Ω (50Ω + 50Ω) differential termination. The center tab between the two 50Ω resistors is biased internally and Xilinx recommends to AC couple the differential reference clock with typical 100nF capacitors to the REFCLKP and REFCLKN input pair.

Xilinx specifies minimum 250mV and maximum 2000mV, differential peak-to-peak. The best fit for driving the Xilinx 7 Series input is the LVDS logic. The VersaClock 6 datasheet specifies the LVDS levels per single ended output pin and translated to differential, the spec says minimum 494mV and maximum 908mV peak-to-peak. This fits nicely inside the Xilinx input spec.

Recommended circuit when using a VersaClock 6 LVDS output to drive a Xilinx 7 Series reference clock input:



Only the AC coupling capacitors are needed to connect the VersaClock LVDS output to the Xilinx 7 Series FPGA reference clock input.

Conclusion

Phase Noise performance of reference clocks generated by VersaClock 6 meet the phase noise mask requirements of Xilinx 7 Series FPGAs.

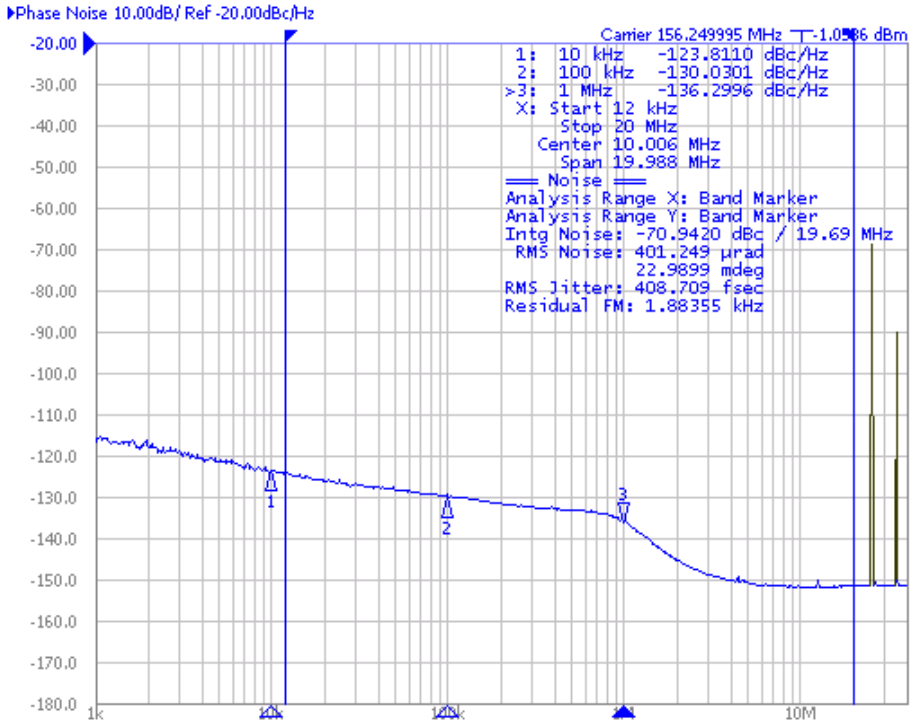
Waveform requirements can be met easily with the LVDS logic type.

References

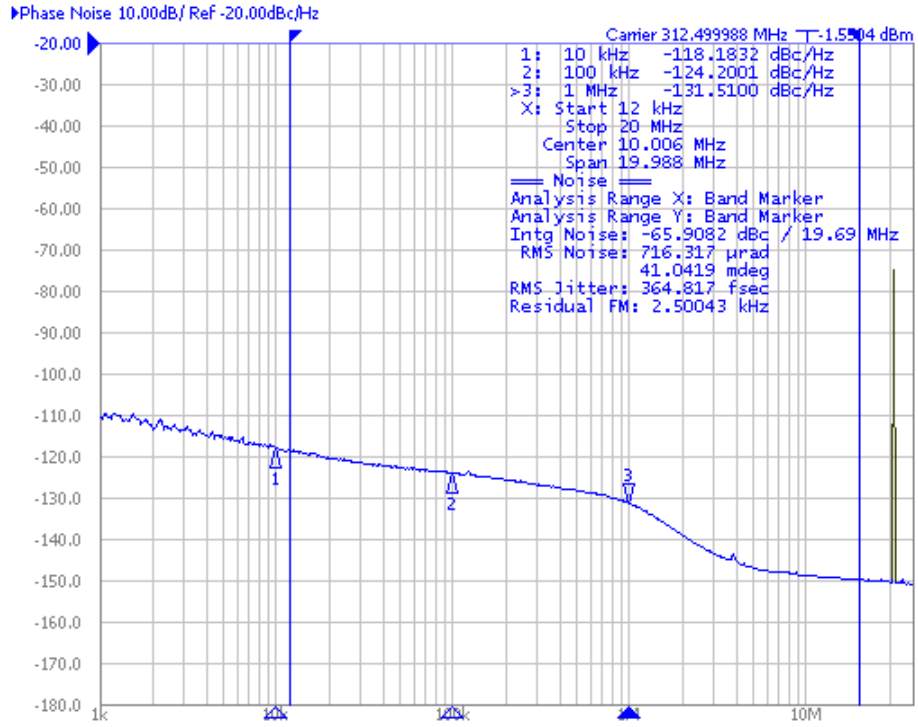
- Xilinx 7 Series FPGAs GTX/GTH Transceivers, User Guide (UG476)
- Xilinx 7 Series FPGAs Overview (DS180)
- Xilinx 7 Series Datasheets for Kintex (DS182) and Virtex (DS183)
- Xilinx 7 Series Phase Noise masks: http://www.xilinx.com/support/answers/44549.html

Appendix A: Phase Noise Plots

Example A1: 156.25MHz LVDS clock, generated by VersaClock 6 with a 25MHz crystal



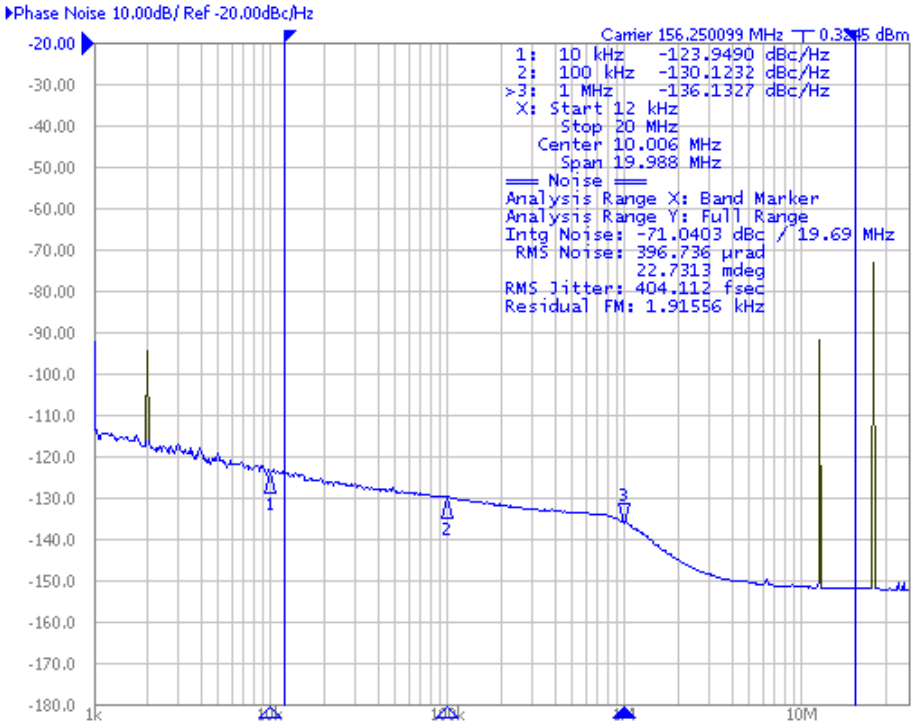
Example A2: 312.5MHz LVDS clock, generated by VersaClock 6 with a 31.25MHz crystal



Appendix B: Full VersaClock 6 Configuration, Multiple Outputs

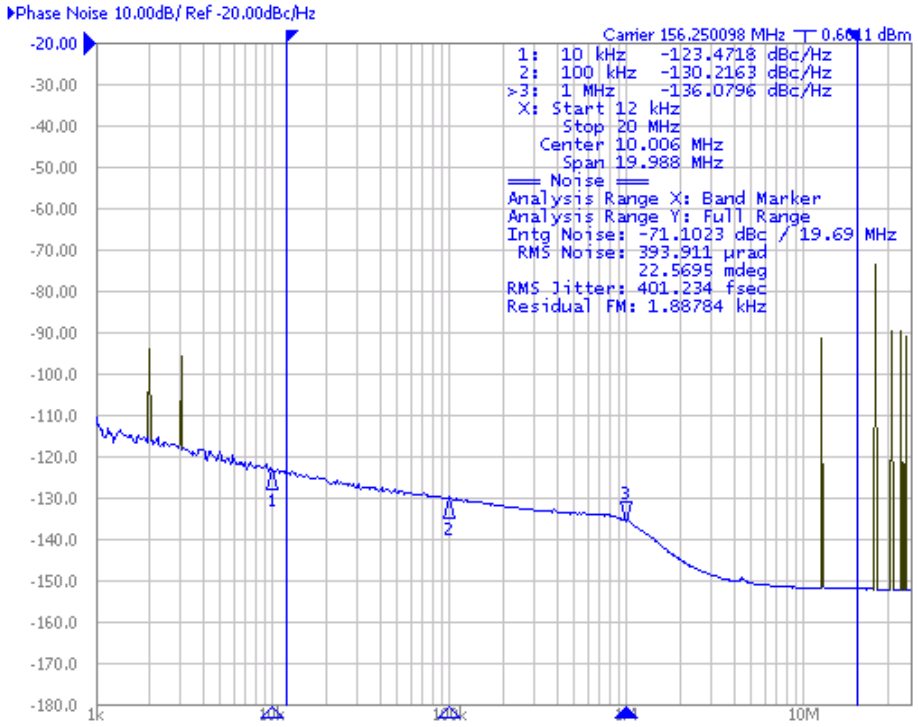
Most applications will use one output for driving a Xilinx 7 Series FPGA and other outputs for other purposes. The other outputs will have different frequencies and mixing of the output signals causes spurs in the phase noise plot and jitter. The following phase noise plots show a few example combinations. In all plots we look at a 156.25MHz clock while different frequencies are present on other outputs. For this study a 25MHz crystal was used and all outputs have LVDS logic.

Example B1: 156.25MHz for FPGA and 100MHz for PCI Express®



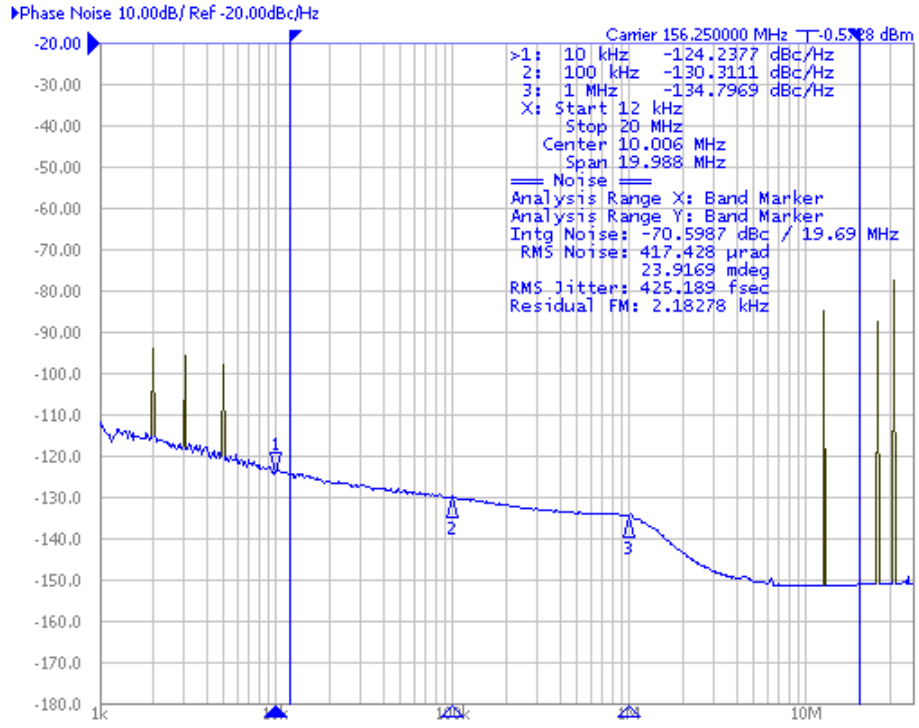
Adding one output at 100MHz causes a 12.5MHz spur but this spur is below -90dBc and does not contribute significantly to the 12K~20M phase jitter. Phase Noise levels at 10KHz, 100KHz and 1MHz are unaffected. This combination is perfect for the 5P49V6913 with two differential outputs.

Example B2: 156.25MHz for FPGA, 2 X 100MHz for PCI Express and 125MHz for Giga Bit Ethernet



A few spurs appear above 30MHz but still no significant contribution to phase jitter or phase noise levels. This combination is perfect for the 5P49V6901 with four differential outputs.

Example B3: 100MHz, 125MHz, 156.25MHz and 250MHz



In this case the 12.5MHz spur is a little bit stronger, causing the phase jitter to increase to 425fs. Phase Noise levels at 10KHz, 100KHz and 1MHz are still unaffected. This combination is perfect for the 5P49V6901 with four differential outputs.

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