Typical Performance Characteristics - 50Ω Performance

Figure 14. RF1 to RFC Insertion Loss

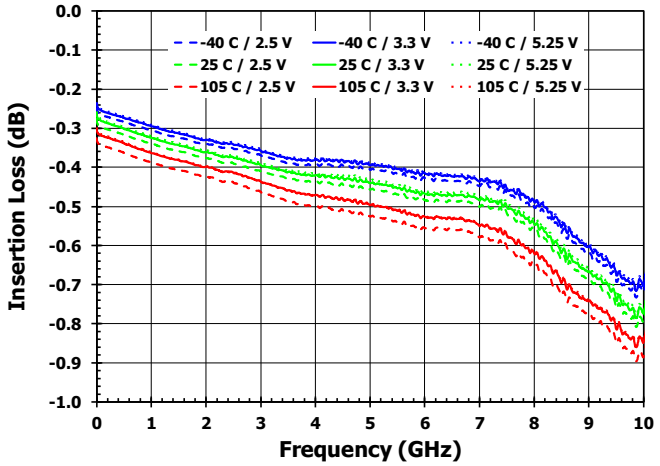


Figure 15. RF2 to RFC Insertion Loss

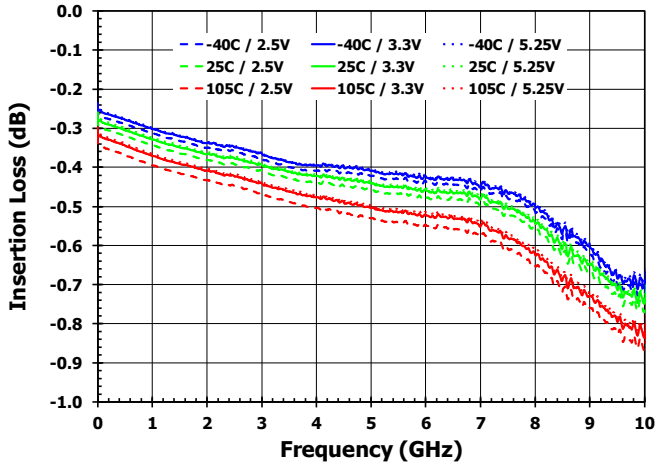


Figure 16. RF1 to RFC Isolation [RF2 On State]

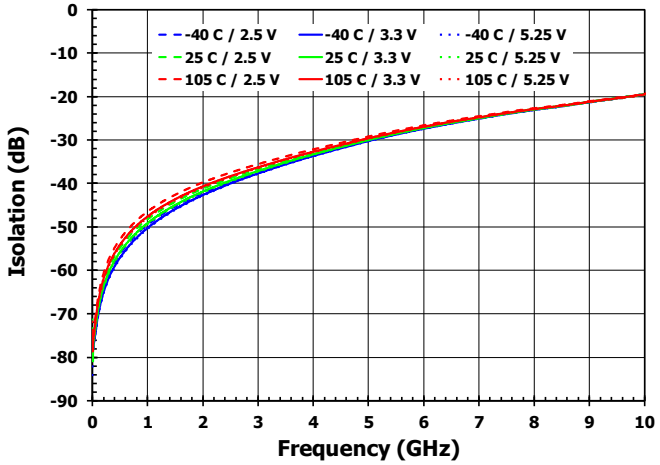


Figure 17. RF2 to RFC Isolation [RF1 On State]

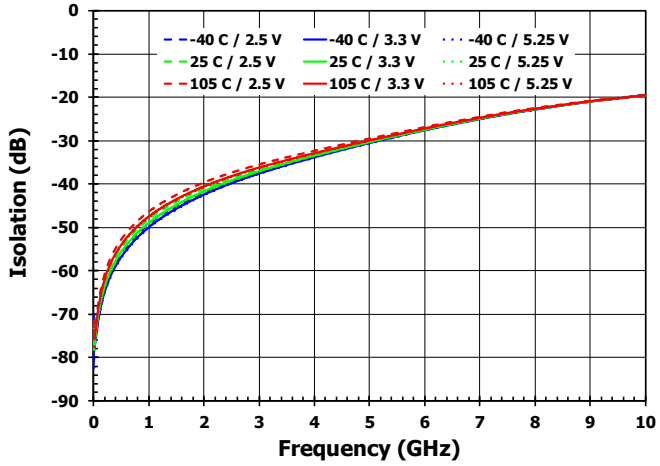


Figure 18. RF1 to RF2 Isolation [RF1 On State]

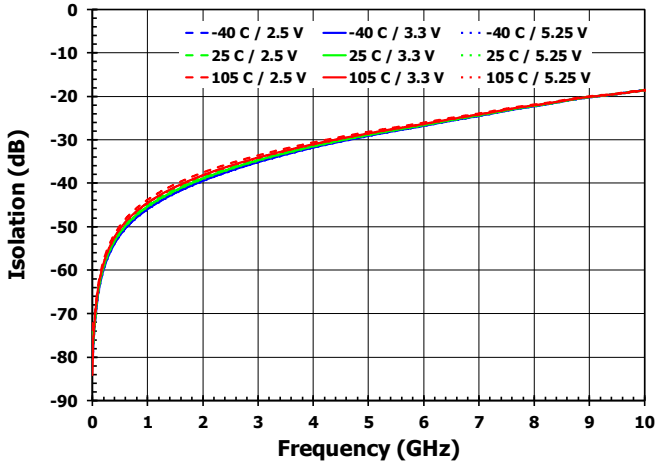
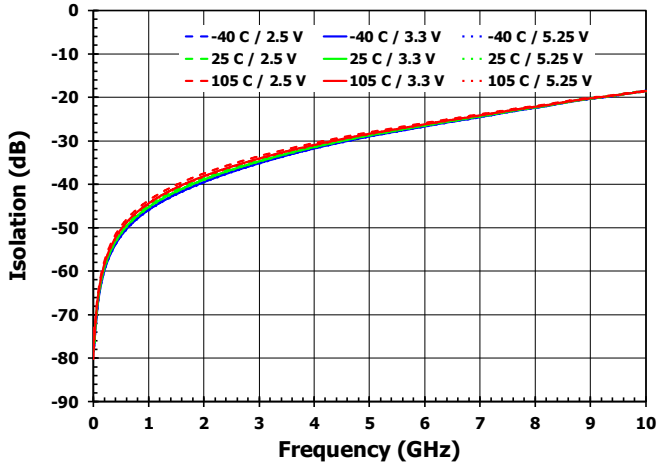


Figure 19. RF1 to RF2 Isolation [RF2 On State]



Typical Performance Characteristics - 50Ω Performance

Figure 20. RFC Return Loss [RF1 On State]

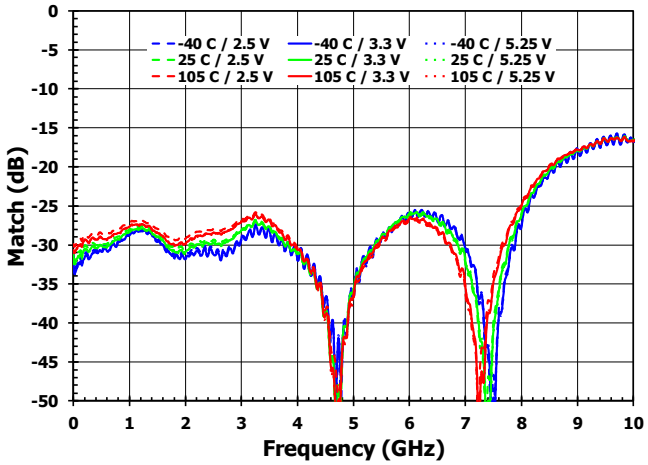


Figure 21. RFC Return Loss [RF2 On State]

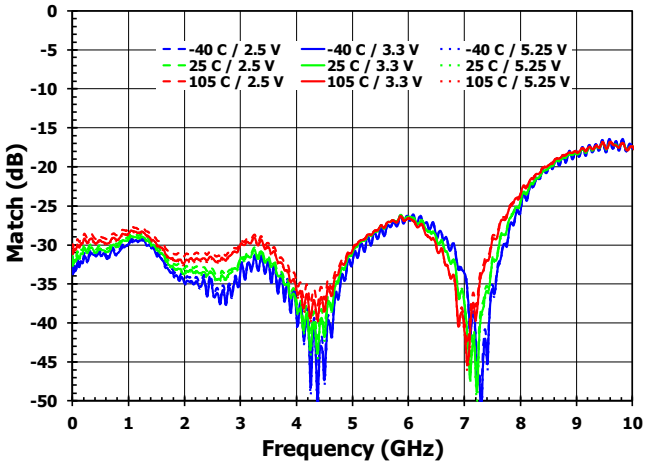


Figure 22. RF1 Return Loss [RF1 On State]

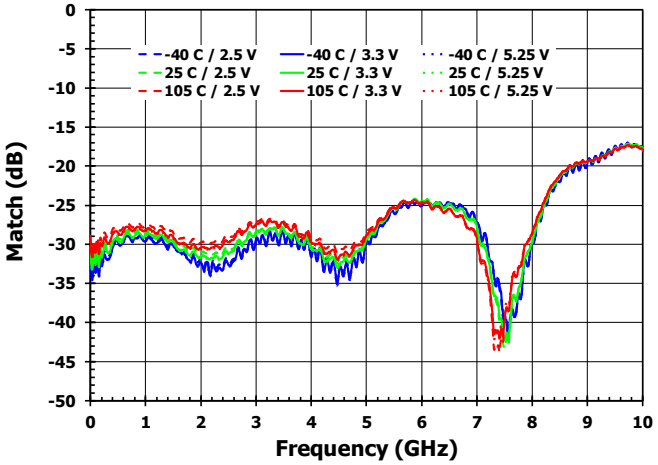


Figure 23. RF2 Return Loss [RF2 On State]

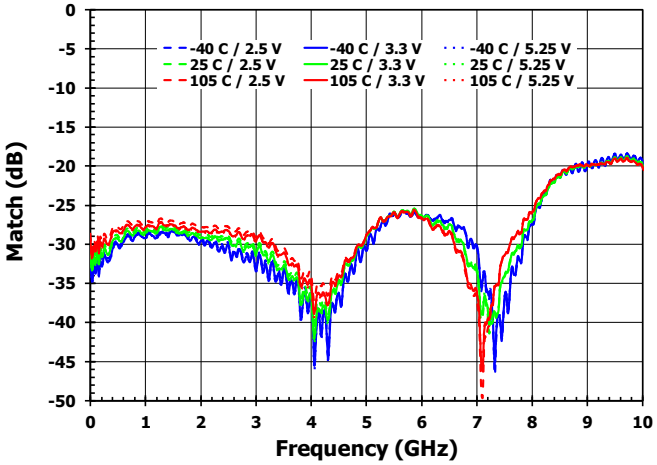


Figure 24. Switching Time [Isolation to Insertion Loss State]

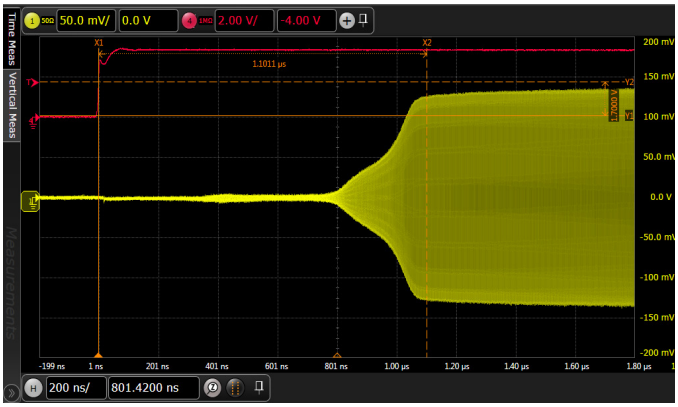


Figure 25. Switching Time [Insertion Loss to Isolation State]

Control Mode

Table 9. Switch Control Truth Table

V_{CTL} (pin 7)	EN (pin 8)	Switch State
LOW	HIGH	RFC to RF1 Insertion Loss State
HIGH	HIGH	RFC to RF2 Insertion Loss State
Don't Care	LOW	Standby

Application Information

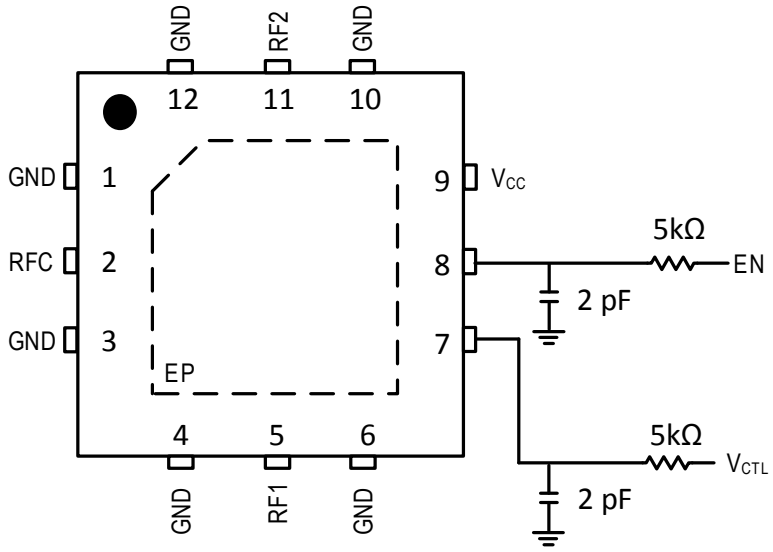
Power Supplies

A common V_{CC} power supply should be used for all pins requiring DC power. All supply pins should be bypassed with external capacitors to minimize noise and fast transients. Supply noise can degrade noise figure and fast transients can trigger ESD clamps and cause them to fail. Supply voltage change or transients should have a slew rate smaller than 1V / 20µs. In addition, all control pins should remain at 0V (+/-0.3V) while the supply voltage ramps up or while it returns to zero.

Control Pin Interface

If control signal integrity is a concern and clean signals cannot be guaranteed due to overshoot, undershoot, ringing, etc., the following circuit at the input of each control pin is recommended. This applies to control pins 7 and 8 as shown below.

Figure 26. Control Pin Interface Schematic



75Ω Evaluation Kit Picture

Figure 27. Top View (75Ω)

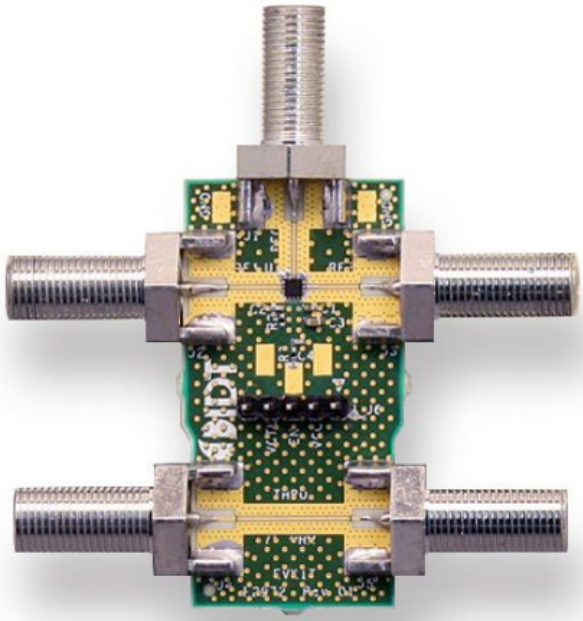
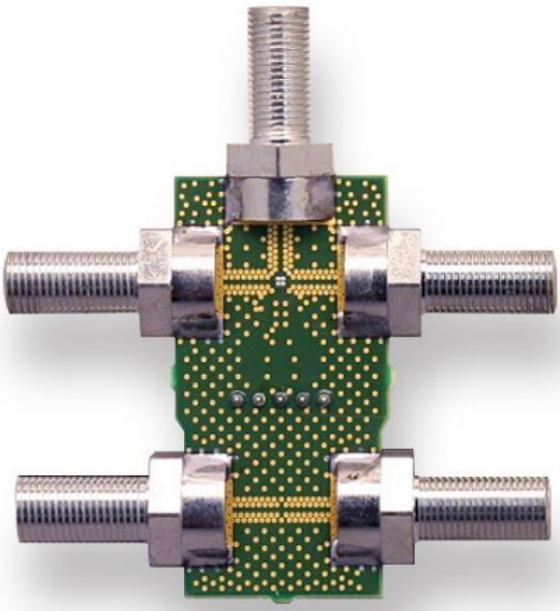


Figure 28. Bottom View (75Ω)



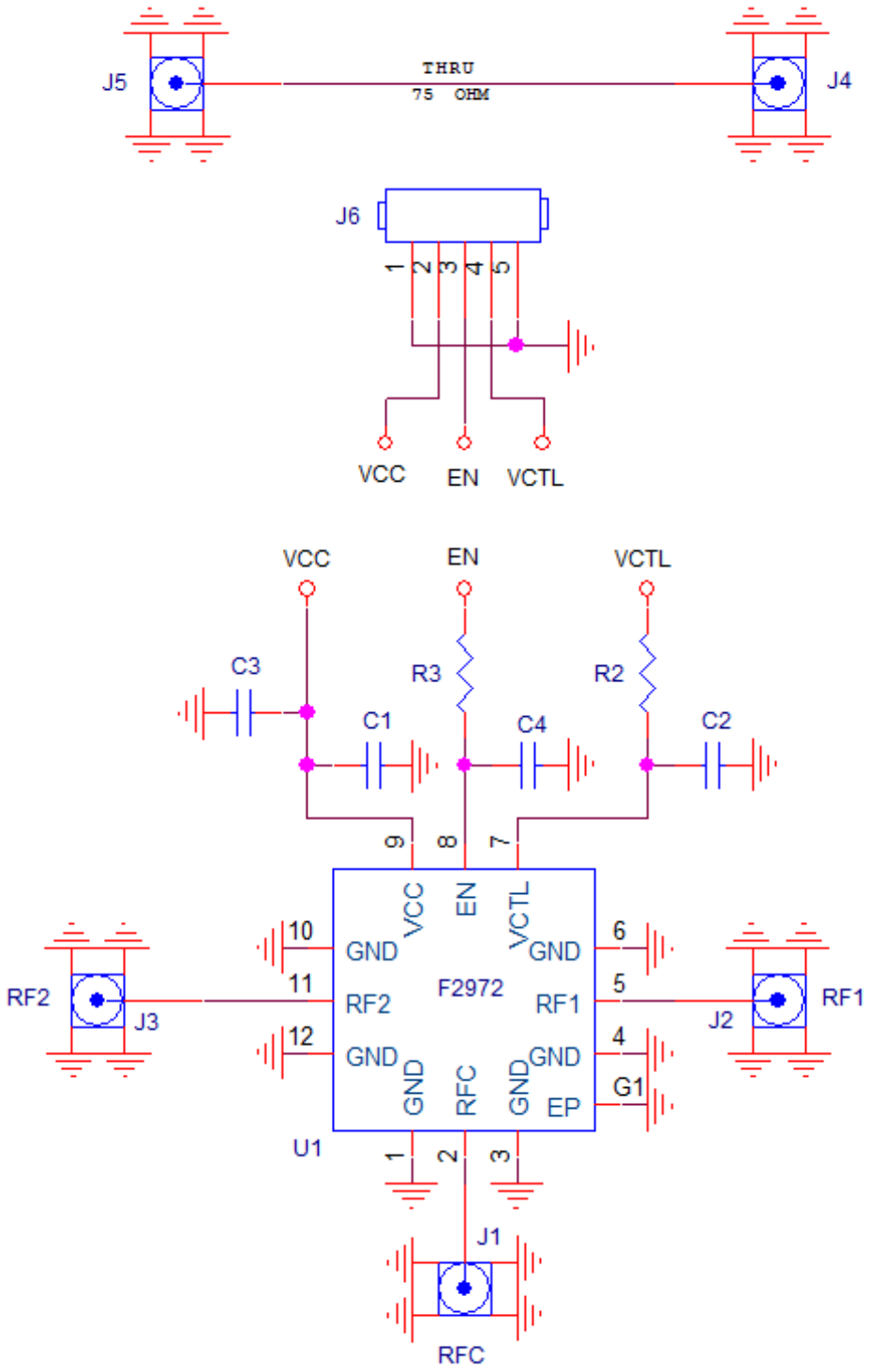
50Ω Evaluation Kit Picture

Figure 29. Top View (50Ω)

Figure 30. Bottom View (50Ω)

75Ω Evaluation Kit / Applications Circuit

Figure 31. Electrical Schematic (75Ω)



50Ω Evaluation Kit / Applications Circuit

Figure 32. Electrical Schematic (50Ω)

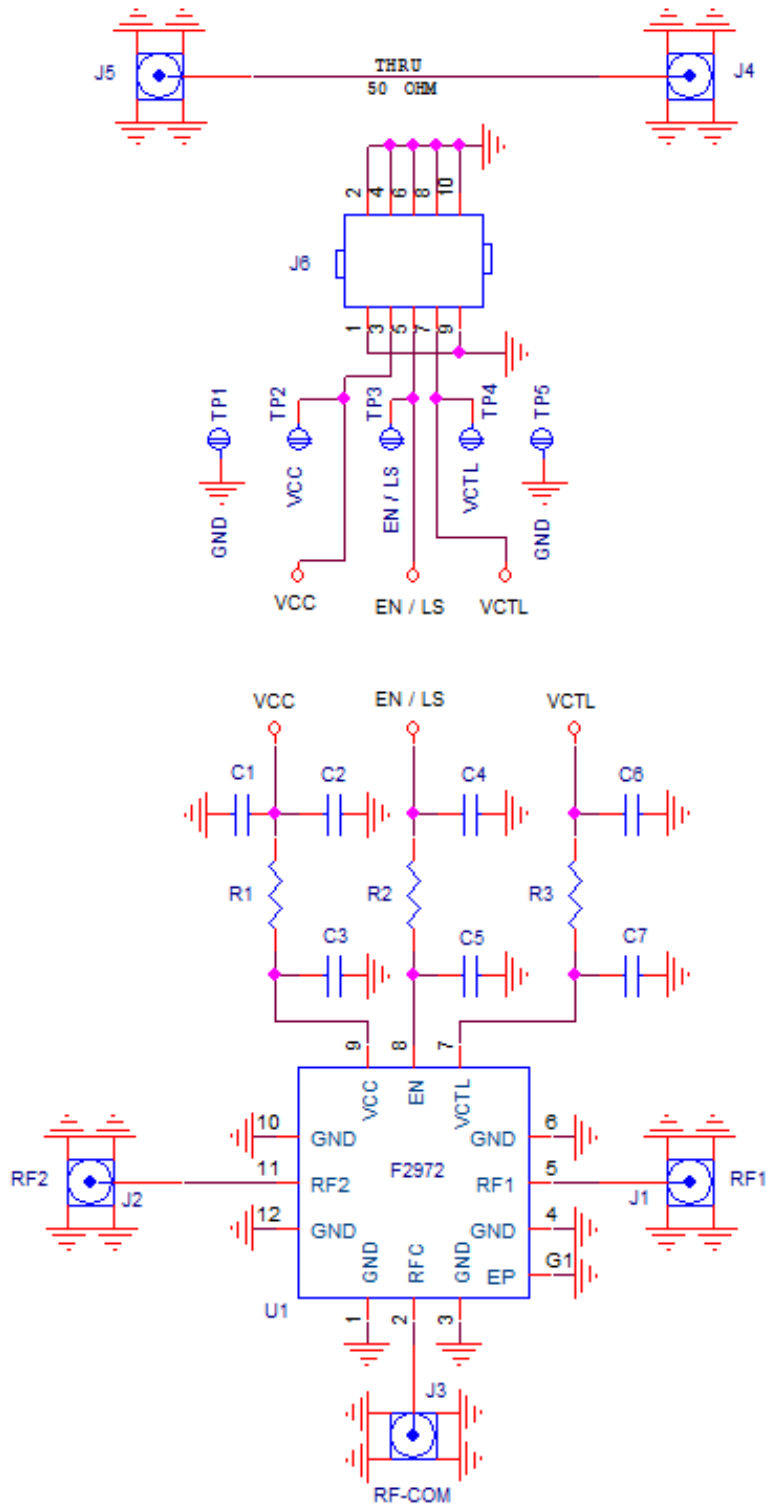


Table 10. 75Ω Bill of Material (BOM)

Part Reference	QTY	Description	Manufacturer Part #	Manufacturer
C1	1	0.1µF ±10%, 16V, X7R, Ceramic Capacitor (0402)	GRM155R71C104KA88D	Murata
C2, C4	2	100pF ±5% 50V, C0G, Ceramic Capacitor (0402)	GRM1555C1H101JA01D	Murata
C3	1	0.01µF ±5% 50V, X7R, Ceramic Capacitor (0603)	GRM188R71H103JA01D	Murata
R2, R3	2	100Ω 1/10W, Resistor (0402)	ERJ-2RKF1000X	Panasonic
J1 – J5	5	F-Type Edge Mount	222181	Amphenol RF
J6	1	Conn Header Vert 5x1 Pos Gold	68002-205HLF	Amphenol FCI
U1	1	SP2T Switch 2mm x 2mm 12-pin TQFN	F2972NEGK	IDT
	1	Printed Circuit Board	F2972 75Ω PCB	IDT

Table 11. 50Ω Bill of Material (BOM)

Part Reference	QTY	Description	Manufacturer Part #	Manufacturer
C1 – C7	0	Not Installed (0402)		
R1– R3	3	0Ω 1/10W, Resistor (0402)	ERJ-2GE0R00X	Panasonic
J1 – J5	5	SMA Edge Mount	142-0761-881	Cinch Connectivity
J6	1	Conn Header 10 Pos 0.100” Str 15 Au	68602-210HLF	Amphenol FCI
TP1, TP2, TP3, TP4, TP5	0	Not Installed Test Point Loop		
U1	1	SP2T Switch 2mm x 2mm 12-pin TQFN	F2972NEGK	IDT
	1	Printed Circuit Board	F2972 50Ω PCB	IDT

Evaluation Kit (EVKit) Operation

External Supply Setup

Set up a V_{CC} power supply in the voltage range of 2.5V to 5.25V with the power supply output disabled.

For the 75Ω EVKit, connect the disabled Vcc supply connection to J6 pin 2 and GND to J6 pins 1 or 5.

For the 50Ω EVKit, connect the disabled Vcc supply connection to J6 pin 3 and GND to J6 pin 1, 2, 4, 6, 8, 9, or 10.

Logic Control Setup

With the logic control lines disabled set the HIGH and LOW logic levels to satisfy the levels stated in the electrical specifications table.

For the 75Ω EVKit, connect the disabled logic control lines to J6 EN (pin 3) and V_{CTL} (pin 4).

For the 50Ω EVKit, connect the disabled logic control lines to J6 EN / LS (pin 5) and V_{CTL} (pin 7).

See Table 9 for the logic truth table.

Turn On Procedure

Setup the supplies and EVKit as noted in the External Supply Setup and Logic Control Setup sections above.

Enable the V_{CC} supply.

Enable the logic control signals.

Set the logic setting to achieve the desired Table 9 configuration. Note that external control logic should not be applied without V_{CC} being present.

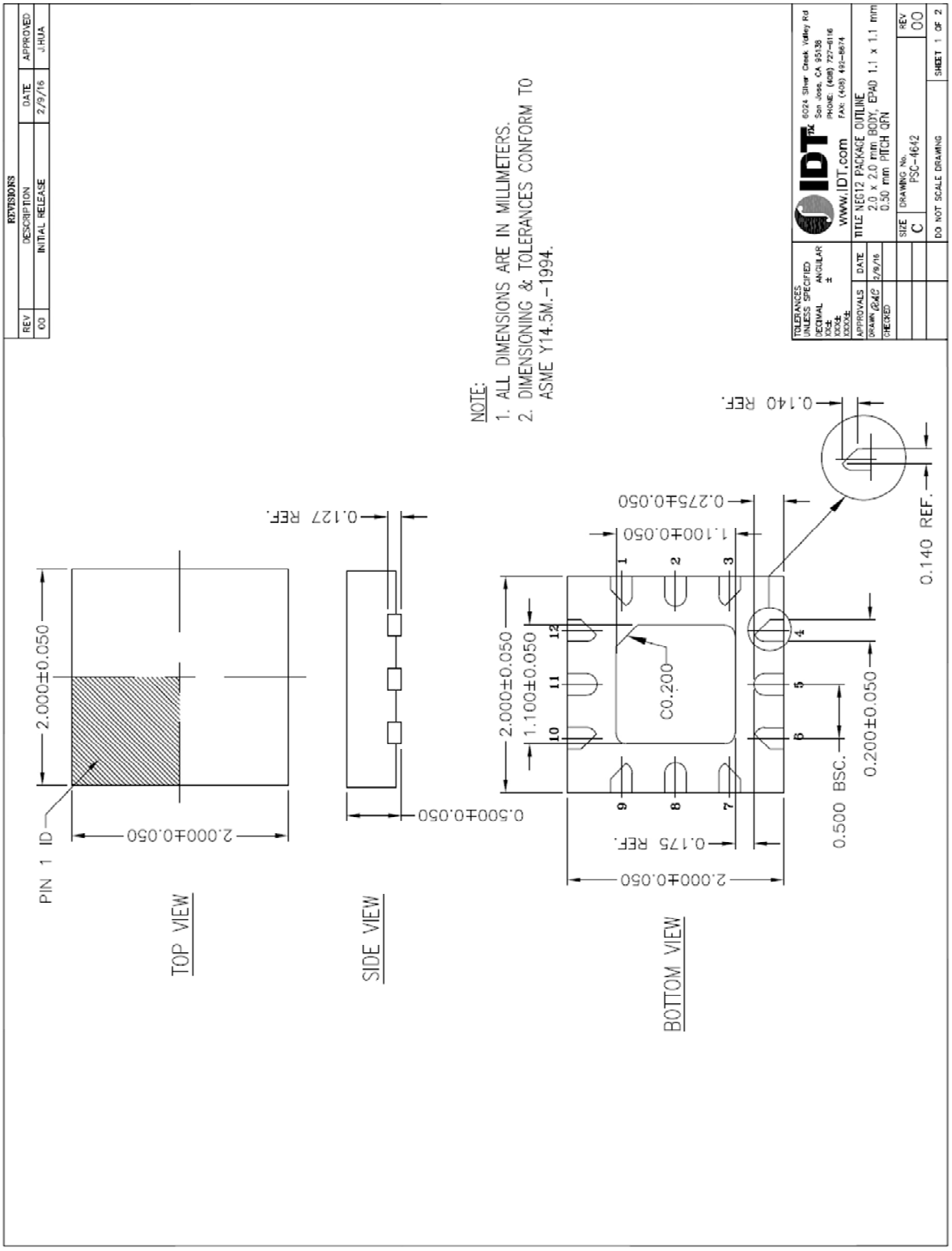
Turn Off Procedure

Set the logic control pins to a logic LOW.

Disable the V_{CC} supply.

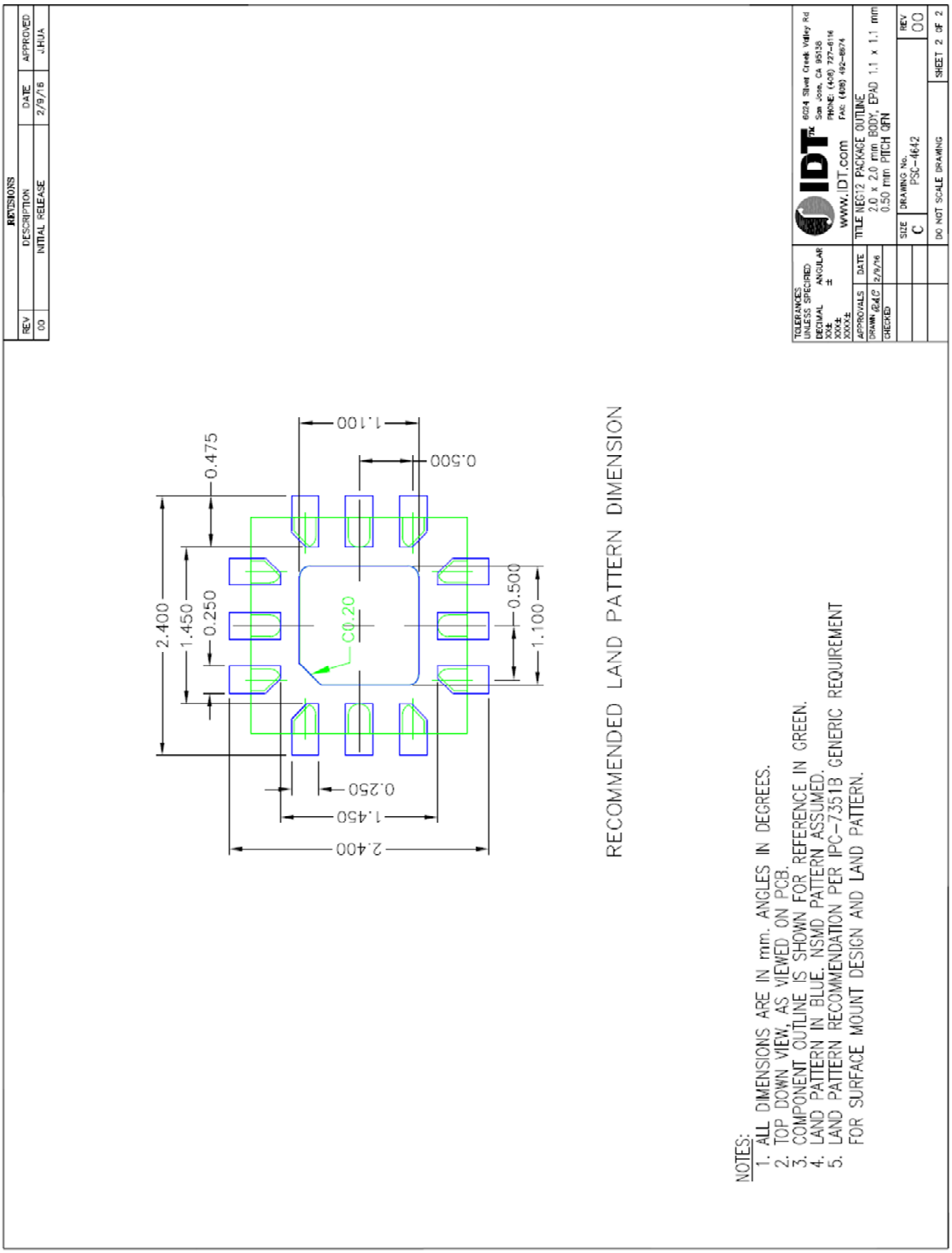
Package Drawings

Figure 33. Package Outline Drawing NEG12 PSC-4642

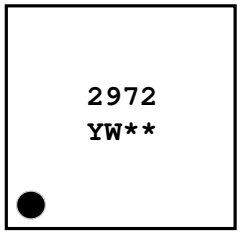


Recommended Land Pattern

Figure 34. Recommended Land Pattern NEG12 PSC-4642



Marking Diagram



Line 1 - 2972 = Abbreviated part number.
Line 2 - Y = Year code.
Line 2 - W = Work week code.
Line 2 - ** = Sequential alpha for lot traceability.

Ordering Information

Orderable Part Number	Package	MSL Rating	Shipping Packaging	Temperature
F2972NEGK	2mm x 2mm x 0.5mm 12-VFQFP-N	MSL1	Cut Reel	-40°C to +105°C
F2972NEGK8	2mm x 2mm x 0.5mm 12-VFQFP-N	MSL1	Tape and Reel	-40°C to +105°C
F2972EVBI-75OHM	75Ω Evaluation Board			
F2972EVBI-50OHM	50Ω Evaluation Board			

Revision History

Revision	Revision Date	Description of Change
Rev O	2017-Apr-19	Initial Release