RE01 Group

Differences Between 1500KB Products and 256KB Products

Summary

This application note is a reference document to summarize the differences in peripheral functions between the 1500KB and 256KB RE01 products. This document describes the differences in I/O registers and pin functions, and indicates points to be noted regarding their use.

Except where noted, this application note compares 1500KB product with the 100-pin LFQFP package and 256KB products with the 100-pin LFQFP package. For specification differences relating to electrical characteristics, points to be noted and design procedures, refer to the individual user's manuals.

Target Device

RE01 group (1500KB products & 256KB products)

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1. Comparison of Incorporated Functions

The following is a comparison of the built-in functions. For details on the functions, refer to the RE01 Group Products with 1.5-Mbyte Flash Memory User's Manual: Hardware Rev. 1.00 (R01UH0796EJ0100) and RE01 Group Products with 256-KB Flash Memory User's Manual: Hardware Rev. 0.80 (R01UH0894EJ0080).

Table 1.1 shows a comparison of the incorporated functions.

Table 1.1 Comparison of Functions between 1500KB and 256KB

Function	1500KB Product	256KB Product
CPU	O	
Startup Modes	Δ	
Reset	Δ	
Option-Setting Memory	Δ	
Low Voltage Detection (LVD)	O	
Clock Generation Circuit	Δ	
Clock Correction Circuit (CCC)	O	
Clock Frequency Accuracy Measurement Circuit (CAC)	Δ	
Power-Saving Functions	Δ	
Energy harvesting controller (EHC)	Δ	
Register write protection function	Δ	
Exception handling	O	
Interrupt Controller Unit (ICU)	Δ	
Key Interrupt Function (KINT)	O	
Bus	Δ	
Memory Protection Unit (MPU)	O	
DMA Controller (DMAC)	O	
Data Transfer Controller (DTC)	O	
Event Link Controller (ELC)	Δ	
I/O port	Δ	
Multi-function Pin Controller (MPC)	Δ	
Port Output Enable for GPT (POE)	Δ	
General PWM Timer (GPT)	O	
Low-speed pulse generator (LPG)	O	x
Asynchronous general-purpose timer (AGT)	O	
Asynchronous general-purpose timer W (AGTW)	x	O
8-bit timer (TMR)	O	
Wakeup timer (WUPT)	x	O
Realtime Clock (RTC)	Δ	
Low-speed clock timer (LST)	O	
Watchdog timer (WDT)	O	
Independent watchdog timer (IWDT)	O	
USB2.0FS host/function module (USB)	O	x
Serial communication interface (SCIg, SCIi)	O	
IrDA interface	O	
I^2C bus interface (RIIC)	O	
Serial peripheral interface (SPI)	O	
Quad serial peripheral interface (QSPI)	O	
CRC calculator (CRC)	O	
Division circuit (DIV)	O	
Data inversion circuit (DIL): 1500KB products, Data conversion circuit (DIL): IO	Δ	

Function	1500KB Product	256KB Product
LED driver (LED)	O	x
MIP LCD Controller (MLCD)	Δ	
2D graphics data conversion circuit (GDT)	O	
Boundary scan	O	
Trusted Secure IP Lite (TSIP-Lite)	O	
14-bit A/D converter (S14AD)	Δ	
Reference voltage generation circuit (VREF)	O	
12-bit D/A converter (R12DA)	O	x
Temperature sensor (TEMPS)	O	
Analog comparator (ACMP)	O	x
Motor driver control circuit (MTDV)	O	x
Data operation circuit (DOC)	O	
Memory mirror function (MMF)	O	
RAM	Δ	
Flash memory	Δ	

O: Function incorporated, x: Function not incorporated, Δ: Differences in functions for 1500KB and 256KB

2. Comparison of Specifications

2.1 Startup Modes

Table 2.1 is a summary comparison of CPU specifications.

Table 2.1 Comparison of Startup Mode Specifications

Item	1500KB Product	256KB Product
Operating mode determined by the mode setting pins	Single chip mode	Single chip mode
	Boot mode (SCI interface)	Boot mode (SCI interface)
	Boot mode (USB interface)	—

2.2 Resets

Table 2.2 summarizes a comparison of reset specifications; Table 2.3 compares the reset registers.

Table 2.2 Comparison of Reset Specifications

Parameter	1500KB Product	256KB Product
MINPWON mode reset	MINPWON mode reset occurs when the following events occur. • Power supply mode changes from minimum power supply mode (MINPWON) to flash-excluded power supply mode (EXFPWON).	MINPWON mode reset occurs when the following events occur. • Power supply mode changes from minimum power supply mode (MINPWON) to flash-excluded power supply mode (EXFPWON). • There is a transition from all-power mode (ALLPWON) to software standby mode of minimum-power mode (MINPWON), and software standby mode is cancelled. • There is a transition from flash-excluded power supply mode (EXFPWON) to software standby mode of minimum-power mode (MINPWON), and software standby mode is cancelled

Reset Source of RTC for 256KB product has been changed. It only can be reset RTC registers by Power-on reset. Thus, it can keep counting even some reset happened except Power-on reset.

Table 2.3 Comparison of Targets to be Initialized by Each Reset Source

Target to be Initialized	Reset Source	1500KB Product	256KB Product
Registers related to the RTC (e.g. RSECCNT, RMINCNT and so on Registers)	RES# pin reset	O	x
	Power-on reset	O	O
	Voltage monitor 0 reset	O	x
	Independent watchdog timer reset	O	x
	Watchdog timer reset	O	x
	Voltage monitor 1 reset, a voltage monitor BAT reset	O	x
	Software reset	O	x
	Bus master MPU error reset	O	x
	Bus slave MPU error reset	O	x
	Stack pointer error reset	O	x
	MINPWON mode reset	O	x
	Deep software standby reset	O	x

O: Function incorporated, x: Function not incorporated

LDOCR register is changed reset source too.

Target to be Initialized		Reset Source	1500KB Product	256KB Product
Registers related to the functions for reducing power consumption	LDOCR	RES# pin reset	O	O
		Power-on reset	O	O
		Reset sequence WDT reset	x	x
		Voltage monitor 0 reset	x	O
		Independent watchdog timer reset	x	x
		Watchdog timer reset	x	x
		Voltage monitor 1 reset, a voltage monitor BAT reset	x	x
		Software reset	x	x
		Bus master MPU error reset	x	x
		Bus slave MPU error reset	x	x
		Stack pointer error reset	x	x
		MINPWON mode reset	x	x
		Deep software standby reset	x	x

O: Function incorporated, x: Function not incorporated

2.3 Option-Setting Memory

Table 2.4 compares the option-setting memory registers.

Table 2.4 Comparison of Option-Setting Memory Registers

Register	Bit	1500KB Product	256KB Product
OFS1	VBATSEL	Secondary Battery (VBAT) Charging Voltage Select 0: Select 2.6 V for charging VBAT 1: Select 3.0 V for charging VBAT	—
	VBATSEL[2:0]	—	Secondary Battery (VBAT) Charging Voltage Select b14 b12 0 0 0: Select V_{batc_0} (2.4V) 0 0 1: Select V_{batc_1} (2.5V) 0 1 0: Select V_{batc_2} (2.6V) 0 1 1: Select V_{batc_3} (2.7V) 1 0 0: Select V_{batc_0} (2.8V) 1 0 1: Select V_{batc_1} (2.9V) 1 1 0: Select V_{batc_2} (3.0V) 1 1 1: Select V_{batc_3} (3.1V)
	SLPWMN	—	Flash memory power reduction function 0: Enabled flash memory current consumption reduction function in low leakage current mode. 1: Disabled flash memory current consumption reduction function in low leakage current mode.

2.4 Clock Generation Circuit

Table 2.5 summarizes a comparison of clock generation circuit specifications; Table 2.6 compares the clock generation circuit registers.

Table 2.5 Comparison of Clock Generation Circuit Specifications

Item	1500KB Product	256KB Product
PLL circuit (PLL)	Available	Not available
High-speed on-chip oscillator (HOCO)	• Oscillation frequency: 24/32/48/64 MHz • Oscillation stabilization wait circuit: Available	• Oscillation frequency: 24/32/48/64 MHz • Oscillation stabilization wait circuit: Available • FLL function: Available
Specification of clock generation circuit (internal clock)	USB clock (UCLK)	-
	-	WUPT (WUPY32K)
	-	CPU-OCD clock (OCDCLK)
	MTDV clock (MOTOR32K)	-

Table 2.6 Comparison of Clock Generation Circuit Registers

Register	Bit	1500KB Product	256KB Product
SCKSCR	CKSEL[2:0]	b2 b0 0 0 0 : HOCO 0 0 1 : MOCO (initial value) 0 1 0 : LOCO 0 1 1 : Main clock oscillator 1 0 0 : Sub-clock oscillator 1 0 1 : PLL Settings other than the above are prohibited.	b2 b0 0 0 0 : HOCO 0 0 1 : MOCO (initial value) 0 1 0 : LOCO 0 1 1 : Main clock oscillator 1 0 0 : Sub-clock oscillator Settings other than the above are prohibited.
PLLCCR	—	PLL clock control register	—
PLLCR	—	PLL control register	—
FLLCR1	—	—	FLL control register 1
OSCSF	b2-b1, b4	Reserved These bits are read as 0. The write value should be 0.	Reserved These bits are read as 0.
	PLLSF	PLL clock oscillation stabilization flag	—
	b7-b6	Reserved These bits are read as 0. The write value should be 0.	Reserved These bits are read as 0.

2.5 Clock Frequency Accuracy Measurement Circuit

Table 2.7 compares the clock frequency accuracy measurement circuit registers.

Table 2.7 Comparison of Clock Frequency Accuracy Measurement Circuit Registers

Register	Bit	1500KB Product	256KB Product
CAICR	FERRFCL	FERRF flag clear Setting the FERRFCL bit to 1 clears the CASTR.FERRF flag. This bit is read as 0.	FERRF flag clear Setting the FERRFCL bit to 1 clears the CASTR.FERRF flag.
	MENDFCL	MENDF clear Setting the MENDFCL bit to 1 clears the CASTR.MENDF flag. This bit is read as 0.	MENDF clear Setting the MENDFCL bit to 1 clears the CASTR.MENDF flag.
	OVFFCL	OVFF clear Setting the OVFFCL bit to 1 clears the CASTR.OVFF flag. This bit is read as 0.	OVFF clear Setting the OVFFCL bit to 1 clears the CASTR.OVFF flag.

2.6 Power-Saving Functions

Table 2.8 summarizes a comparison of power-saving functions; Table 2.9 compares the power-saving function registers.

Table 2.8 Comparison of Power-Saving Functions

Item	1500KB Product	256KB Product
Power control modes	Power consumption can be reduced in operating (OPE), sleep (SLEEP), software standby (SSTBY) and snooze (SNOOZE) modes by selecting an appropriate power control mode according to the operating frequency. • Boost mode (BOOST): Max 64 MHz • Normal mode (NORMAL): Max 32 MHz — High-speed mode: Max 32 MHz — Low-speed mode: Max 2 MHz — Subosc-Speed mode: Max 32.768 kHz • Low leakage current mode (VBB): Max 32.768 kHz	Power consumption can be reduced in operating (OPE), sleep (SLEEP), software standby (SSTBY) and snooze (SNOOZE) modes by selecting an appropriate power control mode according to the operating frequency. • Boost mode (BOOST): Max 64 MHz • Normal mode (NORMAL): Max 32 MHz — High-speed mode: Max 32 MHz — Low-speed mode: Max 2 MHz • Low leakage current mode (VBB): Max 32.768 kHz
Normal operating mode (NORMAL OPE)	Operation at up to 32 MHz is allowed. Furthermore, low power consumption is achieved by selection from the following three modes according to the operating frequency. • High-Speed mode: Maximum operating frequency of 32 MHz. This mode is enabled after a reset release. • Low-Speed mode: Maximum operating frequency of 2 MHz. • Subosc-Speed mode: Maximum operating frequency of 32.768 kHz	Operation at up to 32 MHz is allowed. Furthermore, low power consumption is achieved by selection from the following two modes according to the operating frequency. • High-Speed mode: Maximum operating frequency of 32 MHz. This mode is enabled after a reset release. • Low-Speed mode: Maximum operating frequency of 2 MHz. In all power supply mode (ALLPWON) Low-Speed mode is not available.
Boost operating mode (BOOST OPE)	Operation at up to 64 MHz is allowed. This mode is the most suitable for high-speed processing. This mode can only be entered from High-Speed mode in all power supply mode (ALLPWON).	Operation at up to 64 MHz is allowed. This mode is the most suitable for high-speed processing. This mode can only be entered from High-Speed mode or VBB mode in all power supply mode (ALLPWON).
Low leakage current operating mode (VBB OPE)	When the chip is operating at a frequency no higher than 32.768 kHz, the leakage current can be reduced by back bias voltage control (VBBC), and the chip consumes less power in operation than in subosc-speed mode. This mode can only be entered from subosc-speed mode.	When the MCU is operating at a frequency no higher than 32.768 kHz, the leakage current can be reduced by back bias voltage control (VBBC), and the MCU consumes less power in operation. This mode can be entered from high-speed mode or low-speed mode.

Item		1500KB Product	256KB Product
Interrupt	Software standby mode	Non-maskable interrupt, port, LVD, EHC, AGT0, AGT1, IWDT, RTC, ACMP, USB, KINT, CCC	Non-maskable interrupt, port, LVD, EHC, AGT0, AGT1, AGTW0, AGTW1, WUPT, IWDT, RTC, KINT, CCC
	Snooze mode	Non-maskable interrupt, port, LVD, EHC, AGT0, AGT1, IWDT, RTC, ACMP, USB, KINT, CCC, ICU	Non-maskable interrupt, port, LVD, EHC, AGT0, AGT1, AGTW0, AGTW1, WUPT, IWDT, RTC, KINT, CCC, ICU
	Deep software standby mode	Non-maskable interrupt, PORT_IRQ0_DS to PORT_IRQ3_DS, LVD, CCC	Non-maskable interrupt, PORT_IRQ0_DS to PORT_IRQ3_DS, LVD, WUPT, RTC, CCC
Canceling Software Standby Mode		The route to transition to software standby has changed significantly. For 256KB products, a path has been added that enables transition/return from normal mode, Boost mode to VBB mode software standby mode. As a result, 256KB products can significantly reduce the mode transition/recovery time.	
		• Cannot transition/return from Normal mode to software standby mode of VBB mode • Cannot transition/return from Boost mode to software standby mode	• Can transition/return from Normal mode to software standby mode of VBB mode • Can transition/return from Boost mode to software standby mode • Addition of transition time reduction function (However, standby current increases when using)
IOVCC1		I/O functions assigned to port 3, port 6, port 7, and P202 to P204	I/O functions assigned to Port 1, Port 3, Port 5, Port 6, Port 7, and P202 to P205
Setting Power Supply Mode (ALLPWON/EXFPWON/MINPWON)		—	To Switch from all power supply mode (ALLPWON) to minimum power supply mode (MINPWON) To Switch from minimum power supply mode (MINPWON) to all power supply mode (ALLPWON)
Setting Power Control Mode (BOOST/NORMAL/VBB)		To switch from normal mode (NORMAL) to boost mode (BOOST) 1. Set the HOCO frequency to 24 MHz or 32 MHz Stop the PLL. (HOCOMCR.HCFRQ[1:0] = 00b or 01b). 2. Set OPCCR.OPCM[1:0] = 00b, and SOPCCR.SOPCM = 0 (High-Speed mode)	To switch from boost mode (BOOST) to normal mode (NORMAL) 1. Set the HOCO frequency to 24 MHz or 32 MHz (HOCOMCR.HCFRQ[1:0] = 00b or 01b). Set the system clock to less than the maximum operating frequency in High-Speed mode. 2. Set OPCCR.OPCM[1:0] = 00b (High-Speed mode)
		—	To switch from low leakage current mode (VBB) to boost mode (BOOST) When switching from boost mode (BOOST) to low leakage current mode (VBB)

Item	1500KB Product	256KB Product
	To switch from normal mode (NORMAL) to low leakage current mode (VBB) —	To switch from normal mode (NORMAL) to low leakage current mode (VBB), the PWSTCR.PWST[2:0] bits cannot be modified. Confirm the following.
	[A] The mode transition is not from boost mode (BOOST) → normal mode (NORMAL) → low leakage current mode (VBB) —	[A] The mode transition is not from boost mode (BOOST) → normal mode (NORMAL) → low leakage current mode (VBB) 5. Change system clock to SOSC clock or LOCO clock
	[B] The mode transition is from boost mode (BOOST) → normal mode (NORMAL) → low leakage current mode (VBB) 2. Enter subosc-speed mode in normal mode (NORMAL).*2 Note 2. Low leakage current mode (VBB) cannot be entered from any mode other than subosc-speed mode. Note 3. Changing the setting of VBBCR.IVDIS is prohibited in modes other than subosc-speed mode.	[B] The mode transition is from boost mode (BOOST) → normal mode (NORMAL) → low leakage current mode (VBB) 6. Change system clock to SOSC clock or LOCO clock. 7. Stop oscillator other than system clock source. —
	To switch from low leakage current mode (VBB) to normal mode (NORMAL) Set SOPCCR.SOPCM = 1（Subosc-Speed mode)*1 Note 1: If the SOPCCR.SOPCM bit is set to any mode other than subosc-speed mode, transition to normal mode (NORMAL) is not possible.	To switch from low leakage current mode (VBB) to normal mode (NORMAL) —
Functions for Reducing Power	Setting High-Speed/Low-Speed/Subosc-Speed Mode in Normal Mode (NORMAL) (2) Switching from a lower to a higher power consumption mode	Setting High-Speed/Low-Speed Mode in Normal Mode (NORMAL)
Deep Software Standby Mode Transition to Deep Software Standby Mode	In deep software standby mode, the CPU, on-chip peripheral functions except for the CCC, and all oscillators except for the sub-clock oscillator are stopped. Power consumption is reduced because the internal power supply to these modules is stopped. The contents of all of the CPU registers and peripheral modules except for the CCC become undefined.	In this mode, the CPU, on-chip peripheral functions (except for CCC, RTC, and WUPT), and all oscillators (except for sub-clock oscillator) are stopped; furthermore, since the internal power supply to these modules is stopped, power consumption is reduced. The contents of all the CPU registers and peripheral modules (except for CCC, RTC, and WUPT) become undefined.

Item	1500KB Product	256KB Product
Usage Notes	Valid setting for the clock-related registers SOSCCR. SOSTP	Valid setting for the clock-related registers —
	Write access to registers in subosc-speed mode	—
	Write access to the FLWT.FLWT[2:0] bits	—
	MOCO, the main clock oscillator, and the PLL must be stopped before entering software standby mode.	The main clock oscillator must be stopped before entering Software Standby mode.
	—	Notes on mode transition

Table 2.9 Comparison of Power-Saving Function Registers

Register	Bit	1500KB Product	256KB Product
MSTPCRB	MSTPB11	USB module stop	—
MSTPCRC	MSTPC10	LED module stop	—
MSTPCRD	MSTPD4	LPG module stop	—
	MSTPD8	MTDV module stop	—
	MSTPD9	—	RTC module stop
	MSTPD10	—	IWDT module stop
	MSTPD11	—	WDT module stop
	MSTPD12	—	AGTW0 module stop
	MSTPD13	—	AGTW1 module stop
	MSTPD18	—	WUPT module stop
	MSTPD20	R12DA module stop	—
	MSTPD28	ACMP module stop	—
FSTPCR	FLFSTP	Flash memory function stop	Reserved
	DBGSTP	Reserved	Debug function stop

Register	Bit	1500KB Product	256KB Product
PWSTCR	PWST[2:0]	Power Supply State Select b2 b0 000 : Transition to one of the following modes • Switching High-Speed/ Low-Speed/Subosc-Speed in normal mode (NORMAL) • Software standby mode • Deep software standby mode 001 : Transition to all power supply mode (ALLPWON) 010 : Transition to minimum power supply mode (MINPWON) 011 : Transition to minimum power supply mode (MINPWON) 100 : Transition to normal mode (NORMAL) 101 : Transition to boost mode (BOOST) 110 : Transition to low leakage current mode (VBB) 111 : Setting prohibited	Power Supply State Select b2 b0 000 : Transition to one of the following modes • Switching High-Speed/ Low-Speed in normal mode (NORMAL) • Software standby mode • Deep software standby mode 001 : Transition to all power supply mode (ALLPWON) 010 : Transition to minimum power supply mode (MINPWON) 011 : Transition to minimum power supply mode (MINPWON) 100 : Transition to normal mode (NORMAL) 101 : Transition to boost mode (BOOST) 110 : Transition to low leakage current mode (VBB) 111 : Setting prohibited
	SSBYPWG	Reserved	Select voltage cut-off area in software standby mode
	SSBYVBB		Back bias voltage control selection in software standby mode
	SSBYACC		Fast transition / return select in software standby mode
SOPCCR	—	Sub-Operating Power Control Register	—
SBYCR	RETPM	Target Power Supply Mode Select for Transition from Software Standby Mode in Flash-excluded Power Supply Mode (EXFPWON)	Reserved These bits are read as 0. The write value should be 0.
	SSBYMP	Software Standby Mode Transition in Minimum Power Supply Mode	
RAMSDCR	RAMSD7 to RAMSD4	SRAM Cutoff in Software Standby Mode	Reserved These bits are read as 0. The write value should be 0.
SNZREQCR	SNZREQEN23	Enables the ACMP snooze request	Enables the AGTW0 compare match A snooze request
DPSBYCR	DPSBY	Associated with SBYCR.SSBY bit and SBYCR.SSBYMP bit	Associated with SBYCR.SSBY bit.

Register	Bit	1500KB Product	256KB Product
DPSIER1	DRTCIIE	Reserved	RTC cycle interrupt deep software standby release signal enable
	DRTCAIE		RTC alarm interrupt deep software standby release signal enable
	DCCCIE	CCC Periodic Interrupt Deep Software Standby Cancel Signal Enable	CCC Periodic Interrupt/WUPT Interrupt Deep Software Standby Cancel Signal Enable
DPSIFR1	DRTCIIF	Reserved	RTC Deep Software Standby Cancel Flag
	DRTCAIF		RTC Alarm Interrupt Deep Software Standby Cancel Flag
	DCCCIF	CCC Periodic Interrupt Deep Software Standby Cancel Flag	CCC Periodic Interrupt /WUPT Interrupt Deep Software Standby Cancel Flag
VOCR	AV1CTL	AVCC1 Supply Control	Reserved These bits are read as 1. The write value should be 1.
	IV2CTL	IOVCC2 Supply Control	
	IV3CTL	IOVCC3 Supply Control	
	UVCTL	USBVCC Supply Control	
	VPMCTL	MTDV Power Supply Control	
VBBCR	IVDIS	Regarding the procedure for mode transitions when the internal voltage is discharged, see section 12.5.2, (3), [B] The mode transition is from boost mode (BOOST) → normal mode (NORMAL) → low leakage current mode (VBB). The setting of this bit can only be changed in subosc-speed mode in normal mode (NORMAL). Do not change the setting in other modes. The setting of this bit must be 0 in high-speed and low-speed mode in boost mode (BOOST), low leakage current mode (VBB), and normal mode (NORMAL). When a mode other than subosc-speed mode in normal mode (NORMAL) is to be entered, be sure to clear this bit to 0 in subosc-speed mode before the mode transition.	Regarding the procedure for mode transitions when the internal voltage is discharged, see (5) When switching from normal mode (NORMAL) to low leakage current mode (VBB), [B] The mode transition is from boost mode (BOOST) → normal mode (NORMAL) → low leakage current mode (VBB). The setting of this bit can be changed only when the system clock source is changed to the sub-clock oscillator or LOCO in normal mode (NORMAL) and the clock other than the set clock is stopped. Do not change in other mode. In boost mode (BOOST), low leakage current mode (VBB), and normal mode (NORMAL), this bit must be set to 0 when using clock settings other than the above.

2.7 Energy Harvesting Controller

Table 2.10 summarizes a comparison of energy harvesting controller specifications; Table 2.11 compares the energy harvesting controller registers.

Table 2.10 Comparison of Energy Harvesting Controller Specifications

Item	1500KB Product	256KB Product
VBAT_EHC input pin	Pin for the supply of power from a secondary battery. Connect a 2.6-V or 3.0-V secondary battery or a super capacitor in energy harvesting mode.	Pin for the supply of power from a secondary battery. Connect a 2.4-V, 2.5-V, 2.6-V, 2.7-V, 2.8-V, 2.9-V, 3.0-V, or 3.1-V secondary battery or a super capacitor in energy harvesting startup mode.

Table 2.11 Comparison of Energy Harvesting Controller Registers

Register	Bit	1500KB Product	256KB Product
EHCCR0	VBATCTL[1:0] b9-8	00 : Do not charge the secondary battery connected to the VBAT_EHC pin 11 : Charge the secondary battery connected to the VBAT_EHC pin The other settings are prohibited.	
	VBATCTL b9	—	0 : Do not charge the secondary battery connected to the VBAT_EHC pin. 1 : Charge the secondary battery connected to the VBAT_EHC pin.

2.8 Register Write Protection

Table 2.12 summarizes a comparison of register write protection functions.

Table 2.12 Comparison of Register Write Protection Functions

Item	1500KB Product	256KB Product
PRC0 bit	• Registers related to the clock generation circuit: SCKDIVCR, SCKSCR, PLLCCR, PLLCR, MOSCCR, HOCOCR, HOCOMCR, MOCOCR, CKOCR, CKO32CR, OSTDCR, OSTDSR, MOSCWTCR, MOMCR, SOSCCR, SOMCR, LOCOCR	• Registers related to the clock generation circuit: SCKDIVCR, SCKSCR, MOSCCR, HOCOCR, HOCOMCR, MOCOCR, FLLCR, FLLCR2, CKOCR, CKO32CR, OSTDCR, OSTDSR, MOSCWTCR, MOMCR, SOSCCR, SOMCR, LOCOCR
PRC1 bit	• Registers related to the functions for reducing power consumption: SBYCR, RAMSDCR, SNZCR, SNZEDCR, SNZREQCR, OPCCR, SOPCCR, DPSBYCR, DPSIER0, DPSIER1, DPSIFR0, DPSIFR1, DPSIEGR0, DPSIEGR1, SYOCDCR, FSTPCR, EHCCR0, EHCCR1, VOCR, PWSTCR, VBBCR	• Registers related to the functions for reducing power consumption: SBYCR, RAMSDCR, SNZCR, SNZEDCR, SNZREQCR, OPCCR, DPSBYCR, DPSIER0, DPSIER1, DPSIFR0, DPSIFR1, DPSIEGR0, DPSIEGR1, SYOCDCR, FSTPCR, EHCCR0, EHCCR1, VOCR, PWSTCR, VBBCR
PRC3	• Registers related to the LVD: LVD1CR1, LVD1SR, LVDBATCR1, LVDBATSR, LVCMPCR, LVDLVLR, LVD1CR0, LVDBATCR0	• Registers related to the LVD: LVD1CR1, LVD1SR, LVDBATCR1, LVDBATSR, LVCMPCR, LVDLVLR, LVD1CR0, LVDBATCR0

2.9 Interrupt Controller Unit

Table 2.13 compares the interrupt controller unit registers.

Table 2.13 Comparison of Interrupt Controller Unit Registers

Register	Bit	1500KB Product	256KB Product
IELSRn.IELS[4:0]	00111	(IELSR3 / 11 / 19 / 27) AMP_CMPI	(IELSR3 / 11 / 19 / 27) AGTW0_AGTCMAI
	01011	(IELSR0 / 8 / 16 / 24) CCC_PRD	(IELSR0 / 8 / 16 / 24) CCC_PRD WUPT_OVI
	01100	(IELSR3 / 11 / 19 / 27) MTDV_PM1INT (IELSR7 / 15 / 23 / 31) MTDV_PM1INT	(IELSR3 / 11 / 19 / 27) Setting prohibited (IELSR7 / 15 / 23 / 31) Setting prohibited
	10010	(IELSR2 / 10 / 18 / 26) USBFS_USBI	(IELSR2 / 10 / 18 / 26) AGTW1_AGTI
	10100	(IELSR1 / 9 / 17 / 25) USBFS_D1FIFO (IELSR3 / 11 / 19 / 27) USBFS_USBR	(IELSR1 / 9 / 17 / 25) AGTW0_AGTCMBI (IELSR3 / 11 / 19 / 27) AGTW1_AGTCMAI
	10101	(IELSR0 / 8 / 16 / 24) USBFS_D0FIFO (IELSR5 / 13 / 21 / 29) MTDV_PM36INT	(IELSR0 / 8 / 16 / 24) AGTW0_AGTI (IELSR5 / 13 / 21 / 29) Setting prohibited
	10110	(IELSR4 / 12 / 20 / 28) MTDV_PM25INT	(IELSR4 / 12 / 20 / 28) Setting prohibited
WUPEN	ACMP0WUPEN AGTW0CAWUPEN	ACMP_CMPI Interrupt Software Standby Returns Enable	AGTW0_AGTCMAI Interrupt Software Standby Returns Enable
	USBFSWUPEN AGTW1CAWUPEN	USBFS Interrupt Software Standby Returns Enable	AGTW1_AGTCMAI Interrupt Software Standby Returns Enable

2.10 Buses

Table 2.14 is a summary comparison of bus specifications.

Table 2.14 Comparison of Bus Specifications

Bus Type		1500KB Product	256KB Product
Bus Slaves	Internal peripheral bus 3	• Connected to peripheral modules (I/O Ports, ELC, SCI2 to SCI5, SCI9, POE, RTC, WDT, IWDT, CAC, TMR, RIIC, DOC, GPT, S14AD, TEMPS, R12DA)	• Connected to peripheral modules (I/O Ports, ELC, SCI2 to SCI5, SCI9, POE, RTC, WDT, IWDT, CAC, TMR, WUPT, RIIC, DOC, GPT, S14AD, TEMPS)
	Internal peripheral bus 5	• Connected to peripheral modules (KINT, CCC, AGT, LST, DIL, LPG, DIV, MTDV, ACMP, LED, VREF, USB)	• Connected to peripheral modules (KINT, CCC, AGT, AGTW, LST, DIL, DIV, VREF)

2.11 Event Link Controller

Table 2.15 compares the event link controller registers.

Table 2.15 Comparison of Event Link Controller Registers

Register	Bit	1500KB Product	256KB Product
ELSRn	ELS[10h]	Snooze entry This event cannot be selected in the ELSR0 to ELSR3 registers.	Snooze entry This event cannot be selected in the ELSR0 to ELSR3, ELSR6, and ELSR7 registers.
	ELS[14h]	—	AGTW0 interrupt
	ELS[15h]	—	AGTW0 compare match A
	ELS[16h]	—	AGTW0 compare match B
	ELS[28h]	—	WUPT overflow
	ELS[37h]	—	AGTW1 interrupt
	ELS[38h]	—	AGTW1 compare match A
	ELS[39h]	—	AGTW1 compare match B
	ELS[67h]	MTDV PM1 interrupt	—
	ELS[68h]	MTDV PM25 interrupt	—
	ELS[69h]	MTDV PM36 interrupt	—
ELSR6	—	—	TMR0 event link setting register
ELSR7	—	—	TMR1 event link setting register
ELSR12	—	R12DA event link setting register	—
ELOPA	—	—	Event Link Option Setting Register A

2.12 I/O Ports

Table 2.16 summarizes a comparison of I/O port specifications; Table 2.17 compares the I/O port registers.

Table 2.16 Overview of I/O Port Specifications

Port Symbol	1500KB Product	256KB Product
PORT0	P000 to P015	P000 to P007, P010 to P015
PORT1	P100 to P113	P100 to P113
PORT2	P200 to P205, P207	P200 to P205, P207 to P210
PORT3	P300 to P302, P314, P315	P300 to P302, P314, P315
PORT4	P404 to P413	P409 to P413
PORT5	P500, P508 to P511	P500, P501, P508 to P511
PORT6	P600 to P604	P600 to P604
PORT7	P700 to P704	P700 to P704
PORT8	P806 to P810	P806 to P815

Table 2.17 Comparison of I/O Port Registers

Register	Bit	1500KB Product	256KB Product
INLATCH	—	Input Latch Control Register	—
INLATCHRSTLV	—	Input Latch Level Reset Control Register	—
INLATCHRSTPL	—	Input Latch Pulse Reset Control Register	—

2.13 Multi-Function Pin Controller

Table 2.18 compares the multi-function pin controller registers.

Table 2.18 Comparison of Multi-Function Pin Controller Registers

Register	Bit	1500KB Product	256KB Product
PmnPFS	PDCR	Pull-Down Control	Reserved This bit is read as 0. The write value should be 0.
	PCODR	P-Channel Open-Drain Control	Reserved This bit is read as 0. The write value should be 0.
	DSCR[1:0] (b11-10)	Port Drive Capability 0 0: Low driving ability 0 1: Middle driving ability 1 0: Standard driving ability 1 1: High driving ability	—
	DSCR (b10)	—	Port Drive Capability 0: Standard drive 1: High drive
	(b11)	—	Reserved This bit is read as 0. The write value should be 0.

2.14 Port Output Enable

Table 2.19 summarizes a comparison of port output enable specifications; Table 2.20 compares the port output enable registers.

Table 2.19 Comparison of Port Output Enable Specifications

Item	1500KB Product	256KB Product
Output-disable control through ACMP interrupt request detection	Available	Not available
Interrupt	• Interrupts can be generated by detecting the input level of external trigger input pins (GTETRGn (n = A, B) pins). • Interrupts can be generated when all GPT output pins are driven to an active level simultaneously. • Interrupts can be generated when an output-disable request is generated by a comparator.	• Interrupts can be generated by detecting the input level of external trigger input pins (GTETRGn (n = A, B) pins). • Interrupts can be generated when all GPT output pins are driven to an active level simultaneously.

Table 2.20 Comparison of Port Output Enable Registers

Register	Bit	1500KB Product	256KB Product
POEGGn	IOCF	Output-Disable Request from GPT or ACMP Detection Flag	Detection Flag for GPT Output-Disable Request
	CDRE0	Comparator Output-Disable Request Enable	Reserved

2.15 Realtime Clock

Table 2.21 summarizes a comparison of realtime clock specifications; Table 2.22 compares the realtime clock registers.

Table 2.21 Comparison of Realtime Clock Specifications

Item	1500KB Product	256KB Product
Count mode	Calendar count mode/binary count mode	Calendar count mode/binary count mode/32-kHz count mode
Clock and calendar functions	• Calendar count mode Year, month, date, day of week, hour, minute, second are counted, BCD display 12 hours/24 hours mode switching function 30 seconds adjustment function (a number less than 30 is rounded down to 00 seconds, and 30 seconds or more are rounded up to 1 minute) Automatic adjustment function for leap years • Binary count mode Seconds are counted in 32 bits, binary display. • Common to both modes Start/stop function The sub-second digit is displayed in binary units (1 Hz, 2 Hz, 4 Hz, 8 Hz, 16 Hz, 32 Hz, or 64 Hz) • Time error correction function Clock (1-Hz/64-Hz) output	• Calendar count mode Year, month, date, day of week, hour, minute, second are counted, BCD display 12 hours/24 hours mode switching function 30 seconds adjustment function (a number less than 30 is rounded down to 00 seconds, and 30 seconds or more are rounded up to 1 minute) Automatic adjustment function for leap years • Binary count mode Count seconds in 32 bits, binary display • 32-kHz count mode Count 32.768 kHz in 32 bits, binary display • Shared by three modes Start/stop function The sub-second digit is displayed in binary units (1 Hz, 2 Hz, 4 Hz, 8 Hz, 16 Hz, 32 Hz, or 64 Hz) • Clock error correction function (Not supported in 32-kHz count mode) Clock (1-Hz/64-Hz) output
Interrupts	• Alarm interrupt (RTC_ALM) As an alarm interrupt condition, selectable for comparison with the following: Calendar count mode: Year, month, date, hour, minute, or second can be selected Binary count mode: Each bit of the 32-bit binary counter • Carry interrupt (RTC_CUP) An interrupt is generated at either of the following conditions: - When a carry from the 64-Hz counter to the second counter is generated. - When the 64-Hz counter is changed and the R64CNT register is read at the same time. • Return from Software Standby mode can be performed by an alarm interrupt or periodic interrupt	• Alarm interrupt (RTC_ALM) As an alarm interrupt condition, selectable for comparison with the following: Calendar count mode: Year, month, date, hour, minute, or second can be selected Binary count mode: Each bit of the 32-bit binary counter 32-kHz count mode: Upper 30 bits of the 32-bit binary counter • Carry interrupt (RTC_CUP) An interrupt is generated at either of the following conditions: - When a carry from the 64-Hz counter to the second counter is generated. - When the 64-Hz counter is changed and the R64CNT register is read at the same time. (32 kHz count mode is for 64-Hz counter reading only) • Return from Software Standby mode or Deep Software Standby mode can be performed by an alarm interrupt or periodic interrupt

Table 2.22 Comparison of Realtime Clock Registers

Register	Bit	1500KB Product	256KB Product
RSECCNT /BCNT0	—	The value after a reset is undefined.	The value after a reset is 0.
RMINCNT /BCNT1	—	The value after a reset is undefined.	The value after a reset is 0.
RHRCNT /BCNT2	—	The value after a reset is undefined.	The value after a reset is 0.
RWKCNT /BCNT3	—	The value after a reset is undefined.	The value after a reset is 0.
RDAYCNT	b5-b0	The value after a reset is undefined.	The value after a reset is 0.
RMONCNT	b4-b0	The value after a reset is undefined.	The value after a reset is 0.
RYRCNT	b7-b0	The value after a reset is undefined.	The value after a reset is 0.
RSECAR /BCNT0AR	—	The value after a reset is undefined.	The value after a reset is 0.
RMINCAR /BCNT1AR	—	The value after a reset is undefined.	The value after a reset is 0.
RHRAR /BCNT2AR	—	The value after a reset is undefined.	The value after a reset is 0.
RWKAR /BCNT3AR	—	The value after a reset is undefined.	The value after a reset is 0.
RDAYAR / BCNT0AER	—	The value after a reset is undefined.	The value after a reset is 0.
RMONAR / BCNT1AER	—	The value after a reset is undefined.	The value after a reset is 0.
RYRAR /BCNT2AER	b7-b0	The value after a reset is undefined.	The value after a reset is 0.
RYRAREN /BCNT3AER	—	The value after a reset is undefined.	The value after a reset is 0.
RCR1	PES[3:0]	The value after a reset is undefined.	These bits can be cleared to 0 by a power-on reset, but cannot be cleared by any other reset.
	PIE		
	AIE		
RCR2	START	The value after a reset is undefined.	This bit can be cleared to 0 by a power-on reset, but cannot be cleared by any other reset.
	AADJE		The value after a reset is 0.
	AADJP		The value after a reset is 0.
	HR24		This bit can be cleared to 0 by a power-on reset, but cannot be cleared by any other reset.
	CNTMD		This bit can be cleared to 0 by a power-on reset, but cannot be cleared by any other reset.
RCR4	RCKSEL	Count Source Setting	Reserved
	RSKSTP	Reserved	SOSC clock supply setting
RADJ	b7-b0	The value after a reset is undefined.	The value after a reset is 0.

Register	Bit	1500KB Product	256KB Product
RCPE	RTCEN	RTC Time Capture Event Input Enable The value after a reset is undefined.	RTC Time Capture Event Input Enable This bit can be cleared to 0 by a power-on reset, but cannot be cleared by any other reset.
	b3-b1	Reserved bits	Reserved bits This bit can be cleared to 0 by a power-on reset, but cannot be cleared by any other reset.
RTCCRn (n = 0 to 2)	TCCT[1:0]	Time Capture Control The value after a reset is undefined.	Time Capture Control The value after a reset is 0.
	TCST	Time Capture Status The value after a reset is undefined.	Time Capture Status The value after a reset is 0.
	TCNF[1:0]	Time Capture Noise Filter Control The value after a reset is undefined.	Time Capture Noise Filter Control The value after a reset is 0.
	TCPSEL	Reserved	Time Capture Event Input Pin Select
	TCEN	RTC Time Capture Event Enable The value after a reset is undefined.	Time Capture Event Input Pin Enable The value after a reset is 0.
RSECCPn /BCNT0CPn (n = 0 to 2)	—	The value after a reset is undefined. After RTC software reset, the value becomes 0.	The value after a reset is 0.
RMINCPn /BCNT1CPn (n = 0 to 2)	—	The value after a reset is undefined. After RTC software reset, the value becomes 0.	The value after a reset is 0.
RHRCPn /BCNT2CPn (n = 0 to 2)	—	The value after a reset is After RTC software reset, the value becomes 0.	The value after a reset is 0.
RDAYCPn /BCNT3CPn (n = 0 to 2)	—	The value after a reset is undefined. After RTC software reset, the value becomes 0.	The value after a reset is 0.
RMONCPn (n = 0 to 2)	—	The value after a reset is undefined. After RTC software reset, the value becomes 0.	The value after a reset is 0.

2.16 Data Inversion/Conversion Circuit

Table 2.23 summarizes a comparison of data inversion/conversion circuit specifications; Table 2.24 compares the data inversion/conversion circuit register.

Table 2.23 Comparison of Data Inversion/Conversion Circuit Specifications

Parameter	1500KB Product	256KB Product
Data inversion	The bit inversion value of input data is output	—
Data conversion	—	• Data inversion • The bit inversion value of input data is output • AND, OR, and EXOR operations of two input data By combining with data inversion, NAND、NOR, and EXNOR operations possible • Conversion of data alignment per byte width (byte swap) • The MSB and LSB can be swapped. (Endian conversion)

Table 2.24 Comparison of Data Inversion/Conversion Circuit Registers

Register	Bit	1500KB Product	256KB Product
IDRn (n = 0 to 3)	—	Input Data Registers n	DIL Input Data Registers n
IDR1n (n = 0 to 3)	—	—	DIL Input Data Registers 1n
ODRn (n = 0 to 3)	—	Output Data Registers n	DIL Output Data Registers n
DILCR	—	—	DIL Control Register

2.17 MIP LCD Controller

Table 2.25 summarizes a comparison of MIP LCD controller specifications; Table 2.26 compares the MIP LCD controller registers.

Table 2.25 Comparison of MIP LCD Controller Specifications

Item	1500KB Product	256KB Product
Functions	• Block transfer rewriting in 16-bit × 16-bit units (setting of the number of horizontal and vertical blocks and scanning method enabled)	• Block transfer rewriting in 16-bit × 16-bit or 8-bit × 8-bit units (setting of the number of horizontal and vertical blocks and scanning method enabled)

Table 2.26 Comparison of MIP LCD Controller Registers

Register	Bit	1500KB Product	256KB Product
MLCDBKCR	BKSIZE	Reserved	Block Transfer Size
	BKHNUM[4:0] BKHNUM[5:0]	Horizontal Transfer Count Setting 01h to 10h : These bits specify the number of blocks in the horizontal direction (1 to 16 blocks) for transfer. The other settings are prohibited.	Horizontal Transfer Count Setting 01h to 20h : These bits specify the number of blocks in the horizontal direction (1 to 32 blocks) for transfer. The other settings are prohibited.
	BKVNUM[4:0] BKVNUM[5:0]	Vertical Transfer Count Setting 01h to 10h : These bits specify the number of blocks in the vertical direction (1 to 16 blocks) for transfer. The other settings are prohibited.	Vertical Transfer Count Setting 01h to 20h : These bits specify the number of blocks in the vertical direction (1 to 32 blocks) for transfer. The other settings are prohibited.
MLCDVCOMCTL	HWMSKEN	Reserved	HW VCOM Mask
	HWMSKF		HW Mask
	FMASK[7:0]		VCOM Hardware Mask Range Bits Before Data Transmission
	BMASK[7:0]		VCOM Hardware Mask Range Bits After Data Transmission

2.18 14-bit A/D Converter

Table 2.27 summarizes a comparison of 14-bit A/D converter specifications; Table 2.28 compares the 14-bit A/D converter registers.

Table 2.27 Comparison of 14-bit A/D Converter Specifications

Item	1500KB Product	256KB Product
Input channels	Up to 18 channels: AN000 to AN006 (high precision), and AN016, AN017, and AN020 to AN028 (standard precision)	Up to 12 channels: AN000 to AN007 (high precision), and AN016, AN017, AN020, and AN021 (standard precision)
Extended analog function	Temperature sensor output	Temperature sensor output, VSC_VCC pin voltage output
Data registers	• 18 registers for analog input	• 12 registers for analog input • One register for VSC_VCC pin voltage output

Table 2.27 Comparison of 14-bit A/D Converter Registers

Register	Bit	1500KB Product	256KB Product
ADDRy	—	—	A/D Data Register y
ADDBLDR	—	—	A/D Data Duplexing Register
ADTSDR	—	—	A/D Temperature Sensor Data Register
ADVSCDR	—	—	A/D VSC_VCC Pin Voltage Data Register
ADRD	—	—	A/D Self-Diagnosis Data Register
ADANSA0	ANSAn <1500KB product> (n = 0 to 6) <256KB product> (n = 0 to 7)	A/D Conversion Channels Select	A/D Conversion Channels Select
ADANSA1	ANSAn <1500KB product> (n = 16, 17, 20 to 28) <256KB product> (n = 16, 17, 20, 21, 31)	A/D Conversion Channels Select	A/D Conversion Channels Select Bit 15 (ANSA31) is associated with VSC_VCC pin voltage.
ADANSB0	ANSBn <1500KB product> (n = 0 to 6) <256KB product> (n = 0 to 7)	A/D Conversion Channels Select	A/D Conversion Channels Select

Register	Bit	1500KB Product	256KB Product
ADANSB1	ANSBn <1500KB product> (n = 16, 17, 20 to 28) <256KB product> (n = 16, 17, 20, 21, 31)	A/D Conversion Channels Select	A/D Conversion Channels Select Bit 15 (ANSB31) is associated with VSC_VCC pin voltage.
ADANSC0	ANSCn <1500KB product> (n = 0 to 6) <256KB product> (n = 0 to 7)	A/D Conversion Channels Select	A/D Conversion Channels Select
ADANSC1	ANSCn <1500KB product> (n = 16, 17, 20 to 28) <256KB product> (n = 16, 17, 20, 21, 31)	A/D Conversion Channels Select	A/D Conversion Channels Select Bit 15 (ANSC31) is associated with VSC_VCC pin voltage.
ADSCSn	SCSm[4:0]	(mth) Conversion Channel Setting m = 00 to 06, 16 to 17, 20 to 28 n = 0 to 6, 16 to 17, 20 to 28	(mth) Conversion Channel Setting m = 00 to 07, 16 to 17, 20 to 21 n = 0 to 7, 16 to 17, 20 to 21, 31
ADADS0	ADSn <1500KB product> (n = 0 to 6) <256KB product> (n = 0 to 7)	A/D-Converted Value Addition/Average Channel Select	A/D-Converted Value Addition/Average Channel Select
ADADS1	ADSn <1500KB product> (n = 16, 17, 20 to 28) <256KB product> (n = 16, 17, 20, 21, 31)	A/D-Converted Value Addition/Average Channel Select	A/D-Converted Value Addition/Average Channel Select Bit 15 (ADS31) is associated with VSC_VCC.
ADSSTRn <1500KB product> (n = 0 to 6, L, T) <256KB product> (n = 0 to 7, L, T)	—	A/D Sampling State Register n	A/D Sampling State Register n

Register	Bit	1500KB Product	256KB Product
ADCMPANSR0	CMPCHAn <1500KB product> (n = 0 to 6) <256KB product> (n = 0 to 7)	Compare Window A Channel Select	Compare Window A Channel Select
ADCMPANSR1	CMPCHAn <1500KB product> (n = 16, 17, 20 to 28) <256KB product> (n = 16, 17, 20, 21, 31)	Compare Window A Channel Select	Compare Window A Channel Select Bit 15 (CMPCHA31) is associated with VSC_VCC pin voltage.
ADCMPLR0	CMPLCHAn <1500KB product> (n = 0 to 6) <256KB product> (n = 0 to 7)	Compare Window A Comparison Condition Select	Compare Window A Comparison Condition Select
ADCMPLR1	CMPLCHAn <1500KB product> (n = 16, 17, 20 to 28) <256KB product> (n = 16, 17, 20, 21, 31)	Compare Window A Comparison Condition Select These bits set comparison conditions of the standard-precision analog input channels to which window A comparison conditions are applied.	Compare Window A Comparison Condition Select These bits set comparison conditions of the standard-precision analog input channels or VSC_VCC pin voltage to which window A comparison conditions are applied.
ADCMPSR0	CMPSTCHAn <1500KB product> (n = 0 to 6) <256KB product> (n = 0 to 7)	Compare Window A Flag	Compare Window A Flag
ADCMPSR1	CMPSTCHAn <1500KB product> (n = 16, 17, 20 to 28) <256KB product> (n = 16, 17, 20, 21, 31)	Compare Window A Flag When window A operation is enabled (ADCMPCR.CMPAE = 1), these bits indicate the comparison result of the standard-precision analog input channels to which window A comparison conditions are applied.	Compare Window A Flag When window A operation is enabled (ADCMPCR.CMPAE = 1), these bits indicate the comparison result of the standard-precision analog input channels or VSC_VCC pin voltage to which window A comparison conditions are applied.

Register	Bit	1500KB Product	256KB Product
ADCMPBNSR	CMPCHB[5:0]	These bits select channels to be compared with the compare Window B conditions. b5 b0 0 0 0 0 0 0 : AN000(high-precision) 0 0 0 0 0 1 : AN001(high-precision) 0 0 0 0 1 0 : AN002(high-precision) : 0 0 0 1 1 0 : AN006(high-precision) 0 0 0 1 1 1 : Setting prohibited 0 1 0 0 0 0 : AN016(standard-precision) 0 1 0 0 0 1 : AN017(standard-precision) 0 1 0 1 0 0 : AN020(standard-precision) 0 1 0 1 0 1 : AN021(standard-precision) : 0 1 1 0 1 0 : AN026(standard-precision) 0 1 1 0 1 1 : AN027(standard-precision) 0 1 1 1 0 0 : AN028(standard-precision) 0 1 1 1 1 1 : Setting prohibited 1 0 0 0 0 0 : Temperature sensor 1 1 1 1 1 1 : No selection Settings other than the above are prohibited.	These bits select channels to be compared with the compare Window B conditions. b5 b0 0 0 0 0 0 0 : AN000(high-precision) 0 0 0 0 0 1 : AN001(high-precision) 0 0 0 0 1 0 : AN002(high-precision) : 0 0 0 1 1 0 : AN006(high-precision) 0 0 0 1 1 1 : AN007(high-precision) 0 1 0 0 0 0 : AN016(standard-precision) 0 1 0 0 0 1 : AN017(standard-precision) 0 1 0 1 0 0 : AN020(standard-precision) 0 1 0 1 0 1 : AN021(standard-precision) : Setting prohibited 0 1 1 1 1 1 : VSC_VCC 1 0 0 0 0 0 : Temperature sensor 1 1 1 1 1 1 : No selection Settings other than the above are prohibited.
ADCMPBSR	CMPSTB	When window B operation is enabled (ADCMPCR.CMPBE = 1), this bit indicates the comparison result of the high-precision and standard-precision analog input channels, and temperature sensor output to which window B comparison conditions are applied.	When Window B operation is enabled (ADCMPCR.CMPBE = 1), this bit indicates the comparison result of the high- and standard-precision analog input channels, VSC_VCC pin voltage output, and temperature sensor output to which Window B comparison conditions are applied.

Register	Bit	1500KB Product	256KB Product
ADEDCRm <1500KB product> (m = 0,1, 4 to 7) <256KB product> (m = 0, 1, 4, 5)	EDANCn [1:0] <1500KB product> (n = 0 to 6, 16, 17, 20 to 28) <256KB product> (n = 0 to 7, 16, 17, 20, 21, 31)	Emulator Debug Function Control	Emulator Debug Function Control

2.19 RAM

Table 2.29 is a summary comparison of RAM specifications.

Table 2.29 Comparison of RAM Specifications

Parameter	1500KB Product	256KB Product
RAM capacity	256 Kbytes	128 Kbytes
RAM address	SRAM0: 2000 0000 to 2000 7FFFh SRAM1: 2000 8000 to 2003 FFFFh	SRAM0: 2000 0000 to 2000 7FFFh SRAM1: 2000_8000 to 2001_FFFFh

2.20 Flash Memory

Table 2.30 is a summary comparison of flash memory specifications.

Table 2.30 Comparison of Flash Memory Specifications

Item	1500KB Product	256KB Product
Memory capacity	Up to 1.5 Mbytes	Up to 256 Kbytes
On-board programming	• Programming in serial programming mode (SCI boot mode) • Programming in serial programming mode (USB boot mode)	• Programming in serial programming mode (SCI boot mode)
Code flash memory size	Read Address 0000 0000h ~ 0017 FFFFh P/E Address 0000 0000h ~ 0017 FFFFh Number of Blocks 0 ~ 383	Read Address 0000 0000h ~ 0003 FFFFh P/E Address 0000 0000h ~ 0003 FFFFh Number of Blocks 0 ~ 63

3. Comparison of Pin Functions

Below, the pin functions are compared, including power supply, clock, and system control pins. Items that are present only in one group appear in **blue**, and items that appear in both groups but are different appear in **red**. Items for which there is no difference in specifications appear in **black**.

3.1 100-pin LFQFP package

Table 3.1 compares pin functions of the 100-pin LFQFP package

Table 3.1 Comparison of Pin Functions of 100-Pin LFQFP Package

100-pin LFQFP	1500KB Product	256KB Product
1	P810/CACREF_B/AGTIO0_A/GTIOC2A_B/SCK3_B/SCL0	P812/AGTWEE1_B/TXD4_C/QSPCLK_A
2	VSS	P811/AGTWIO1_B/QIO0A
3	IOVCC0	P810/GTIOC3A_B/AGTIO1_B/QIO1_A/IRQ5_B
4	P809/AGTEE0_A/GTETRGA_B/GTIOC2B_B/TXD3_B/SDA0	P809/GTIOC3B_B/AGTEE1_B/QIO2_A/IRQ6_B
5	P808/AGTO0_A/GTETRGB_B/RXD3_B/IRQ2_B	P808/AGTO1_B/RXD3_B/QIO3_A/IRQ2_B
6	P807/AGTOA0_A/GTIOC1A_B/CTS3_B/SSLB3_C	P807/AGTOA1_A/CTS3_B/QSSL_A/IRQ6_A
7	P806/AGTOB0_A/GTIOC1B_B	P806/AGTOB1_B
8	VCLH	VCLH
9	XCOUT	XCOUT
10	XCIN	XCIN
11	VSS	VSS
12	XTAL/P413/GTETRGA_A/GTIOC0A_A/TXD3_A	XTAL/P413/GTIOC0A_A/TXD3_A
13	EXTAL/P412/GTETRGB_A/GTIOC0B_A/RXD3_A	EXTAL/P412/GTIOC0B_A/RXD3_A
14	IOVCC	VCC/IOVCC
15	VCL	VCL
16	SWCLK/CLKOUT32K_A/P411/TMCI0_A/TXD9_A/SCK3_A/IRQ0_A_DS	SWCLK/CLKOUT32K_A/P411/AGTWEE1_A/GTIOC0B_B/TXD9_A/SCK3_A/IRQ0_A_DS
17	P410/GTIOC3B_B/IRQ2_A_DS	P410/IRQ9_A
18	CLKOUT32K_B/P409/GTIOC3A_B/IRQ3_A_DS	CLKOUT32K_B/P409/IRQ9_B
19	EHMD	EHMD
20	VBN	VBN
21	VBP	VBP
22	SWDIO/P207/USB_ID_A/RXD9_A/CTS3_A/IRQ1_A_DS	SWDIO/P207/AGTWO1_A/GTIOC0A_B/RXD9_A/CTS3_A/IRQ1_A_DS
23	RES#	RES#
24	MD/P201/TMRI0_A	MD/P201
25	P200/TMO0_A/NMI	P200/NMI
26	VSS	VSS
27	VCC_SU	VCC_SU
28	VBAT_EHC	VBAT_EHC
29	VSC_VCC	VSC_VCC

100-pin LFQFP	1500KB Product	256KB Product
30	VSC_GND	VSC_GND
31	VSS_USB	BSCANP
32	USB_DM	P210/AGTWOA1_A
33	USB_DP	P209/AGTWOB1_A
34	VCC_USB	P208/AGTWIO1_A/TMWO
35	P205/CTS4_B/IRQ8_B	P205/AGTWO0_B/CTS4_B/IRQ8_C
36	P204/ADTRG0_A/GTIU_A/RTCIC0_B/USB_VBUS/SCK4_B/IRQ9_B	P204/ADTRG0_A/AGTO0_A/GTIU_A/TMCI0_A/RTCIC0_A/SCK4_B/IRQ7_B
37	P203/GTIV_A/RTCIC1_B/USB_OVRCURA_A/TXD4_B	P203/AGTOA0_A/GTIV_A/TMRI0_A/RTCIC1_A/RXD4_B
38	P202/CACREF_A/GTIW_A/CCCOUT_B/RTCOUT_B/USB_OVRCURB_A/RXD4_B/IRQ4_A	P202/CACREF_A/AGTOB0_A/GTIW_A/TMO0_A/CCCOUT_A/RTCOUT_A/TXD4_B/IRQ4_A
39	P704/TMCI1/CTS0_C	P704/AGTWOA0_B/CTS0_C
40	P703/TXD0_C	P703/AGTWOB0_B/TXD0_C
41	P702/RXD0_C	P702/AGTWEE0_B/RXD0_C
42	P701/TMRI1/RTCIC2_B/USB_VBUSEN_A/SCL1	P701/TMRI1/RTCIC2_A/SCL1
43	P700/TMO1/SCK0_C/SDA1	P700/TMO1/SCK0_C/SDA1
44	P315/GTIOC4A_B/TXD5_B	P315/AGTWIO0_B/GTIOC4A_B/TXD5_B
45	P314/GTIOC4B_B/RXD5_B	P314/GTIOC4B_B/RXD5_B
46	IOVCC1	IOVCC1
47	VSS	VSS
48	P302/GTIU_B/TMCI0_B/CTS5_C/CTS5_B	P302/GTIU_B/GTIOC2A_B/TMCI0_B/CTS5_B
49	P301/GTIV_B/TMRI0_B/CCCOUT_A/RTCOUT_A/SCK5_C/SCK5_B	P301/GTIV_B/GTIOC2B_B/TMRI0_B/CCCOUT_B/RTCOUT_B/SCK5_B
50	P300/GTIW_B/TMO0_B	P300/GTIW_B/TMO0_B
51	P604/GTIOC5B_B/RTCIC0_A/TXD9_B/SSLB3_B/IRQ5_B	P604/GTOWLO_B/GTIOC5B_B/RTCIC0_B/TXD9_B/IRQ3_C
52	P603/GTIOC5A_B/RTCIC1_A/RXD9_B/SSLB0_D	P603/GTETRGB_B/GTIOC5A_B/RTCIC1_B/RXD9_B
53	P602/GTOUUP_B/RTCIC2_A/SCK9_B/QSPCLK_A	P602/GTOUUP_B/RTCIC2_B/SCK9_B
54	P601/GTOULO_B/CTS9_B/QSSL_A	P601/GTOULO_B/CTS9_B
55	P600/LPGOUT/SCK9_C	P600/GTETRGA_B
56	P113/AGTEE1_A/GTOWUP_A/GTIOC3A_A/TXD4_A/SSLB2_A/QIO0_B/IRQ5_A	P113/AGTEE0_A/GTOWUP_A/TMCI1/TXD4_A/SSLB2_A/QIO0_B/MLCD_VCOM/IRQ3_A_DS
57	P112/AGTEE0_B/GTOWLO_A/GTIOC3B_A/RXD4_A/SSLB3_A/QIO1_B/IRQ6_A	P112/AGTEE0_B/AGTWEE0_A/GTOWLO_A/RXD4_A/SSLB3_A/QIO1_B/MLCD_XRST/IRQ8_B
58	P111/AGTO0_B/GTOUUP_A/GTIOC2A_A/CTS4_A/RXD5_A/SSLB1_A/QIO2_B	P111/AGTO0_B/AGTWO0_A/GTOUUP_A/GTIOC2A_A/CTS4_A/RXD5_A/SSLB1_A/QIO2_B/MLCD_SCLK
59	P110/AGTOA0_B/GTOULO_A/GTIOC2B_A/SCK9_A/SCK5_A/MOSIB_A/QIO3_B	P110/AGTOA0_B/AGTWOA0_A/GTOULO_A/GTIOC2B_A/SCK9_A/SCK5_A/MOSIB_A/QIO3_B/MLCD_DEN
60	P109/AGTOB0_B/GTOVUP_A/CTS9_A/CTS5_A/MISOB_A/QSPCLK_B	P109/AGTOB0_B/AGTWOB0_A/GTOVUP_A/CTS9_A/CTS5_A/MISOB_A/QSPCLK_B/MLCD_ENBS

100-pin LFQFP	1500KB Product	256KB Product
61	P108/AGTIO0_B/GTOVLO_A/SCK4_A/TXD5_A/RSPCKB_A/QSSL_B	P108/AGTIO0_B/AGTWIO0_A/GTOVLO_A/SCK4_A/TXD5_A/RSPCKB_A/QSSL_B/MLCD_ENBG
62	IOVCC2	IOVCC1
63	VSS	VSS
64	TMS/P107/AGTOB1_A/GTIOC1A_A/CTS0_A/RSPCKA_A/IRQ7_A/KRM07_A	TMS/P107/AGTOB1_A/GTETRGA_A/GTIOC1A_A/CTS0_A/RSPCKA_A/MLCD_SI0/IRQ7_A/KRM07_A
65	TDO/P106/AGTOA1_A/GTIOC1B_A/TXD0_A/SSLB0_A/IRQ0_B/KRM06_A/VCOUT_A	TDO/P106/AGTOA1_A/GTETRGB_A/GTIOC1B_A/TXD0_A/SSLB0_A/MLCD_SI1/IRQ3_B/KRM06_A
66	TDI/P105/AGTO1_A/GTIOC4A_A/USB_EXICEN/RXD0_A/MISOA_A/IRQ8_A/KRM05_A	TDI/P105/AGTO1_A/GTIOC4A_A/RXD0_A/MISOA_A/MLCD_SI2/IRQ8_A/KRM05_A
67	TCK/P104/AGTIO1_A/GTIOC4B_A/SCK0_A/MOSIA_A/IRQ9_A/KRM04_A	TCK/P104/AGTIO1_A/GTIOC4B_A/SCK0_A/MOSIA_A/MLCD_SI3/IRQ4_B/KRM04_A
68	P103/GTIOC5A_A/CTS2_A/CTS1_A/SSLA0_A/KRM03_A	P103/AGTEE1_A/GTIOC5A_A/CTS2_A/CTS1_A/SSLA0_A/MLCD_SI4/KRM03_A
69	P102/GTIOC5B_A/TXD2_A/TXD1_A/IRTXD1_A/SSLA1_A/KRM02_A	P102/AGTIO0_A/GTIOC5B_A/TXD2_A/TXD1_A/IRTXD1_A/SSLA1_A/MLCD_SI5/KRM02_A
70	P101/GTIOC0A_B/RXD2_A/RXD1_A/IRRXD1_A/SSLA2_A/KRM01_A	P101/AGTRG0_B/GTIOC0A_C/RXD2_A/RXD1_A/IRRXD1_A/SSLA2_A/MLCD_SI6/KRM01_A
71	P100/GTIOC0B_B/SCK2_A/SCK1_A/SSLA3_A/KRM00_A	P100/CACREF_B/GTIOC0B_C/SCK2_A/SCK1_A/SSLA3_A/MLCD_SI7/KRM00_A
72	P511/GTOVUP_B/GTIOC1B_C/KRM03_B	P511/GTOVUP_B/GTIOC1B_B/SCK0_B/KRM03_B
73	P510/GTOVLO_B/GTIOC1A_C/KRM02_B	P510/GTOVLO_B/GTIOC1A_B/RXD0_B/KRM02_B/AN021
74	P509/USB_OVRCURB_B/KRM01_B	P509/TXD0_B/KRM01_B/AN020
75	P508/GTIOC2B_C/IRQ4_B	P508/IRQ4_C/AN017
76	P500/ADTRG0_B/AGTOB1_B/GTOWUP_B/GTIOC4B_C/CTS0_B/MISOA_B/QIO0_A/AN022	P501/AN016
77	IOVCC3	P500/GTOWUP_B/GTIOC1A_B/CTS0_B
78	VSS	AVCC0
79	P015/AGTIO1_B/GTOWLO_B/GTIOC4A_C/SCK0_B/SSLA3_B/QIO1_A/IRQ7_B/AN022	AVSS0
80	P014/AGTEE1_B/GTIOC3B_C/RXD0_B/SSLA2_B/QIO2_A/IRQ6_B/AN021	P007/AN007
81	P013/AGTO1_B/GTIOC3A_C/TXD0_B/SSLA1_B/QIO3_A	P006/AN006
82	P012/SSLA0_B	P005/AN005
83	CLKOUT/P011/RSPCKA_B/AN017	VREFL0
84	P010/MOSIA_B/AN016	VREFH0/AVTRO
85	AVCC1	P004/AN004
86	P009/CMPREF	P003/AN003
87	P008/CMPIN	P002/AN002
88	P007/DA0	P001/AN001
89	AVSS1	P000/AN000
90	P006/AN006	VSS

100-pin LFQFP	1500KB Product	256KB Product
91	P005/AN005	IOVCC0
92	P004/AN004	CLKOUT/P015/GTIOC3A_A/SSLA1_B/IRQ5_A
93	P003/AN003	P014/GTIOC3B_A/SSLA0_B/IRQ2_A_DS
94	P002/AN002	P013/SCK3_B/SCL0
95	VREFL0	P012/TXD3_B/SDA0
96	P001/AN001	P011/RSPCKA_B
97	P000/AN000	P010/MOSIA_B
98	VREFH0/AVTRO	P815/AGTWOB1_B/CTS4_C/MISOA_B
99	AVCC0	P814/AGTWOA1_B/SCK4_C/SSLA2_B
100	AVSS0	P813/AGTWO1_B/RXD4_C/SSLA3_B

4. Usage Notes

4.1 Notes on Pin Design

4.1.1 Power Supply Pins

For 256KB products, a voltage should be applied to the VCC/IOVCC pin before the IOVCCn pins.

The capacitance values of the smoothing capacitors connected to the VBN and VBP pins of are different between the 1500KB and 256KB products. For 1500KB products the capacitance is 1.0 µF, and for 256KB products a 0.56 µF smoothing capacitor should be connected.

4.1.2 General I/O Ports

Depending on the input/output port, there are differences in the number of I/O pins and the number of bits for 1500KB and 256KB products. For details, please refer to the 256KB Product User's Manual: Hardware appearing in "5. Reference Documents".

When the P201/MD pin is not used, processing is different for 1500KB and 256KB products. In 1500KB products, the pin is connected to VCC via a resistor "pull-up" or is "used as a mode pin". For 256KB products, the pin should be "used as a mode pin".

4.2 Notes on Function Settings

4.2.1 Power saving functions

There are places in 1500KB and in 256KB products where settings are different when switching power supply modes, power control modes, and low-power consumption modes. For details, refer to their user's manuals.

As a common limitation for both products , when transitioning from a mode other than all power supply mode (ALLPWON) to all power supply mode (ALLPWON), it is necessary to set ICLK≦4 MHz before executing the WFI command. When transitioning from the all-power mode (ALLPWON) to software standby mode (SSTBY), it is necessary to set ICLK≦4 MHz before executing the WFI command.

However, with 256KB products, you should also note the following:

In 256KB products, a path is added that allows direct transition from all power supply mode (ALLPWON) to power supply mode other than Flash (EXFPWON) and minimum power supply mode (MINPWON) software standby mode (SSTBY). In this case as well, the restriction of ICLK≦4 MHz must be observed.

4.2.2 Interrupt Controller Unit

There are fewer modules that may fail to catch interrupts during operation in other than software standby mode.

During operation in a mode other than software standby mode, there is the possibility that the following interrupts may not be caught, and so the PCLKB frequency should be set to 32 kHz or higher.

<1500KB products>

— CCC/RTC/WDT/IWDT/AGT

<256KB products>

— WDT/IWDT

There are several changes related to interrupts during module-stop state.

<1500KB products>

— CCC, RYC, and AGT does not stop counting even if the module is stopped (MSTP = 1). Therefore, the interrupt occurs even if the peripheral is in module-stop state.

<256KB products>

— CCC, RYC, WUPT, AGT, and AGTW does not stop counting even if the module is stopped (MSTP = 1). However, the interrupt circuit is stopped. Therefore, the interrupt will occur only once, and no subsequent interrupts will occur.

4.2.3 Event Link Controller

The number of registers that cannot be selected in a snooze entry event has increased.

<1500KB products>

— This event cannot be selected in the ELSR0 to ELSR3 registers.

<256KB products>

— This event cannot be selected in the ELSR0 to ELSR3 and ELSR7 registers.

For 256KB product, do not set the same peripheral module as the event source and destination from/to ELC.

4.2.4 Memory Protection Unit

In 1500KB products, when protecting the registers within DMAC/DTC, a setting should be used for the entire DMAC/DTC register region (4000 5000h to 4000 5FFFh).

4.2.5 Realtime Clock

In 1500KB products, a value written to the RCR4 register is reflected beginning with the fourth time the register is read after writing.

In 256KB products, in order to capture a value upon a time capture event input, the time capture control bit (RTCCRn.TCCT bit) should be set during counting operation (RCR2.START bit=1). The time capture function cannot be used during LVD reset.

The initialization procedure when not using the RTC is different for 1500KB and for 256KB products. In 1500KB products, the registers in the RTC are not initialized by a reset. Depending on the initial state, the occurrence of unintended interrupt requests or counter operation may result in increased power consumption. For details of initialization procedures, please refer to the user's manual. In 256KB products, the registers in the RTC are initialized by a power-on reset and by an RTC software reset. However, the RCR1, RCR2, RCR4, and RCPE registers have bits that are initialized only upon a power-on reset.

4.2.6 Boundary scan

The pins that are not subject to boundary scans are different.

<1500KB products>

- Power supply pins (VCC, VCL, VCLH, VSS, AVCC0/1, AVSS0/1, VSC_VCC, VSC_GND, VCC_USB, VSS_USB, IOVCC0/1/2/3, VBAT_EHC, VCC_SU, VBN, VBP, VREFL0, VREFH0, VL1) cannot be boundary-scanned.
- USB-dedicated pins (USB_DP, USB_DM) cannot be boundary-scanned.
- Boundary scan pins (TCK, TMS, TDI, TDO) cannot be boundary-scanned.
- Mode pins (MD,EHMD, BSCANP) cannot be boundary-scanned.
- MTDV pins (MTDO1_DRV0 to MTDO2_DRV0, MTDO4_DRV1 to MTDO6_DRV1, MTDO7_DRV2 to MTDO9_DRV2, PM_RES_DRV0, VPM) cannot be boundary-scanned.

<256KB products>

- Power supply pins (VCC, VCL, VCLH, VSS, AVCC0, AVSS0, VSC_VCC, VSC_GND, IOVCC ,IOVCC0/1, VBAT_EHC, VCC_SU, VBN, VBP, VREFL0, VREFH0, VL1) cannot be boundary-scanned.
- Clock pins (EXTAL, XTAL, XCIN, XCOUT) cannot be boundary-scanned.
- Reset pin (RES#) cannot be boundary-scanned.
- Boundary scan pins (TCK, TMS, TDI, TDO) cannot be boundary-scanned.
- Mode pins (MD, EHMD, BSCANP) cannot be boundary-scanned.

4.2.7 14-bit A/D converter

The bit positions of reserved bits in the A/D emulator debug function control register m (ADEDCRm) are different.

<1500KB products>

- In the ADEDCR1 register, bits b13 and b12 are also reserved bits. In the ADEDCR4 register, bits b13, b12, b9, and b8 are also reserved bits. In the ADEDCR7 register, bits b13, b12, b9, b8, b5, and b4 are also reserved bits.

<256KB products>

- In the ADEDCR5 register, bits b13, b12, b9 and b8 are also reserved bits. In the ADEDCR7 register, bits b9, b8, b5, b4, b1 and b0 are also reserved bits.

4.2.8 Reference voltage generation circuit

The method for setting the reference voltage output control register (AVCR) is different.

<1500KB products>

- Settings of the LPMD bit and the STDMD bit are exclusive. When one of these is 1, the other must always be set to 0. The low-power consumption mode should be set when using the 14-bit A/D converter and with PCLKB set to 32 kHz.

<256KB products>

- Set the same value for the IBIASEN and VREFEN bits.
- Settings of the LPMD bit and the STDMD bit are exclusive. When one of these is 1, the other must always be set to 0. The low-power consumption mode should be set when using the 14-bit A/D converter and with PCLKB set to 32.768 kHz.

5. Reference Documents

User's Manual: Hardware

RE01 Group Products with 1.5-Mbyte Flash Memory User's Manual: Hardware Rev. 1.00 (R01UH0796EJ0100)

(The latest version can be downloaded from the Renesas Electronics website.)

RE01 Group Products with 256-KB Flash Memory User's Manual: Hardware Rev. 1.00 (R01UH0894EJ0100)

(The latest version can be downloaded from the Renesas Electronics website.)

Technical Update/Technical News

(The latest version can be downloaded from the Renesas Electronics website.)

Revision History

Rev.	Date	Description	
		Page	Summary
1.00	Jun.30.2020	-	First edition issued

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)

   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on

   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state

   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins

   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals

   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin

   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
7. Prohibition of access to reserved addresses

   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
8. Differences between products

   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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