For the RH850/F1KM-S1 series and the RH850/F1K series, it was found that the High Speed Internal Oscillator (HS IntOSC) does not meet the specification at a specific condition. In addition, for all products of the RH850/F1K, RH850/F1KM and the RH850/F1KH, it was found that the HS IntOSC does not meet the specification when the user trimming function is used.

This Technical Update reports this issue, workarounds and final handling.

1. **Contents of the defect**

   <1> The HS IntOSC frequency \( f_{RH} \) may not meet the specification range (8.00MHz ±0.4MHz), because its frequency may swing while writing and/or erasing the code/data flash. The impacts when the HS IntOSC frequency swings are shown below:
   
   - The operation timing of functions set to the HS IntOSC / EMCLK as the source clock, may shift from the intended timing\(^{\text{Note1}}\).
   - Since the Clock Monitor (CLMA\(^{x}\)) that monitors the PLL by the HS IntOSC may detect an unintended error and an error reset (CLMA\(^{x}\)RES\(^{\text{ Note2} }\)) may be generated.
   - Since the CLMA0 that monitors the HS IntOSC may detect an unintended error, a 'CLMA0RES' may be generated.
   - The operation timing of the Low-power sampler (LPS) including the stabilization time, may shift from the intended timing. The LPS at the analog input mode may not operate just as intended, since the stabilization time of the A/D converter (min. 1μs) may not be met.

   Note 1: This is also applicable when the HS IntOSC is set as PLL source clock.
   Note 2: \( x = 2 \) (RH850/F1K series)
   \( x = 3 \) (RH850/F1KM-S1 series)

   <2> The HS IntOSC frequency \( f_{RH} \) (Condition: After user trimming @ trimming temp) may not meet the specification range (8.00MHz ±0.08MHz), because its frequency may swing while writing and/or erasing the code/data flash.
2. Applicable products

<table>
<thead>
<tr>
<th>Products series</th>
<th>Defect &lt;1&gt;</th>
<th>Defect &lt;2&gt;</th>
</tr>
</thead>
<tbody>
<tr>
<td>RH850/F1K series</td>
<td>Applicable</td>
<td>Applicable</td>
</tr>
<tr>
<td>RH850/F1KM-S1 series</td>
<td>Applicable</td>
<td>Applicable</td>
</tr>
<tr>
<td>RH850/F1KM-S4 series</td>
<td>Not applicable</td>
<td>Applicable</td>
</tr>
<tr>
<td>RH850/F1KH-D8 series</td>
<td>Not applicable</td>
<td>Applicable</td>
</tr>
<tr>
<td>RH850/F1L, F1M, F1H series</td>
<td>Not applicable</td>
<td>No function</td>
</tr>
</tbody>
</table>

3. Judgment flow

For defect <1>

START

(A) No

(B) Yes

(C) No

Yes

No

Applicable

Not Applicable

(A) Are the HS IntOSC and EMCLK selected as the source clock during self-programing or User boot mode? Or is CLMAx<sup>x</sup> or LPS used during self-programing or User boot mode?

(B) Is the data flash written and/or erased during RUN mode?

(C) Are the HS IntOSC and EMCLK selected as the source clock during RUN mode? Or is CLMAx<sup>x</sup> or LPS used during RUN mode?

Note 3: x = 0, 2 (RH850/F1K series) x = 0, 3 (RH850/F1KM-S1 series)

For defect <2>

START

(D) No

(E) Yes

(F) No

Yes

No

Applicable

Not Applicable

(D) Is the user trimming function for the HS IntOSC used?

(E) Are the HS IntOSC or the EMCLK selected as the source clock during self-programing or User boot mode?

(F) Are the code/data flash written and/or erased during RUN mode?

(G) Are HS IntOSC and EMCLK selected as the source clock during RUN mode?
4. Workarounds

Please apply either (1) or (2) shown below. Further, if it is possible to apply neither please contact Renesas.

(1) In case of using the HS IntOSC while tolerating the swing frequency when writing and/or erasing the code/data flash:

Please apply (a), (b) and (c) shown below for defect <1> and apply (a) shown below for defect <2>.

(a) Please do not select the HS IntOSC and EMCLK as the source clock when writing and/or erasing the code/data flash\textsuperscript{Note4}.

(b) Please disable all CLMAX\textsuperscript{Note5} (CLMAXCTL0.CLMAXCLME=0\textsuperscript{Note5})

(c) Please disable the LPS (DPEN=0, ADEN=0) when writing and/or erasing the code/data flash.

Note 4: This is also applicable when the HS IntOSC is set as PLL source clock.

Note 5: x = 0, 2 (RH850/F1K series)

x = 0, 3 (RH850/F1KM-S1 series)

(2) To avoid that the frequency will swing when writing and/or erasing the code/data flash adjust the external circuit:

Please apply both (a) and (b) shown below for defect <1>.

(a) Please change the resistance component on the board shown at the following figure to 1.90-2.14Ω by adding 2Ω (tolerance ≤ ±5%).

(b) Please change the loopback inductance on the board shown at the following figure to 5-10nH.

5. Final Handling

Workarounds (1) and (2) shown at the above will be added to the User’s manual as cautions.