R-Car S4

User’s Manual: Hardware

- Preliminary -

arm

R-Car S4 Series (R8A779F4*) Products

For R-Car S4 Starter Kit

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(Rev.5.0-1  October 2020)
General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)
   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity.
   Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.

2. Processing at power-on
   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.

3. Input of signal during power-off state
   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements.
   Follow the guideline for input signal during power-off state as described in your product documentation.

4. Handling of unused pins
   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.

5. Clock signals
   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.

6. Voltage application waveform at input pin
   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between $V_{IL}$ (Max.) and $V_{IH}$ (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between $V_{IL}$ (Max.) and $V_{IH}$ (Min.).

7. Prohibition of access to reserved addresses
   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.

8. Differences between products
   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems.
   The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.
1. Overview

1.1 Introduction

The R-Car S4 is SoCs that feature the basic functions for next-generation car Gateway systems.

- Eight 1.2GHz Arm® Cortex®-A55 cores, 2 cores x 4 clusters.
  Configurations that can be selected for hardware lockstep (Option)
- 1.0 GHz Arm® Cortex®-R52 core
  Hardware Lock step is supported.
- Two 400MHz G4MH cores.
  Hardware Lock step is supported.
- Memory controller for LPDDR4X-3200 with 32 bit bus (16 bit x 1ch + 16 bit x 1ch) with ECC
- SD card host interface/eMMC
- UFS 3.0 x 1 channel
- PCI Express Gen4.0 interface, (Dual lane x 2 channels)
- ICUMX
- ICUMH
- SHIP-S x 3 channels
- AES Accelerator x 8 channels
- CAN FD interface x 16 channels
- R-Switch2 (Ether)
- 100base EtherAVB x 1 channel.
- Gbit-EtherTSN x 3 channels.
- 1 unit FlexRay (A,B 2 channels) interface,

Note: Arm and Cortex are registered trademark of Arm Limited. All other brands or product names are the property of their respective holders.

Remarks: For items noted as "option", please contact a Renesas Electronics sales representative.
### 1.1.1 R-Car S4 Series Lineup

<table>
<thead>
<tr>
<th>Package size (ball pitch) [mm]</th>
<th>23 x 23 (0.8)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Application system Core</td>
<td></td>
</tr>
<tr>
<td>Arm Cortex-A55</td>
<td>8x</td>
</tr>
<tr>
<td>CVM</td>
<td>5x</td>
</tr>
<tr>
<td>PCIe</td>
<td>2x 2 Lanes</td>
</tr>
<tr>
<td>UFS</td>
<td>1x</td>
</tr>
<tr>
<td>I2C</td>
<td>7x</td>
</tr>
<tr>
<td>FlexRay</td>
<td>1x</td>
</tr>
<tr>
<td>GPIO (always on area)</td>
<td>55x</td>
</tr>
<tr>
<td>Total GPIO</td>
<td>189x</td>
</tr>
<tr>
<td>JTAG</td>
<td>2x</td>
</tr>
</tbody>
</table>

*Access to the modules or channels that have been removed from the S4-8 product specifications is prohibited. If the user accesses these modules or channels, the correct operation of the LSI is not guaranteed.*
1.1.2 Target Architecture

APPLICATION PROPOSAL (EXAMPLE FOR FUTURE)
MID (30KDMIPS)
1.2  List of Specifications

1.2.1  G4MH Core

<table>
<thead>
<tr>
<th>Item</th>
<th>Description</th>
</tr>
</thead>
</table>
| System CPU       | • Dual Core G4MH 400MHz  
                   | Instruction cache 16 KB per core  
                   | CPU operating modes  
                   | - User mode, supervisor mode  
                   | Address space: 4-GB linear space for both data and instructions |

1.2.2  Arm-based Application system Core

<table>
<thead>
<tr>
<th>Item</th>
<th>Description</th>
</tr>
</thead>
</table>
| System CPU       | • Octa Core Arm Cortex-A55 (dual core per cluster) 1.2GHz  
                   | 2 core par cluster(4 cluster)  
                   | L1 : I/ 32 KB per core [w/ Parity]  
                   | D/32 KB per core [w/ ECC]  
                   | L2 : 0 B  
                   | L3 : 256 KB per cluster [w/ ECC] |

1.2.3  Arm-based Realtime Core

<table>
<thead>
<tr>
<th>Item</th>
<th>Description</th>
</tr>
</thead>
</table>
| Realtime Core    | • Arm Cortex-R52 1.0GHz  
                   | L1 I/D cache 32K/32 Kbytes (ECC)  
                   | ATCM/BTCM/CTCM (32K/32K/32Kbytes) (ECC)  
                   | Single CPU with Dual Lock-Step supported  
                   | Armv8-R architecture |
### 1.2.4 Debug and Trace

<table>
<thead>
<tr>
<th>Item</th>
<th>Description</th>
</tr>
</thead>
</table>
| Debug and Trace                   | JTAG interface  
  Supports dedicated 5-pin JTAG x 2, SWD, and LPD*1  
  The cross trigger function between following IPs.  
  Cortex-A55 CPU.  
  Cortex-R52 CPU.  
  **G4MH CPU**  
  ICUMX  
  ICUMH  
|                                   | Tracing function  
  10 Gbps or 5 Gbps HSSTP output bandwidth through PCIe*2  
  32-Kbyte embedded trace FIFO for Cortex-A55  
  32-Kbyte embedded trace FIFO for Cortex-R52  
  32-Kbyte embedded trace FIFO for CoreSight  
  32-Kbyte embedded trace FIFO for G4MH  
  System Trace Macrocell (ISP/MTI, AXI Masters)  
|                                   | Secure debug  
  Debugging is disabled if secure engine is used in Secure LCS*6 and it can be enabled with secure debugging authentication. |
# 1.2.5 CPU Core Peripherals

<table>
<thead>
<tr>
<th>Item</th>
<th>Description</th>
</tr>
</thead>
</table>
| Clock Pulse Generator (CPG) | - Generates the clocks from external clock (EXTAL).  
  - Maximum Cortex-A55 clock: 1200MHz  
  - Maximum Cortex-R52 clock: 1072MHz (or 1060MHz)  
  - Maximum G4MH clock 400MHz  
  - Maximum AXI-bus clock: 400 MHz  
  - Maximum SDRAM bus clock: 800MHz (LPDDR4X-3200)  
  - System-CPU shut down mode control supported  
  - Module-standby mode supported  
  - Includes module reset registers to control reset operation of individual on-chip peripheral modules |
| System Controller (SYSC) | - Shuts down and restores power to target modules.  
  Target modules:  
  - Cortex-A55 (with independent shutting down of each CPUs and SCU+L3 cache) (*)  
  (*): SCU and L3 cache are treated as one power-domain. When CPU is working, SCU+L3 cache can't be powered off.  
  - Low leakage standby mode supported. |
| RESET | - Includes 2 reset-signal external output port for external modules  
  - Includes Boot Address Register etc. |
| Pin function controller (PFC) | - Setting multiplexed pin functions for LSI pins  
  Function of the LSI pin selectable by setting the registers in the PFC module  
  - Module selection  
  Enable and disable the functions of LSI pins to which pin functions from multiple pin groups are assigned by setting the registers in the PFC module.  
  - Pull-up/down control for each LSI pin  
  On/off and up/down of the pull register on each LSI pin can be controlled by setting the registers in the PFC module. |
| General-purpose I/O (GPIO) | - General-purpose I/O ports  
  - Supports GPIO interrupts |
| Thermal sensor / Core Voltage Monitor (THS/CVM) | - 4 channels of thermal sensor (For Cortex-A55 core0, Cortex-A55 core4, G4MH core PE0 and Cortex-R52 core + around LPDDR IO)  
  - Programmable 3 temperature level for the sensor, to indicate the temperature level  
  - Interrupt to CPU/ECM when the temperature reaches programmed  
  - This module detects the lower or upper value of VDD’s voltage and notifies the state thereof  
  - Includes voltage monitoring module that measures the voltage supply inside the LSI |
## 1.2.6 External Bus Module

<table>
<thead>
<tr>
<th>Item</th>
<th>Description</th>
</tr>
</thead>
</table>
| External Flash Controller        | • Supports RPC (Reduced Pin Count) flash memory  
                                   |  
                                   | Maximum Frequency 160MHz (320MB/s) for Hyper Flash, Octal-SPI Flash                                                                 |
|                                  | Maximum Frequency 133MHz(133MB/s) for QSPI (QSPI0).                                                                                       |
|                                  | • Dual QSPI operation for two 4-bit serial flash memories is also available; 80MHz (160MB/s) for Dual QSPI (QSPI0+QSPI1).                |
|                                  | Note that Dual QSPI are operated in parallel interface and each 1xQSPI operation is not supported.                                      |
| External Bus Controller for LPDDR4X (DBSC4) | • 2 x 16-bit bus DRAM interfaces                                                                                                           |
|                                  | • 1 x channel 32-bit bus (16-bit bus + 16-bit bus) DRAM interface                                                                       |
|                                  | • LPDDR4X-3200 can be connected directly.                                                                                                 |
|                                  | • Memory Size: Up to 4GB (*)                                                                                                               |
|                                  | • Auto Refresh/Self Refresh/Partial Array Self Refresh supported                                                                         |
|                                  | • Auto Pre-charge Mode                                                                                                                   |
|                                  | • DDR Back Up supported                                                                                                                  |
|                                  | Cache memory for DDR-Memory access efficiency                                                                                             |
|                                  | (*)LPDDR4X-SDRAM compliant with JEDEC JESD209-4C and JEDEC JESD209-4-1A.                                                                  |
|                                  | (One LPDDR4X-SDRAM can be connected to one channel. two 16bit channels within a pair must have same sizes. Support memory with sizes from 2 Gbits to 16 Gbits per 16bit channel per rank.)The maximum memory space is 4GBytes per two 16bit channels. |
|                                  | R-Car S4 does not support LPDDR4X SDRAM Byte (x8) mode Addressing. 2 ranks/channel support.                                               |
### 1.2.7 Internal Bus Module

<table>
<thead>
<tr>
<th>Item</th>
<th>Description</th>
</tr>
</thead>
</table>
| AXI-bus | - On-chip main bus  
  - Bus protocol: AXI3 with QoS control  
  - Frequency: 266MHz/400MHz  
  - Bus width: 512 bits/256 bits/128 bits/64 bits/32bits |
| Direct Memory Access Controller for System (SYS-DMAC) | - 32channels for Application domain with Dual core lock step  
  - Address space: 1 TBytes on architecture  
  - Data transfer length: Byte, word (2 Bytes), longword (4 Bytes), 8 Bytes, 16 Bytes, 32 Bytes and 64 Bytes  
  - Maximum number of transfer times: 16,777,215 times  
  - Transfer request: Selectable from on-chip peripheral module request and auto request  
  - Bus mode: Selectable from normal mode and slow mode  
  - Priority: Selectable from fixed channel priority mode and round-robin mode  
  - Interrupt request: Supports interrupt request to CPU at the end of data transfer  
  - Repeat function: Automatically resets the transfer source, destination, and count at the end of DMA transfer (by descriptor function)  
  - Descriptor function (each channel) supported  
  - MMU (each channel) supported  
  - Channel bandwidth arbiter (each channel) |
| Boot | - System startup with selectable boot mode at power-on reset  
  - In on-chip ROM boot, QSPI serial ROM boot is supported.  
  - Program downloaded to internal memory  
  - Autorun function for the downloaded program  
  - Secure boot supported. Integrity check of boot image is proceeded before executing.  
  - On secure chip, boot operation is restricted to on-chip ROM boot mode. |
| Realtime Direct Memory Access Controller (RT-DMAC) | - 64 channels for Realtime domain with Dual core lock step  
  - Address space: 4 GBytes on architecture  
  - Data transfer length: Byte, word (2 Bytes), longword (4 Bytes), 8 Bytes, 16 Bytes, 32 Bytes and 64 Bytes  
  - Maximum number of transfer times: 16,777,215 times  
  - Transfer request: Selectable from on-chip peripheral module request and auto request  
  - Bus mode: Selectable from normal mode and slow mode  
  - Priority: Selectable from fixed channel priority mode and round-robin mode  
  - Interrupt request: Supports interrupt request to CPU at the end of data transfer  
  - Repeat function: Automatically resets the transfer source, destination, and count at the end of DMA transfer (by descriptor function)  
  - Descriptor function (each channel) supported  
  - MMU (each channel) supported  
  - Channel bandwidth arbiter (each channel) |
## 1. Overview

### sDMA(sDMAC for Control domain)
- 16 channels x 2 units for Control domain

### IPMMU
- An IPMMU is a memory management unit (MMU) which provides address translation and access protection functionalities to processing units and interconnect networks.

### Interrupt Controller (INTC)
- **(Application domain)**
  - 6 interrupt pins which can detect external interrupts
  - Max. 960 shared peripheral interrupts supported
  - Fall/rise/high level/low level detection is selectable
  - On-chip peripheral interrupts: Priority can be specified for each module
  - 16 software interrupts that have been generated and 6 private peripheral interrupts supported
  - 32-level priority selectable
  - Trust Zone supported

- **(Control domain)**
  - Interrupt sources
  - Non-Maskable interrupt (FENMI): 1 channel for each CPU.
  - FE level interrupt (FEINT): 1 channel for each CPU.
  - Low latency EI level interrupt (maskable) (EIINT0 to 31): 32 channels for each CPU.

### Multifunctional Interface (MFIS)
- Interrupt generation between Cortex-A55 core and Cortex-R52 core and G4MH core
- Fifteen external source bits for controlling 32-K types of interrupts
- Lock function for exclusive access supported

### Error Control Module (ECM)
- Error checking function control and arbitrate error signal from other module.

### 1.2.8 Internal Memory

<table>
<thead>
<tr>
<th>Item</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>RT-SRAM (application domain)</td>
<td>1M byte</td>
</tr>
<tr>
<td>RT-VRAM (application domain)</td>
<td>1M byte</td>
</tr>
<tr>
<td>System RAM (application domain)</td>
<td>384k byte</td>
</tr>
<tr>
<td>Code-SRAM (control domain)</td>
<td>6M byte</td>
</tr>
<tr>
<td>Data-SRAM (control domain)</td>
<td>256k byte</td>
</tr>
<tr>
<td>Cluster RAM (control domain)</td>
<td>512k byte x 2</td>
</tr>
<tr>
<td>LRAM (control domain)</td>
<td>64k byte x 2</td>
</tr>
<tr>
<td>Retention RAM (control domain)</td>
<td>128k byte</td>
</tr>
</tbody>
</table>

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**Note:**
- RT-Car Gen4
- R19UH0225EJ0050 Rev.0.50
- July 3, 2023
- Renesas
### 1.2.9 Storage

<table>
<thead>
<tr>
<th>Item</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>UFS 3.0</td>
<td>- 1-lane</td>
</tr>
<tr>
<td></td>
<td>- The UFS interface have to support a transfer speed of up to 1450 MB/s (11.6 Gbps) per lane (assume UFS rev. 3.0 Spec:1450MB/s(11.6Gbps) is wire rate).</td>
</tr>
<tr>
<td></td>
<td>- The UFS interface shall support a memory density (size) from 32 GB (256 Gb) up to 512 GB (4096 Gb).</td>
</tr>
<tr>
<td>Multi Media Card Interface (MMC)</td>
<td>- 1 channel</td>
</tr>
<tr>
<td></td>
<td>- eMMC 5.0 base, Support HS400 class transfer rate</td>
</tr>
<tr>
<td>SD Card Interface</td>
<td>- 1 channel</td>
</tr>
</tbody>
</table>
# 1.2.10 Network

<table>
<thead>
<tr>
<th>Item</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>CAN-FD</td>
<td>- 16 interfaces CANFD instance</td>
</tr>
<tr>
<td></td>
<td>- 8 Mbps</td>
</tr>
<tr>
<td>PCIe Controller</td>
<td>- PCI Express Base Specification Revision 4.0</td>
</tr>
<tr>
<td></td>
<td>- PHY integrated</td>
</tr>
<tr>
<td></td>
<td>- 2 Lanes x 2 channel</td>
</tr>
<tr>
<td>Ethernet Switch (EtherTS-IF)</td>
<td>- SGMII (LinkSpeed 1GHz; DataRatio 1Gbps, 100Mbps) / 5G USXGMII (LinkSpeed 5GHz; DataRatio 1Gbps, 2.5Gbps) interface</td>
</tr>
<tr>
<td></td>
<td>- Magic packet detection</td>
</tr>
<tr>
<td></td>
<td>- 3 channels</td>
</tr>
<tr>
<td>Ethernet AVB-IF</td>
<td>- Supports IEEE802.1BA, IEEE802.1AS, IEEE802.1Qav and IEEE1722 functions</td>
</tr>
<tr>
<td></td>
<td>- Supports transfer at 100 Mbps</td>
</tr>
<tr>
<td></td>
<td>- Magic packet detection</td>
</tr>
<tr>
<td></td>
<td>- MII/RMII interface</td>
</tr>
<tr>
<td></td>
<td>- 1 channel</td>
</tr>
<tr>
<td>FlexRay</td>
<td>- 2 channels (A,B interfaces)</td>
</tr>
<tr>
<td></td>
<td>- Comply with FlexRay protocol specification v2.1 Revision A</td>
</tr>
<tr>
<td></td>
<td>- Data transfer rate: up to 10 Mbit/s on each channel</td>
</tr>
</tbody>
</table>
### 1.2.11 Timer

<table>
<thead>
<tr>
<th>Item</th>
<th>Description</th>
</tr>
</thead>
</table>
| **RCLK Watchdog Timer** | - 1 channel  
- Internal 16-bit watchdog timer operated by RCLK  
- Programmable overflow time period: more than 1 hour count capable |
| **System Watchdog Timer (SWDT)** (For All Products) | - 1 channel  
- Internal 16-bit watchdog timer  
- Programmable overflow time period: more than 1 hour count capable  
- Initial counter value 171[s] |
| **Window WDT (WWDT)** | - 10 channels (8 channels for Cortex-A55, 2 channels for Cortex-CR52)  
- Window watchdog function, Window & 75% interrupt  
- Generates Reset or NMI on error detection  
- 3 start mode selectable. (Automatic, Intelligent automatic, software trigger.)  
- Configuration can be done by configuration terminals (flash/mask option or clamp) information |
| **Window WDT (WDTB)** | - 2 channels (WDTB for G4MH)  
- Selection of the operation mode after reset, by using the option bytes  
- WDTB trigger function  
- Interrupt request signal  
- Window function  
- WDTB error detection function |
| **Compare Match Timer Type0 (CMT0)** | - 2 channels  
- 32-bit timer (16 bits/32 bits can be selected)  
- Source clock: RCLK clock  
- Compare match function provided  
- Interrupt requests |
| **Compare Match Timer Type1 (CMT1)** | - 8 channels  
- 48-bit timer (16 bits/32 bits/48 bits can be selected)  
- Source clock: RCLK/system clock  
- Compare match function provided  
- Interrupt requests |
| **Compare match timer 2 (CMT2)** | (same as CMT1) |
| **Compare match timer 3 (CMT3)** | (same as CMT1) |
| **System Timer** | - 32-bit timer, 1 channel (16 bits/32 bits can be selected)  
- Compare match function provided  
- Interrupt requests |
| **System up-time clock** | - 1 channel  
- Internal 32-bit timer  
- Programmable overflow time period: maximum 24 hours |
## 1. Overview

<table>
<thead>
<tr>
<th>Item</th>
<th>Description</th>
</tr>
</thead>
</table>
| Timer Unit (TMU)            | • 15 channels  
• 32-bit timer  
• Auto-reload type 32-bit down counter  
• Internal prescaler  
• Interrupt request  
• 4 channels for input capture                                                                 |
| Timer Array Unit D (TAUD)   | • 2 units (32 channels)  
• 16 channels per 1 unit, 16-bit counter and 16-bit data register per channel                                                               |
| Timer Array Unit J (TAUJ)   | • 2 units (8 channels)  
• 4 channels per 1 unit, 32-bit counter and 32-bit data register per channel                                                                    |
| OS Timer (OSTM)             | • 8 units  
• 32-bit timer assuming the use of OS                                                                                                           |
| Real-Time Clock (RTCA)      | • 1 unit  
• Counters for years, months, day of the month, day of the week, hours, minutes, seconds, and asubcounter.                                                              |
| Secure Watchdog Timer (SWDT)| • 2 units (for ICU-MX, ICU-MH)  
• 1 channel Operation after release from the reset state can be set by using eFUSE  
• Internal 16-bit watchdog timer                                                                                                                     |
### 1.2.12 Peripheral Modules

<table>
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<tr>
<th>Item</th>
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</table>
| **Secure Engine** | - Supporting secure boot acceleration  
- Secure boot engine support RSA based authentication (key length up to 4096bit) |
| **ICUMX** | - The ICUMXB integrates an Intelligent Cryptographic Unit Processor (ICUP) that controls the ICUMXB sub-system and runs the user-defined security services.  
- The ICUMXB includes an accelerator that supports a block cipher algorithm based on the AES (Advanced Encryption Standard, FIPS PUB 197).  
- ICUMXB integrates several public key cryptographic algorithms like RSA, ECC.  
- ICUMXB integrates an accelerator that supports HASH function based on SHA-1, SHA-2 (Secure Hash Algorithm, FIPS PUB 180) and SHA-3 (Secure Hash Algorithm, FIPS PUB 202).  
- ICUMXB integrates a true random number generator. |
| **ICUMH** | - The ICUMHB integrates an Intelligent Cryptographic Unit Processor (ICUP) that controls the ICUMHB sub-system and runs the user-defined security services.  
- The ICUMHB includes an accelerator that supports a block cipher algorithm based on the AES (Advanced Encryption Standard, FIPS PUB 197).  
- ICUMHB integrates several public key cryptographic algorithms like RSA, ECC.  
- ICUMHB integrates an accelerator that supports HASH function based on SHA-1, SHA-2 (Secure Hash Algorithm, FIPS PUB 180) and SHA-3 (Secure Hash Algorithm, FIPS PUB 202).  
- ICUMHB integrates a true random number generator. |
| **AES accelerator** | - 8 channels  
- Accelerating AES encryption/decryption operation for high speed communication  
- Key length is 128 and 256 bits is supported.  
- Mode of operation supported ECB, CBC, CMAC, XTS, CTR, GCM  
- Key management function protects encryption keys from being exposed on memory or falsified by other functions |
| **SHIP-S** | - 3 channels  
- The SHIP-S includes an accelerator that supports a block cipher algorithm based on the AES (Advanced Encryption Standard, FIPS PUB 197).  
- The SHIP-S integrates several public key cryptographic algorithms like RSA, ECC.  
- The SHIP-S integrates an accelerator that supports HASH function based on SHA-1, SHA-2 (Secure Hash Algorithm, FIPS PUB 180) and SHA-3 (Secure Hash Algorithm, FIPS PUB 202).  
- The SHIP-S integrates an accelerator that supports a stream cipher algorithm ChaCha20 and authenticated encryption algorithm ChaCha20-Poly1305  
- The SHIP-S integrates a physical random number generator.  
- The SHIP-S has the key management function which protects encryption keys from being exposed on memory or falsified by other functions |
| **I2C Bus Interface (I2C)** | - 6 channels for open drain buffer  
- NXP I2C bus interface method supported  
- Master/slave functions  
- Multi-master functions  
- Fast mode compatible  
- Programmable clock generation from the system clock  
- Master and Slave function DMA supported |
## Overview

### I2C Bus Interface (RIIC)
- 1 channel
- I2C bus format
- Master mode or slave mode selectable
- Automatic securing of the various set-up times, hold times, and bus-free times for the transfer rate
- Transfer rate: Up to 400 kbps

### Multi-channel Serial Peripheral Interface (MSPI)
- 6 units incorporated
- Chip select: Up to 8 for each unit
- Three-wire serial synchronous data transfer
- Master mode or slave mode selectable
- Transmission rate up to 20 Mbps
- Arbitrary bit rate settable by the on-chip baud rate generator

### LIN/UART interface (RLIN3)
- 16 units incorporated
- Conforming to LIN Protocol Spec versions 1.3, 2.0, 2.1, 2.2, and SAE J2602
- Three operating modes
- LIN Master mode
- LIN Slave mode
- UART mode (half-duplex, full-duplex)
- Arbitrary bit rate is selectable by the on-chip baud rate generator
- LIN Self-test mode with internal data loop back

### Single Edge Nibble Transmission (RSENT)
- 8 units incorporated
- Conforming to the SENT (Single Edge Nibble Transmission) protocol specified in the SAE J2716_201604 standard and the SPC (Short PWM Code) extension to the SENT specification
- Unidirectional or bidirectional transfer is possible through a single pin
- Bidirectional transfer is possible through two pins
- Data transfer protected by a CRC is possible
1. Overview

<table>
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<tr>
<td>Serial communication interface with FIFO (SCIF)</td>
<td></td>
</tr>
</tbody>
</table>

- 4 channels
- Asynchronous, clock-synchronized modes
- Asynchronous serial communication mode

The SCIF performs serial data communication based on a character-by-character asynchronous system. This feature enables serial data communication with standard asynchronous communication chips that support Universal Asynchronous Receiver/Transmitter (UART) or Asynchronous Communication Interface Adapter (ACIA). There is a choice of eight serial data transfer formats.
- Data length: 7 bits or 8 bits
- Stop bits: 1 bit or 2 bits
- Parity: Even/odd/none
- Receive error detection: Parity, framing, and overrun errors
- Break detection:
  - A break is detected when a framing error lasts for more than 1 frame length at Space 0 (low level).
  - When a framing error occurs, a break can also be detected by reading the RX pin level directly from the serial port register (SCSPTR).

- Clock synchronous serial communication mode

The SCIF performs serial data communication synchronized with a clock. This feature enables serial data communication with other LSIs that support synchronous communication. There is a single serial data communication format for clock synchronous serial communication.
- Data length: 8 bits
- Receive error detection: Overrun errors

- Full-duplex communication capability

The SCIF has an independent transmitter and receiver that enable simultaneous transmission and reception. The transmitter and receiver both have a 16-stage FIFO buffer structure, enabling continuous serial data transmission and reception.

- On-chip baud rate generator, enabling any bit rate to be selected

The SCIF enables choice of a clock source for transmission/reception: a clock from the on-chip baud rate generator based on the internal clock or an external clock.

- Eight interrupt sources

The SCIF has eight types of interrupt sources. receive-data-ready, receive-FIFO-data-full, break, transmit-FIFO-data-empty, transmit-end, receive-error, overrun-error and time-out and enables any of them to be requested independently.
### 1. Overview

<table>
<thead>
<tr>
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</table>
| **Serial Communication Interface with FIFO (SCIF)** | • DMA data transfer  
When the transmit FIFO register is empty or the receive FIFO register has received data, issuing a DMA transfer request activates the DMA controller (DMAC) to execute a data transfer.  
• In asynchronous mode, modem control functions (RTS and CTS) are stored.  
• The amount of data in the transmit/receive FIFO registers and the number of receive errors in receive data in the receive FIFO register are available.  
• In asynchronous mode, a receive data ready (DR) or a timeout error (TO) can be detected during reception. |
| **Clock-Synchronized Serial Interface with FIFO (MSIOF)** | • 4 channels  
• MSIOF0/MSIOF1/MSIOF3  
  MSIOF_SCK clock cycle time (when master TX and master RX): 25ns (min)  
  MSIOF_SCK clock cycle time (when slave RX only): 16.666ns (min)  
  MSIOF_SCK clock cycle time (when slave RX and slave TX): 40ns (min)  
• MSIOF2  
  MSIOF_SCK clock cycle time (when master TX and master RX): 51ns (min)  
  MSIOF_SCK clock cycle time (when slave RX only): 45ns (min)  
  MSIOF_SCK clock cycle time (when slave RX and slave TX): 66ns (min)  
• Internal 32-bit x 64-stage transmit FIFOs/internal 32-bit x 256-stage receive FIFOs  
• Supports master and slave modes  
• Internal prescaler  
• Supports serial formats: IIS, SPI (master and slave modes)  
• Interrupt request, DMAC request |
| **High Speed Serial Communication Interface with FIFO (HSCIF)** | • 4 channels  
• Asynchronous serial communication mode  
• Capable of full-duplex communication  
• On-chip baud rate generator, enabling any bit rate to be selected  
• Eight interrupt sources  
• DMA data transfer  
• Modem control functions (HRTS# and HCTS#) are stored.  
• The amount of data in the transmit/receive FIFO registers and the number of receive errors in receive data in the receive FIFO register are available.  
• A receive data ready (DR) or a timeout error (TO) can be detected during reception. |
1.2.13 Special Edition Modules (Restricted)

<table>
<thead>
<tr>
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</tr>
</thead>
<tbody>
<tr>
<td>CRC</td>
<td>The cyclic redundancy check (CRC) block is a function block to generate and check CRC codes of input data via the APB bus. The 32-bit Ethernet polynomial (CRC-32-IEEE 802.3) is used as the generator polynomial. The CRC codes based on this generator polynomial are stored in the register.</td>
</tr>
<tr>
<td>Failure Self-Detection Output (RFSO)</td>
<td>This module distinguishes between permanent failure and temporary failure detected by CPU or other important circuit module; moreover, detects time-out error in the process of detecting failures. The failure of CPU or other important circuit will be detected by other circuit (Runtime Test). Also, this module will be used for managing FTTI of this LSI.</td>
</tr>
</tbody>
</table>