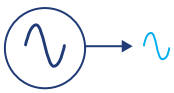
IDT Reference Clocks for Xilinx FPGAs

IDT's broad timing portfolio is well-suited for Xilinx FPGA and multiprocessor SoC applications. Featuring industry-leading high-performance PLL technology, IDT timing products address the stringent clock requirements of Xilinx programmable solutions, while wide design margins and flexible timing architectures help ease the clock tree design and implementation process.

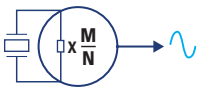
Xilinx Reference Clocks

Xilinx		IDT Clock Generator		IDT Jitter Attenuator Clock	IDT Crystal Oscillator		IDT Clock Buffer	IDT Synchronization Timing
Xilinx Technology Generation	Xilinx Product Family	VersaClock® 6E Programmable Clock 5P49V6965	Universal Frequency Translator (UFT™) 8T49N287	Universal Frequency Translator (UFT™) 8T49N241/2	Programmable XO 5P49V6975	Fixed Frequency XO XU/XL	8SLVD1204	82P33831
UltraSCALE+ 16nm	Zynq		●	●	●		●	●
	Virtex	●		●	●		●	●
	Kintex	●		●	●	●		●
UltraSCALE 20nm	Virtex	●		●	●		●	
	Kintex	●		●	●		●	
7 Series 28nm	Zynq-7000	●		●	●	●		
	Virtex-7	●		●	●	●		
	Kintex-7	●		●	●	●		
	Artix-7	●		●	●	●		
	Spartan-7	●		●	●	●		

Oscillators

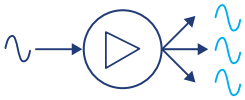


Clock Generators



Jitter Attenuators

Clock Distribution



Synchronous Timing

Xilinx System Timing Needs

Product Type	Function	Use Case Examples
Clock Generator	Generates multiple fixed-frequency clocks from a single device for FPGA systems	125MHz SATA clock, 26MHz USB3, 33.333MHz PS_REF_CLK, 125MHz system clock, 90MHz EMC clock, and 300MHz SYSCLK
Jitter Attenuator Clock	Removes jitter from an incoming recovered clock and drives a clean clock into the Xilinx transceiver	HDMI video systems require a clean and phase-aligned clock to drive the FPGA transceiver
Crystal Oscillator	Generates clocks that default to a certain frequency on power up but can also be easily reprogrammed	300MHz user clock, 156.25MHz user MGT (multi-gigabit transceiver) clock
Clock Buffer	Used to create multiple copies of reference clocks	Multiple GT (gigabit transceivers) running the same protocol require copies of the same clock source
Synchronization Timing	Supports timing synchronization over packet switched network applications	Synchronous Ethernet and IEEE 1588

To request samples, download documentation or learn more visit: **idt.com/timing**