R-Car Series, 3rd Generation


Introduction

This document gives guidelines on the points to take into account when designing power-supply circuits for SoC products with the use of the BD9571MWF-M power-supply IC from ROHM to implement standard control operations such as the sequences of turning the power on and off, booting up the CPU, and shutting down the system, as well as examples of circuits and their layouts.

Also, refer to "Designing Power-Supply Circuits for the R-Car H3, R-Car M3-W, R-Car M3-W+, and R-Car M3-N" on which this document is based. Contact ROHM Co., Ltd. regarding the detailed specifications of the BD9571MWF-M. We also recommend that the user at the same time refer to the SoC-related documents and the design guidelines for any other devices in use.

Target SoCs

- R-Car H3
- R-Car H3-N
- R-Car M3-W
- R-Car M3-W+
- R-Car M3-N

Target Power-Supply IC

- BD9571MWF-M

Reference Document

- Designing Power-Supply Circuits for the R-Car H3, R-Car M3-W, R-Car M3-W+, and R-Car M3-N

Note: Refer to the list of related documents at the end of this document for other related documents.
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1. Power-Supply Specifications

1.1 Features

- The system power supply described in this document consists of a primary power supply block (with 5 V being generated by a battery power supply), a secondary power supply block (generating secondary power-supply voltages from the 5-V input), and power supplies for peripheral circuits (additional options to suit the system configuration and needs).
- The BD9571MWF-M, which is a power-supply IC with multiple outputs, is used as the secondary power supply block.
- The BD9571MWF-M supplies all power-supply voltages to the SoCs and DRAM.
- The BD9571MWF-M controls the sequences of turning the power on and off.
- The BD9571MWF-M supports the DDR backup mode.
- The BD9571MWF-M supports AVS and DVFS control.
- The power supplies for peripheral circuits should be designed to suit the specifications of your system.

1.1.1 Block Diagram of a System Using an R-Car H3 (Example)

The following figure shows an example of a block diagram of a system in which the BD9571MWF-M is used to supply power to an R-Car H3 and DRAM. If peripheral circuits require power supplies that exceed the power-supply capacity of the BD9571MWF-M, add power supplies that suit the specifications of your system.

![Block Diagram of a System Using an R-Car H3 (Example)](image-url)
1.1.2  Block Diagram of a System Using an R-Car H3-N, R-Car M3-W, or R-Car M3-W+ (Example)

The following figure shows an example of a block diagram of a system in which the BD9571MWF is used to supply power to an R-Car H3-N, R-Car M3-W, or R-Car M3-W+, and DRAM.

![Block Diagram of a System Using an R-Car H3-N, R-Car M3-W, or R-Car M3-W+ (Example)](image)

Figure 1.1.2  Block Diagram of a System Using an R-Car H3-N, R-Car M3-W, or R-Car M3-W+ (Example)
1.1.3 Block Diagram of a System Using an R-Car M3-N (Example)

The following figure shows an example of a block diagram of a system in which the BD9571MWF-M is used to supply power to an R-Car M3-N and DRAM.

System 1 (producing the outputs on the DDR1C and DDR1) is not in use because the R-Car M3-N only has one DRAM channel.

![Block Diagram](image)

Figure 1.1.3  Block Diagram of a System Using an R-Car M3-N (Example)
1.2 Power Supply Profile

1.2.1 Power Supply Profile of the BD9571MWF-M

The specifications of the power-supply outputs of the BD9571MWF-M are listed below.

The power-supply outputs must meet the specifications of the SoC power supplies.

When choosing the DRAM, use devices to which the BD9571MWF-M can supply the required amount of current.

### Table 1.2.1 Specifications of BD9571MWF-M Power-Supply Outputs

<table>
<thead>
<tr>
<th>Objective</th>
<th>Voltage Range</th>
<th>Current Load Condition</th>
</tr>
</thead>
<tbody>
<tr>
<td>DVFS</td>
<td>Min.</td>
<td>Typ.</td>
</tr>
<tr>
<td>SoC (core)</td>
<td>0.805 V</td>
<td>0.830 V</td>
</tr>
<tr>
<td>VD09</td>
<td>0.795 V</td>
<td>0.820 V</td>
</tr>
<tr>
<td>VD18</td>
<td>1.755 V</td>
<td>1.800 V</td>
</tr>
<tr>
<td>SD0</td>
<td>3.215 V</td>
<td>3.300 V</td>
</tr>
<tr>
<td>SD1</td>
<td>1.755 V</td>
<td>1.800 V</td>
</tr>
<tr>
<td>SD2</td>
<td>3.215 V</td>
<td>3.300 V</td>
</tr>
<tr>
<td>SD3</td>
<td>1.755 V</td>
<td>1.800 V</td>
</tr>
<tr>
<td>VD25</td>
<td>2.455 V</td>
<td>2.500 V</td>
</tr>
<tr>
<td>DDR0</td>
<td>1.086 V</td>
<td>1.107 V</td>
</tr>
<tr>
<td>DDR1</td>
<td>1.325 V</td>
<td>1.350 V</td>
</tr>
<tr>
<td>DDR0C</td>
<td>1.755 V</td>
<td>1.800 V</td>
</tr>
<tr>
<td>DDR1C</td>
<td>1.755 V</td>
<td>1.800 V</td>
</tr>
<tr>
<td>V3P3</td>
<td>3.168 V</td>
<td>3.300 V</td>
</tr>
</tbody>
</table>

Notes:
1. The voltage values from DDR0 and DDR1 are examples. Values can be set by external resistors, to suit the specifications of the LPDDR4, DDR3L, or DDR3 device to be used. Note that DDR3L and DDR3 are only usable with the R-Car M3-N.
2. This value applies to the DC current. The instantaneous current should not exceed the overcurrent protection level specified in the specification of the BD9571MWF-M (OCP = 0.6 A (min.)).
1.3 Power-Supply-Related Sequences

Set the power-supply-related sequences to suit the SoC specifications (see "R-Car Series, 3rd Generation User’s Manual"). In the BD9571MWF-M, the initial settings of the internal ROM are programmed so that the power is turned on and off in sequences that match the specifications of the SoC. The sequences can also be changed by changing values in an external EEPROM. Contact ROHM Co., Ltd. with inquiries on using an EEPROM and changing the initial values.

1.3.1 Sequences of Turning the Power On and Off

At start-up, after the input power-supply voltage (V5AIN) is supplied, driving the RSTB pin to the high level begins the output of all power-supply voltages in the set sequence. At shut-off, driving the RSTB pin to the low level stops the output of all power-supply voltages in the set sequence.

<table>
<thead>
<tr>
<th>Power or Signal</th>
<th>Power-on Sequence</th>
<th>Power-off Sequence</th>
</tr>
</thead>
<tbody>
<tr>
<td>V5AIN</td>
<td></td>
<td></td>
</tr>
<tr>
<td>RSTB</td>
<td></td>
<td></td>
</tr>
<tr>
<td>V3P3</td>
<td></td>
<td></td>
</tr>
<tr>
<td>DDR0C, DDR1C</td>
<td></td>
<td></td>
</tr>
<tr>
<td>VD09</td>
<td></td>
<td></td>
</tr>
<tr>
<td>DVFS</td>
<td>Max. 3 ms</td>
<td></td>
</tr>
<tr>
<td>VD33</td>
<td>500 us</td>
<td></td>
</tr>
<tr>
<td>VLD25</td>
<td>500 us</td>
<td>10 ms</td>
</tr>
<tr>
<td>VD18</td>
<td>500 us</td>
<td>10 ms</td>
</tr>
<tr>
<td>DDR0, DDR1</td>
<td>500 us</td>
<td>10 ms</td>
</tr>
<tr>
<td>SD0 to SD3</td>
<td>500 us</td>
<td>10 ms</td>
</tr>
<tr>
<td>PRESETB</td>
<td>10 ms</td>
<td>500 us</td>
</tr>
</tbody>
</table>

Figure 1.3.1 Sequences of Turning the Power On and Off (with the BD9571MWF-M in its Initial State)
1.3.2 Sequences of DRAM Backup

In the DRAM backup mode, the output of the DRAM-related power-supply voltages (DDR0, DDR1, DDR0C, and DDR1C) continues when the other power supplies are turned off. When returning from the DRAM backup mode, only the power supplies other than the DRAM-related power supplies require turning on. The sequences are the same as those for normal power-off and power-on, except for the DRAM-related power supplies.

In the DRAM backup mode, the M*BKUP pins of the SoC are controlled by the BKUP_CTRL signal of the BD9571MWF-M, which satisfies the specifications of the SoCs.

<table>
<thead>
<tr>
<th>Power or Signal</th>
<th>Entry to DRAM Backup Mode</th>
<th>Exit from DRAM Backup Mode</th>
</tr>
</thead>
<tbody>
<tr>
<td>V5AIN</td>
<td></td>
<td></td>
</tr>
<tr>
<td>RSTB</td>
<td></td>
<td></td>
</tr>
<tr>
<td>V3P3</td>
<td></td>
<td></td>
</tr>
<tr>
<td>DDR0C, DDR1C</td>
<td></td>
<td></td>
</tr>
<tr>
<td>VD09</td>
<td></td>
<td></td>
</tr>
<tr>
<td>DVFS</td>
<td></td>
<td></td>
</tr>
<tr>
<td>VD33</td>
<td></td>
<td></td>
</tr>
<tr>
<td>VLD25</td>
<td></td>
<td></td>
</tr>
<tr>
<td>VD18</td>
<td></td>
<td></td>
</tr>
<tr>
<td>DDR0, DDR1</td>
<td></td>
<td></td>
</tr>
<tr>
<td>SD0 to SD3</td>
<td></td>
<td></td>
</tr>
<tr>
<td>PRESETB</td>
<td></td>
<td></td>
</tr>
<tr>
<td>BKUP_TRG</td>
<td></td>
<td></td>
</tr>
<tr>
<td>BKUP_REQ</td>
<td></td>
<td></td>
</tr>
<tr>
<td>BKUP_CTRL</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Figure 1.3.2 Sequences of DRAM Backup (with the BD9571MWF-M in its Initial State)

The DRAM backup function of the BD9571MWF-M can be controlled not only by the above signals but also by registers. For details, refer to the data sheet for the BD9571MWF-M.
1.4 AVS and DVFS Functions

The BD9571MWF-M takes advantage of the adaptive voltage scaling (AVS) function and dynamic voltage and frequency scaling (DVFS) functions of the SoC to adjust the power-supply voltage (DVFS0.8V) for the CPU accordingly.

Since using the AVS and DVFS functions requires the support by the SoC, contact a Renesas Electronics sales office for details.
2. Design Examples

2.1 Overall Block Diagram

This section takes a design using the R-Car H3 (DRAM: LPDDR4) as an example and describes the overall configuration and gives an overview of each block.

2.1.1 Types of Power Supplies

Refer to section 1.2.

2.1.2 Example of Implementing Power Generation with the Use of the BD9571MWF-M

![Block Diagram of a Power-Supply System (Example)](image-url)
2.1.3 Overview of the Block Diagram
The main components are described below.

2.1.3.1 Primary Power-Supply Block
This block generates the input power-supply voltage (5 V) for the BD9571MWF-M. Design this block to suit the specifications of the inputs to the BD9571MWF-M.

Since the primary power supply is the input section for the external power supply, it requires certain functions, such as maintaining the boot-up state during boot-up of the BD9571MWF-M, the input of external enable signals, and the output of status signals and enable control signals to the secondary power supply block. Design this block to suit the specifications of your system.

2.1.3.2 Secondary Power-Supply Block
The BD9571MWF-M is used as this block. This block generates the SoC core power supplies (VDD0.8V and DVFS0.8V), DDR power supplies (DDR0_1.1V, DDR1_1.1V, DDR0_1.8V, and DDR1_1.8V), I/O power supplies (D1.8V and D3.3V), SD power supplies (VLDO_SD0, VLDO_SD1, VLDO_SD2, and VLDO_SD3), and the power supply for the Ethernet interface (VLDO_2.5V).

2.1.3.3 Control IC
All of the following power-supply control signals are internally handled by the BD9571MWF-M. An additional external control IC is unnecessary.

- **RSTB** --- Control signal for turning the BD9571MWF-M on and off
- **SYSRSTn** --- Manual reset or shutdown control signal
- **I2C** --- Communications signal
- **PRESETn_18** --- Reset signal for the SoC and other devices
- **IRQ0n** --- Interrupt signal
- **BKUP_REQ** --- Signal for starting the PMIC setup for DRAM backup
- **BKUP_TRG** --- Signal for starting the SoC setup for DRAM backup and detecting a cold or warm boot
- **BKUP_CTRL_11** --- Signal for starting DRAM backup
- **SD[3:0]_PWSEL** --- SD voltage control signals
- **AVS[2:1]** --- AVS control signals for the VDD_DVFS power supply
- **BOOST** --- DVFS control signal for the VDD_DVFS power supply
- **PWM** --- External clock signal for switching the DC/DC converter of the BD9571MWF-M
- **DVFS_PGD** --- Signal for indicating the completion of voltage change by the AVS and DVFS functions

2.1.3.4 Power Isolator
This is unnecessary in normal usage. However, when an external EEPROM is used to change the initial state of the BD9571MWF-M, a power isolator has to be inserted along the I2C line. The power isolator switches the D3.3V domain signals to V3P3 domain signals. V3P3 is a power supply for the BD9571MWF-M and EEPROM.
2.1.3.5 Programmable Device

This is unnecessary in normal usage. However, an EEPROM can be used as a programmable device to change the initial state of the BD9571MWF-M. When power is supplied to the BD9571MWF-M, the values in the EEPROM are automatically read.

2.1.3.6 Power-Supply Circuits for Peripheral Circuits

If a type of power supply not supplied by the BD9571MWF-M is necessary or if the amount of current the BD9571MWF-M can drive is insufficient, design the circuits of power supplies for peripheral devices to suit the specifications of your system.

The block diagram shows an example in which 1.2 V is generated from D3.3V by the LDO in a case where an Ethernet PHY device requires a 1.2-V power supply.
2.1.3.7 List of the Allocation of and Correspondences between Pins of the SoC and BD9571MWF-M

The table below shows an example of the allocation of power supplies and signals to individual pins of the SoC and BD9571MWF-M.

### Table 2.1.3.7 Allocation of and Correspondences between Pins (Example)

<table>
<thead>
<tr>
<th>BD9571MWF-M</th>
<th>Pin Name</th>
<th>I/O</th>
<th>SoC Pin Name</th>
<th>I/O</th>
<th>Other Connection</th>
<th>Voltage</th>
</tr>
</thead>
<tbody>
<tr>
<td>SW_DVFS</td>
<td>Output</td>
<td>VDD_DVFS</td>
<td>Power</td>
<td>⎯</td>
<td>0.83 V</td>
<td></td>
</tr>
<tr>
<td>SW_VD09</td>
<td>Output</td>
<td>VDD09x</td>
<td>Power</td>
<td>⎯</td>
<td>0.82 V</td>
<td></td>
</tr>
<tr>
<td>DDR0C</td>
<td>Power</td>
<td>⎯</td>
<td>⎯</td>
<td>LPDDR4 (DDR0_1.8V)</td>
<td>1.8 V</td>
<td></td>
</tr>
<tr>
<td>DDR1C</td>
<td>Power</td>
<td>⎯</td>
<td>⎯</td>
<td>LPDDR4 (DDR1_1.8V)</td>
<td>1.8 V</td>
<td></td>
</tr>
<tr>
<td>SW_DDR0</td>
<td>Output</td>
<td>VDDQVA_DDR0</td>
<td>Power</td>
<td>⎯</td>
<td>1.1 V</td>
<td></td>
</tr>
<tr>
<td>SW_DDR1</td>
<td>Output</td>
<td>VDDQVA_DDR1</td>
<td>Power</td>
<td>⎯</td>
<td>1.1 V</td>
<td></td>
</tr>
<tr>
<td>SW_VD18</td>
<td>Output</td>
<td>VDDQ18, VDDQ18x, VDD18x</td>
<td>Power</td>
<td>Peripheral</td>
<td>1.8 V</td>
<td></td>
</tr>
<tr>
<td>SW_VD33</td>
<td>Output</td>
<td>VDDQ33, VDDQ33x, VDD33x</td>
<td>Power</td>
<td>Peripheral</td>
<td>3.3 V</td>
<td></td>
</tr>
<tr>
<td>SD0</td>
<td>Power</td>
<td>VDDQVA_SD0</td>
<td>Power</td>
<td>⎯</td>
<td>1.8 V or 3.3 V</td>
<td></td>
</tr>
<tr>
<td>SD1</td>
<td>Power</td>
<td>VDDQVA_SD1</td>
<td>Power</td>
<td>⎯</td>
<td>1.8 V or 3.3 V</td>
<td></td>
</tr>
<tr>
<td>SD2</td>
<td>Power</td>
<td>VDDQVA_SD2</td>
<td>Power</td>
<td>⎯</td>
<td>1.8 V or 3.3 V</td>
<td></td>
</tr>
<tr>
<td>SD3</td>
<td>Power</td>
<td>VDDQVA_SD3</td>
<td>Power</td>
<td>⎯</td>
<td>1.8 V or 3.3 V</td>
<td></td>
</tr>
<tr>
<td>VD25</td>
<td>Power</td>
<td>VDDQ25_ETH</td>
<td>Power</td>
<td>Peripheral</td>
<td>2.5 V</td>
<td></td>
</tr>
<tr>
<td>PRESETB</td>
<td>Output</td>
<td>PRESET#</td>
<td>Input</td>
<td>⎯</td>
<td>O.D. (1.8 V)</td>
<td></td>
</tr>
<tr>
<td>I2C_SCL</td>
<td>I/O</td>
<td>I2C/IIC_SCL</td>
<td>I/O</td>
<td>EEPROM</td>
<td>O.D. *2</td>
<td></td>
</tr>
<tr>
<td>I2C_SDA</td>
<td>I/O</td>
<td>I2C/IIC_SDA</td>
<td>I/O</td>
<td>EEPROM</td>
<td>O.D. *2</td>
<td></td>
</tr>
<tr>
<td>AVS0</td>
<td>Input</td>
<td>AVS1</td>
<td>Output</td>
<td>⎯</td>
<td>3.3 V</td>
<td></td>
</tr>
<tr>
<td>AVS1</td>
<td>Input</td>
<td>AVS2</td>
<td>Output</td>
<td>⎯</td>
<td>3.3 V</td>
<td></td>
</tr>
<tr>
<td>BOOT</td>
<td>Input</td>
<td>GPIO</td>
<td>Output</td>
<td>⎯</td>
<td>3.3 V</td>
<td></td>
</tr>
<tr>
<td>SYNC</td>
<td>Input</td>
<td>PWM</td>
<td>Output</td>
<td>⎯</td>
<td>3.3 V</td>
<td></td>
</tr>
<tr>
<td>BKUP_TRG</td>
<td>Output</td>
<td>GPIO</td>
<td>Input</td>
<td>⎯</td>
<td>3.3 V</td>
<td></td>
</tr>
<tr>
<td>BKUP_CTRL</td>
<td>Output</td>
<td>MBKUP</td>
<td>Input</td>
<td>1.1 V, 1.35 V, or 1.5 V *3</td>
<td>3.3 V</td>
<td></td>
</tr>
<tr>
<td>BKUP_REQ</td>
<td>Input</td>
<td>GPIO</td>
<td>Input</td>
<td>⎯</td>
<td>3.3 V</td>
<td></td>
</tr>
<tr>
<td>INT_B</td>
<td>Output</td>
<td>IRQ</td>
<td>Input</td>
<td>⎯</td>
<td>3.3 V</td>
<td></td>
</tr>
<tr>
<td>DVFS_PGD</td>
<td>Output</td>
<td>GPIO</td>
<td>Input</td>
<td>⎯</td>
<td>3.3 V</td>
<td></td>
</tr>
<tr>
<td>SD0_VL</td>
<td>Input</td>
<td>GPIO</td>
<td>Output</td>
<td>⎯</td>
<td>3.3 V</td>
<td></td>
</tr>
<tr>
<td>SD1_VL</td>
<td>Input</td>
<td>GPIO</td>
<td>Output</td>
<td>⎯</td>
<td>3.3 V</td>
<td></td>
</tr>
<tr>
<td>SD2_VL</td>
<td>Input</td>
<td>GPIO</td>
<td>Output</td>
<td>⎯</td>
<td>3.3 V</td>
<td></td>
</tr>
<tr>
<td>SD3_VL</td>
<td>Input</td>
<td>GPIO</td>
<td>Output</td>
<td>⎯</td>
<td>3.3 V</td>
<td></td>
</tr>
</tbody>
</table>

Notes:
1. The SoC has multiple available signals of this type. Select the one that suits the specifications of your system.
2. This is an open-drain output pin. Set a pull-up voltage that suits the specifications of your system.
3. Select a voltage that suits the I/O power supplies of the DRAM.
2.2 Control Specifications
This section describes the specifications of the control signals between the SoC and BD9571MWF-M.

2.2.1 Control Specifications
2.2.1.1 I2C
The I2C signals used for communications between the SoC and BD9571MWF-M can be used by the SoC to make settings for the BD9571MWF-M. The I2C_SCL and I2C_SDA pins of the BD9571MWF-M are connected to the I2C pins of the SoC. As signals on the I2C pins of the BD9571MWF-M are from 3.3-V open-drain outputs, connect resistors to both signal lines to pull the signals up to the D3.3V power-supply voltage. Since the SoC has multiple I2C interfaces, select the one that best suits the specifications of your system.

Figure 2.2.1.1 Diagram of Connections of the I2C Signals (Normal Usage)

Connecting an EEPROM to the BD9571MWF-M through the I2C enables initial settings of the BD9571MWF-M-related registers and adjusting them from their initial values. When an EEPROM is connected to the I2C signal lines, the BD9571MWF-M will automatically read the values from the EEPROM at the time the power is turned on. At this point in time, the only power-supply output from the BD9571MWF-M is V3P3. Therefore, the I2C bus lines for the EEPROM and BD9571MWF-M must be pulled up to the V3P3 power supply. However, since power is not being supplied to the SoC at this point, the power supplies of the SoC and BD9571MWF-M have to be separated by an isolator.

Figure 2.2.1.2 Diagram of Connections of the I2C Signals (with Use of an EEPROM)

Table 2.2.1.1 Pins for Use with the I2C Signals

<table>
<thead>
<tr>
<th>Signal Name</th>
<th>Function</th>
<th>BD9571MWF-M Pin</th>
<th>SoC Pin</th>
<th>Voltage</th>
<th>Note</th>
</tr>
</thead>
<tbody>
<tr>
<td>SCL_DVFS</td>
<td>I2C clock</td>
<td>I2C_SCL</td>
<td>I2C/IIC_SCL</td>
<td>3.3 V</td>
<td></td>
</tr>
<tr>
<td>SDA_DVFS</td>
<td>I2C data</td>
<td>I2C_SDA</td>
<td>I2C/IIC_SDA</td>
<td>3.3 V</td>
<td></td>
</tr>
</tbody>
</table>

Note: * Select an I2C or IIC interface that suits the specifications of your system.
2.2.1.2 SPI

The SPI cannot be used instead of the I2C as a means of communications between the BD9571MWF-M and SoC.

2.2.1.3 PRESETn_18

The PRESETB pin of the BD9571MWF-M is used for output of the PRESETn_18 reset signal, which is connected to the PRESET# pin of the SoC. As this signal is from an open-drain output, it needs to be pulled up by D1.8V, which is the power domain of the SoC. By connecting this signal to the reset pins of peripheral devices, a reset is applied to the peripheral devices at the same time as the SoC. For the resetting of peripheral devices, refer to the specifications of the given devices.

![Diagram of Connection of the PRESETn_18 Signal](image)

**Figure 2.2.1.3 Diagram of Connection of the PRESETn_18 Signal**

Table 2.2.1.3 Pin for Use with the PRESETn_18 Signal

<table>
<thead>
<tr>
<th>Signal Name</th>
<th>Function</th>
<th>BD9571MWF-M</th>
<th>SoC</th>
<th>Voltage</th>
<th>Note</th>
</tr>
</thead>
<tbody>
<tr>
<td>PRESETn_18</td>
<td>Reset signal for SoC and peripheral devices</td>
<td>PRESETB</td>
<td>PRESET#</td>
<td>1.8 V</td>
<td></td>
</tr>
</tbody>
</table>
2.2.1.4 IRQ0n

The IRQ0n signal is for indicating that an interrupt has occurred in the BD9571MWF-M. The INT_B pin of the BD9571MWF-M is connected to the IRQ0 pin of the SoC.

![Diagram of Connection of the IRQ0n Signal](image)

**Figure 2.2.1.4 Diagram of Connection of the IRQ0n Signal**

**Table 2.2.1.4 Pin for Use with the IRQ0n Signal**

<table>
<thead>
<tr>
<th>Signal Name</th>
<th>Function</th>
<th>BD9571MWF-M</th>
<th>SoC</th>
</tr>
</thead>
<tbody>
<tr>
<td>IRQ0n</td>
<td>Interrupt signals to indicate the occurrence of events to the SoC</td>
<td>INT_B</td>
<td>IRQ *</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Voltage</th>
<th>Note</th>
</tr>
</thead>
<tbody>
<tr>
<td>3.3 V</td>
<td></td>
</tr>
</tbody>
</table>

Note: * Select an IRQ channel that suits the specifications of your system.
2.2.1.5 DRAM Backup Control Signals

The DRAM backup control signals are for use with the DRAM backup function of the SoC. The BKUP_TRG, BKUP_REQ, and BKUP_CTRL pins of the BD9571MWF-M are used. They are respectively connected to GPIO pins and the M*BKUP pin of the SoC. A voltage suiting the DRAM specifications must be applied to the M*BKUP pin of the SoC. Specifically, the voltages are 1.1 V for LPDDR4 and 1.35 V or 1.5 V for DDR3L or DDR3. As the electric potential of the BKUP_CTRL signal of the BD9571MWF-M is the voltage input to the VL_CTRL pin, power must be supplied in accord with the specifications of your system.

If the DRAM backup function is not to be used, none of these pins need be connected.

![Diagram of Connections of the DRAM Backup Control Signals](image)

**Figure 2.2.1.5** Diagram of Connections of the DRAM Backup Control Signals

**Table 2.2.1.5 Pins for Use with the DRAM Backup Control Signals**

<table>
<thead>
<tr>
<th>Signal Name</th>
<th>Function</th>
<th>BD9571MWF-M Pin</th>
<th>SoC Pin</th>
<th>Voltage</th>
<th>Note</th>
</tr>
</thead>
<tbody>
<tr>
<td>BKUP_TRG</td>
<td>Signal for starting the SoC setup for backup and detecting a cold or warm boot</td>
<td>BKUP_TRG</td>
<td>GPIO</td>
<td>3.3 V</td>
<td></td>
</tr>
<tr>
<td>BKUP_REQB</td>
<td>Signal for starting the PMIC setup for backup</td>
<td>BKUP_REQB</td>
<td>GPIO</td>
<td>3.3 V</td>
<td></td>
</tr>
<tr>
<td>BKUP_CTRL_11</td>
<td>Signal for starting backup</td>
<td>BKUP_CTRL</td>
<td>M*BKUP</td>
<td>1.1 V, 1.35 V, or 1.5 V</td>
<td>Note: * Select a GPIO pin that suits the specifications of your system.</td>
</tr>
</tbody>
</table>

Note: * Select a GPIO pin that suits the specifications of your system.
2.2.1.6 SD Voltage Control Signals

The SD power-supply voltage control signals can be used to change the voltage of the VLDO_SD0, VLDO_SD1, VLDO_SD2, and VLDO_SD3 power supplies of the BD9571MWF-M. When the level of the control signal is high, the corresponding power supply output is 3.3 V. When the level of the control signal is low, the corresponding power supply output is 1.8 V.

To dynamically control the power supply outputs, connect the SD voltage control signals to the GPIO pins of the SoC. In this case, make sure that the signals do not become undefined. That is, they are to be either pulled up or pulled down. The figure below shows an example in which all signals are pulled up. If an SD power-supply voltage is to be fixed rather than dynamically controlled, the corresponding signal does not have to be connected to a GPIO pin of the SoC. Fix the SD voltage control signals to the high or low level to suit the specifications of your system.

![Diagram of Connections of the SD Voltage Control Signals](image)

**Figure 2.2.1.6 Diagram of Connections of the SD Voltage Control Signals**

### Table 2.2.1.6 Pins for Use with the SD Voltage Control Signals

<table>
<thead>
<tr>
<th>Signal Name</th>
<th>Function</th>
<th>BD9571MWF-M</th>
<th>SoC</th>
<th>Voltage</th>
<th>Note</th>
</tr>
</thead>
<tbody>
<tr>
<td>SD0_PWSEL</td>
<td>Signal for setting the SD0 voltage</td>
<td>SD0_VL</td>
<td>GPIO *</td>
<td>Output</td>
<td>3.3 V</td>
</tr>
<tr>
<td>SD1_PWSEL</td>
<td>Signal for setting the SD1 voltage</td>
<td>SD1_VL</td>
<td>GPIO *</td>
<td>Output</td>
<td>3.3 V</td>
</tr>
<tr>
<td>SD2_PWSEL</td>
<td>Signal for setting the SD2 voltage</td>
<td>SD2_VL</td>
<td>GPIO *</td>
<td>Output</td>
<td>3.3 V</td>
</tr>
<tr>
<td>SD3_PWSEL</td>
<td>Signal for setting the SD3 voltage</td>
<td>SD3_VL</td>
<td>GPIO *</td>
<td>Output</td>
<td>3.3 V</td>
</tr>
</tbody>
</table>

*Select a GPIO pin that suits the specifications of your system.*

### Table 2.2.1.7 Truth-Value Table for the SD Voltage Control Signals

<table>
<thead>
<tr>
<th>SDx_VL (x: 0 to 3)</th>
<th>PU/PD</th>
<th>SDx_VL Voltage Threshold</th>
<th>SDx Output Voltage (x: 0 to 3)</th>
</tr>
</thead>
<tbody>
<tr>
<td>High level</td>
<td>PU</td>
<td>2.2 V to 3.6 V</td>
<td>3.3 V</td>
</tr>
<tr>
<td>Low level</td>
<td>PD</td>
<td>-0.3 V to +0.5 V</td>
<td>1.8 V</td>
</tr>
</tbody>
</table>
2.2.1.7 AVS

The AVS signals are dedicated to the AVS function of the SoC. The DVFS power supply voltages are separately set in registers of the BD9571MWF-M that are selected by the combination of these signals.

The AVS0 and AVS1 pins of the BD9571MWF-M are exclusively for use for the AVS and are connected to the AVS1 and AVS2 pins of the SoC, respectively. If the pins are not to be used, they need not be connected with the SoC pins. In such cases, connect the AVS0 and AVS1 pins of the BD9571MWF-M to ground.

![Diagram of Connections of the AVS Control Signals](image)

**Table 2.2.1.7 Pins for Use with the AVS Control Signals**

<table>
<thead>
<tr>
<th>Signal Name</th>
<th>Function</th>
<th>BD9571MWF-M</th>
<th>SoC</th>
<th>Voltage</th>
</tr>
</thead>
<tbody>
<tr>
<td>AVS1</td>
<td>AVS</td>
<td>AVS0 Input</td>
<td>AVS1 Output</td>
<td>3.3 V</td>
</tr>
<tr>
<td>AVS2</td>
<td>AVS</td>
<td>AVS1 Input</td>
<td>AVS2 Output</td>
<td>3.3 V</td>
</tr>
</tbody>
</table>

2.2.1.8 BOOST

The BOOST signal is dedicated to the DVFS function of the SoC. The DVFS function is controlled through the I2C interface as well as by this pin. When this signal goes to the high level, the DVFS power supply voltages are separately set in registers.

The BOOST pin of the BD9571MWF-M is used for the BOOST signal, which is connected to a GPIO pin of the SoC. If the pin is not to be used, it need not be connected with the SoC pin.

![Diagram of Connection of the BOOST Signal](image)

**Table 2.2.1.8 Pin for Use with the BOOST Signal**

<table>
<thead>
<tr>
<th>Signal Name</th>
<th>Function</th>
<th>BD9571MWF-M</th>
<th>SoC</th>
<th>Voltage</th>
</tr>
</thead>
<tbody>
<tr>
<td>BOOST</td>
<td>Voltage change in DVFS0.8V</td>
<td>BOOST Input</td>
<td>GPIO * Output</td>
<td>3.3 V</td>
</tr>
</tbody>
</table>

Note: * The GPIO pin to be used is freely selectable.
2.2.1.9 SYNC

The SYNC signal is an external clock signal for switching the DC/DC converter of the BD9571MWF-M. The SYNC pin of the BD9571MWF-M is used for the SYNC signal, which is connected to a PWM pin of the SoC. Since the SoC has multiple PWM pins, select the one that best suits the specifications of your system. The PWM pins of the SoC also need to be controlled from the SoC. For details, refer to PWM (section 60) in "R-Car Series, 3rd Generation for User’s Manual: Hardware".

When connecting this pin and a PWM pin of the SoC, connect an external pull-down resistor with a value no greater than 10 kΩ because the SoC has an internal pull-up resistor and the BD9571MWF-M has an internal pull-down resistor. Connecting the SYNC pin with the SoC pin and inserting the pull-down resistor are unnecessary if the SYNC signal is not to be used.

![Diagram of Connection of the SYNC Signal](image)

**Table 2.2.1.9 Pin for Use with the SYNC Signal**

<table>
<thead>
<tr>
<th>Signal Name</th>
<th>Function</th>
<th>BD9571MWF-M</th>
<th>SoC</th>
<th>Voltage</th>
<th>Note</th>
</tr>
</thead>
<tbody>
<tr>
<td>PWM</td>
<td>External synchronization</td>
<td>SYNC</td>
<td>PWM *</td>
<td>3.3 V</td>
<td></td>
</tr>
</tbody>
</table>

Note: * The PWM channel to be used is freely selectable.
2.2.1.10 DVFS_PGD

The DVFS_PGD signal is for indicating that changing of the DVFS0.8V voltage of the BD9571MWF-M has completed. The DVFS_PGD pin of the BD9571MWF-M is used for this control signal, which is connected to a GPIO pin of the SoC. Since the SoC has multiple GPIO pins, select the one that best suits the specifications of your system. If the DVFS_PGD signal is not to be used, the DVFS_PGD pin need not be connected with the SoC pin.

![Diagram of Connection of the DVFS_PGD Signal](image)

Figure 2.2.1.10 Diagram of Connection of the DVFS_PGD Signal

| Table 2.2.1.10 Pin for Use with the DVFS_PGD Signal |
|---------------------------------|---------------|---------------|--------------|----------------|
| **Signal Name** | **Function** | **BD9571MWF-M** | **SoC** | **Voltage** | **Note** |
| DVFS_PGD | Power-good signal for the DVFS function | DVFS_PGD | GPIO * | Input | 3.3 V |

Note: * The GPIO pin to be used is freely selectable.
2.2.1.11 How to Calculate the Values of Pull-Up and Pull-Down Resistors

Use pull-up and pull-down resistors with values from several kΩ to several tens of kΩ.

Follow the recommended resistance values in cases where they are defined in the interface standards for signals. When a single pin is to be both pulled up and pulled down, make sure to design the circuit so that the resistors do not create a short-circuit between the power supply and ground.

A method of calculating the values of pull-up and power-down resistors is described below for reference.

The pull-up and pull-down resistor values for an SDx_VL signal are calculated here by way of example. The threshold values of the high and low levels are as follows:

- **High level:** 2.2 V to 3.6 V
- **Low level:** −0.3 V to 0.6 V

The maximum resistor values are calculated under the condition of fixing the signal to the high or low level when the I/O pin that drives this signal is in the high-impedance state. The pin which drives this signal belongs to the 3.3-V I/O power domain of the SoC, so its maximum leakage current is 10 μA when in the high-impedance state. The voltages must not exceed the above threshold values even if this maximum leakage current flows.

- **Maximum pull-up resistor value:** \( R_{PU} - max < \frac{(V_{DDQ33} \text{ min} - 2.2)}{10 \mu A} = 80 \text{ kΩ} \)
- **Maximum pull-down resistor value:** \( R_{PD} - max < \frac{0.6}{10 \mu A} = 60 \text{ kΩ} \)

A maximum value for the resistor including a margin in terms of the voltage and current in the range from 10 kΩ to 47 kΩ is typical.

Next, the minimum resistor values are calculated under the condition of being able to drive this signal to the high or low level.

As IOL and IOH (low- and high-level output currents) are 4 and −4 mA and VOL and VOH (low and high output voltages) are a maximum of 0.4 V and minimum of 2.4 V for the 3.3-V I/O power supply, the minimum resistor values are calculated as follows:

- **Minimum pull-up resistor value:** \( R_{PU} - min = \frac{(V_{DDQ33} \text{ max} - 0.4)}{4 \text{ mA}} = 800 \text{ Ω} \)
- **Minimum pull-down resistor value:** \( R_{PD} - min > \frac{2.2}{4 \text{ mA}} = 550 \text{ Ω} \)

A minimum value of the resistor including a margin in terms of the voltage and current in the range from 1 kΩ to 4.7 kΩ is typical.
2.3 Primary Power Supply
Design this power supply in accord with the specifications of the device in use.

2.4 Core Power Supplies of the Secondary Power Supply Block (BD9571MWF-M)
This section describes examples of the design of the power-supply (VDD0.8V and DVFS0.8V) circuits for the cores of the SoC. In the examples of design given in this document, the circuits and peripheral components comply with the recommendations made by ROHM. The SoC peripheral circuits following the smoothing capacitors are designed in accord with the design guidelines for the SoC. For further details, refer to the recommendations in related documents.

2.4.1 Examples of Circuits

(1) Power-supply input circuit for the BD9571MWF-M

![Power-Supply Input Circuit for the BD9571MWF-M](image)

In this circuit configuration, the 5 V that the primary power supply generates is input to a 5-V input (V5AIN) of the BD9571MWF-M and the 3.3 V (V3P3) that is self-generated for the BD9571MWF-M logic is input to V3P3IN.

Connect a capacitor (C1 or C2) for smoothing the power-supply input to each power-supply input.
(2) Output circuit from DVFS0.8V

![Diagram of output circuit from DVFS0.8V]

**Figure 2.4.1.2  Output Circuit from DVFS0.8V**

DVFS0.8V is produced by a switching regulator consisting of a DC/DC controller in the BD9571MWF-M and an external MOSFET. In addition, an output inductor and smoothing capacitors need to be placed in the output stage.

Supply the 5 V that is generated by the primary power supply to the power supply of a MOSFET (U1). Connect the control signal from the HG_DVFS pin with the gate of the high-side switch and the control signal from the LG_DVFS pin with the gate of the low-side switch.

Connect an inductor (L1) in the stage following the MOSFETs. In parallel with the inductor, connect the power-supply input side of the current detection filter circuit (R1, R2, and C4) of the BD9571MWF-M with the IS_P_DVFS pin and the power-supply output side with the IS_M_DVFS pin.

Connect smoothing capacitors (C5 to C14) to the stage following the inductor. The capacitance and the number of capacitors may vary with the load conditions.

The two feedback pins for sensing the power-supply voltage and GND are used for the feedback signals of the DVFS channel of the BD9571MWF-M. Connect the DVFS0.8V power supply in the vicinity of the load with the FB_DVFS pin and GND with the REMOTE_M_DVFS pin to form paired wiring.

The internal equivalent resistance of L1 is used for detecting current. R1, R2, and C4 form a circuit constituting a current sense amplifier. The BOOT pin must be connected with the SW pin via a capacitor.

Select the constants of these circuits based on the data sheet for the PMIC.
Output circuit from VDD0.8V

VDD0.8V is produced by a switching regulator consisting of a DC/DC controller in the BD9571MWF-M and an external MOSFET. In addition, an output inductor and smoothing capacitors need to be placed in the output stage.

Supply the 5 V that is generated by the primary power supply to the power supply of a MOSFET (U1). Connect the control signal from the HG_VD09 pin with the gate of the high-side switch and the control signal from the LG_VD09 pin with the gate of the low-side switch.

Connect an inductor (L1) in the stage following the MOSFETs. In parallel with the inductor, connect the power-supply input side of the current detection filter circuit (R1, R2, and C4) of the BD9571MWF-M with the IS_P_VD09 pin and the power-supply output side with the IS_M_VD09 pin.

Connect smoothing capacitors that suit the current load specifications to the stage following the inductor. As the feedback signals have to follow up the load fluctuation, connect the VDD0.8V power supply with the FB_VD09 pin at a point close to the load fluctuation.

The internal equivalent resistance of L1 is used for detecting current. R1, R2, and C4 form a circuit constituting a current sense amplifier. The BOOT pin must be connected with the SW pin via a capacitor. Select the constants of these circuits based on the data sheet for the PMIC.
2.4.2 Peripheral Components

(1) Power-supply input section for the BD9571MWF-M

<table>
<thead>
<tr>
<th>Table 2.4.2.1 Components in the Power-Supply Input Section for the BD9571MWF-M</th>
</tr>
</thead>
<tbody>
<tr>
<td>Part Name</td>
</tr>
<tr>
<td>-----------</td>
</tr>
<tr>
<td>C1</td>
</tr>
<tr>
<td>C2</td>
</tr>
</tbody>
</table>

Note: * The withstand voltage must be sufficient.

(2) Output section from DVFS0.8V

<table>
<thead>
<tr>
<th>Table 2.4.2.2 Components in the DVFS0.8V Output Section</th>
</tr>
</thead>
<tbody>
<tr>
<td>Part Name</td>
</tr>
<tr>
<td>-----------</td>
</tr>
<tr>
<td>U1A, U1B</td>
</tr>
<tr>
<td>C1</td>
</tr>
<tr>
<td>C2</td>
</tr>
<tr>
<td>C3</td>
</tr>
<tr>
<td>L1</td>
</tr>
<tr>
<td>R1</td>
</tr>
<tr>
<td>R2</td>
</tr>
<tr>
<td>C4</td>
</tr>
<tr>
<td>C5, C6, C7, C8, C9, C10, C11, C12, C13, C14</td>
</tr>
</tbody>
</table>

Notes:
1. Value recommended by ROHM Co., Ltd.
2. The withstand voltage must be sufficient.
3. The number of capacitors and their capacitance depend on the use case and reductions may be possible.
### Output section from VDD0.8V

#### Table 2.4.2.3 Components in the VDD0.8V Output Section

<table>
<thead>
<tr>
<th>Part Name</th>
<th>Component</th>
<th>Qty</th>
<th>Part (or Parts)</th>
<th>Value</th>
<th>Note</th>
</tr>
</thead>
<tbody>
<tr>
<td>U2A, U2B</td>
<td>MOSFET</td>
<td>1</td>
<td>IPG20N04S4L-08*1</td>
<td>20 A</td>
<td>RDS (ON) = max. 8.2 mΩ</td>
</tr>
<tr>
<td>C1</td>
<td>Cin for MOSFET</td>
<td>1</td>
<td>Capacitor</td>
<td>0.1 μF</td>
<td>*2</td>
</tr>
<tr>
<td>C2</td>
<td>Cin for MOSFET</td>
<td>1</td>
<td>Capacitor</td>
<td>47 μF</td>
<td>*2</td>
</tr>
<tr>
<td>C3</td>
<td>C for BOOT_DVFS pin</td>
<td>1</td>
<td>Capacitor</td>
<td>0.1 μF</td>
<td>*2</td>
</tr>
<tr>
<td>L1</td>
<td>Inductor</td>
<td>1</td>
<td>SPM5030VT-R15M-D*1</td>
<td>0.15 μH</td>
<td>Itemp = 17.1 A Isat = 20.2 A Rdc = 3.0 mΩ</td>
</tr>
<tr>
<td>R1</td>
<td>RC filter for current sense</td>
<td>1</td>
<td>Resistor</td>
<td>510 Ω</td>
<td></td>
</tr>
<tr>
<td>R2</td>
<td>RC filter for current sense</td>
<td>1</td>
<td>Resistor</td>
<td>—</td>
<td>Do Not Populate (for adjustment)</td>
</tr>
<tr>
<td>C4</td>
<td>RC filter for current sense</td>
<td>1</td>
<td>Capacitor</td>
<td>0.1 μF</td>
<td>*2</td>
</tr>
<tr>
<td>C5, C6, C7, C8, C9, C10</td>
<td>Cout for VDD0.8V</td>
<td>6*3</td>
<td>Capacitor</td>
<td>47 μF</td>
<td></td>
</tr>
</tbody>
</table>

**Notes:**
1. Value recommended by ROHM Co., Ltd.
2. The withstand voltage must be sufficient.
3. The number of capacitors and the capacitance depend on the use case and are adjustable.
2.4.3 PCB Design

In multi-layered PCBs in general, in terms of the wiring and connections between components, the top and bottom layers are used as signal layers and GND layers are placed adjacent to those layers to prevent noise propagation or adjust the impedances. Therefore, the power-supply patterns are to be placed in a layer further within the board but placing them in a layer adjacent to a GND layer as much as possible is recommended in order to lower the impedance.

The power-supply patterns connect the sources and destinations for the supply of power with the shortest possible paths. The maximum currents of the power supplies determine the widths of the wiring patterns of the paths.

The two core power supplies (VDD0.8V and DVFS0.8V) require two layers for supplying power because their wiring patterns are wide and their destinations for the supply of power are almost the same. As a result, in the configuration of a PCB with the fewest possible layers, the signal layers are the top and bottom layers, the GND layers are the L2 and L5 layers, and the power-supply layers are the L3 and L4 layers.

When inter-layer connections are to be made, as well as the widths of the power-supply patterns, the values of the maximum currents determine the numbers of via holes. Placing sufficient via holes and designing the wiring patterns to be wide enough to allow for the maximum currents for the SoC flowing through the power-supply paths are both recommended. As the maximum currents depend on the use case, adjust the board design to suit the specifications of your system.

In order to obtain correct power-supply outputs, draw out the wiring for the feedback signal line by placing monitoring points close to the load to minimize the effects of noise from the power supplies and signals on the feedback signals.

In regard to peripheral components, place the FETs in the vicinity of the BD9571MWF because the signals connecting the FETs with the BD9571MWF-M will be sources of noise. For the same reason, place the inductor in the vicinity of the FET. Place capacitors in the neighborhood of the power supplies or signal pins to which they are to be connected.

<Example of pattern design>

The design of the patterns for an evaluation board for the R-Car H3 SiP is taken as an example in this section and shown in the above figure as a six-layer board with plated through-holes. As stated above, the signal layers are the top and bottom layers, the GND layers are the L2 and L5 layers, and the power-supply layers are the L3 and L4 layers. DVFS0.8V and VDD0.8V are also placed in the top layer, and power is supplied to the SiP via through holes and the DVFS0.8V power-supply plane in the L4 layer and the VDD0.8V power-supply plane in the L3 layer, respectively.

To allow sufficient current to flow, the widths of the wiring patterns and the numbers of through hole holes in the planes for the core power supplies are as follows.
Note: In this example, a 1-mm trace width per 1 A is ensured under the condition of the copper wiring pattern being 35-μm thick.

- **DVFS0.8V**
  Width of the wiring patterns: 20 mm (20 A is ensured)
  Via holes: 1.2 mm × 11, 0.6 mm × 30 (20 A and the low-impedance state are ensured)

- **VDD0.8V**
  Width of the wiring patterns: 10 mm (10 A is ensured)
  Via holes: 1.2 mm × 13 (10 A and the low-impedance state are ensured)

For the feedback signals (red patterns in the figure below) for DVFS0.8V, the wiring patterns for the signals from the monitoring points at both ends of the bypass capacitors directly below the SiP to the PMIC pins are placed in the bottom layer, on which the power supplies have little effect. Also, for the feedback signals (yellow patterns in the other figure below) for VDD0.8V, the wiring patterns for the signals from the monitoring points at both ends of the bypass capacitors directly below the SiP to the PMIC pins are placed in the bottom layer.

**Figure 2.4.3.2 Layout of DVFS0.8V and VDD0.8V feedback**
The paths along which genuinely large currents are able to flow in the PMIC circuit are as follows.

Low -> High: Cin - FET - L - Cout - GND – Cin
High -> Low: GND - FET - L - Cout - GND

To suppress the generation of noise, components are placed and wiring patterns are designed to minimize the lengths of the above current loops.

For these power-supply paths, design the wiring patterns to be wide enough and place sufficient via holes along them.

Figure 2.4.3.3  Peripheral Components
2.5 I/O Power Supplies from the Secondary Power Supply Block (BD9571MWF-M)

This section describes examples of the design of circuits related to the I/O power supplies for the SoC (D1.8V, D3.3V, VLDO_2.5V, VLDO_SD0, VLDO_SD1, VLDO_SD2, and VLDO_SD3). Note that the specifications of the circuits and peripheral components comply with the recommendations made by ROHM. When designing the circuits around the SoC and peripheral devices following the smoothing capacitors, refer to the specifications of the SoC and devices and design the circuits to suit the specifications.

2.5.1 Examples of Circuits

(1) Output circuit from D1.8V

As D1.8V uses the VD18 channel of the DC/DC converter with FETs in the BD9571MWF-M, its circuit components are an inductor and capacitors used for smoothing.

Supply the 5 V that is generated by the primary power supply to the DC/DC converter power-supply input of the BD9571MWF-M and connect an input capacitor (C1). Connect an inductor (L1) to the SW_VD18 output pin of the DC/DC converter and also connect a smoothing capacitor (C2) to the stage following the inductor. The capacitance depends on the use case and may be changed.

Connect the D1.8V power supply with the FB_VD18 pin at a point close to the load to obtain good feedback signals.

**Figure 2.5.1.1 Output Circuit from D1.8V**

As D1.8V uses the VD18 channel of the DC/DC converter with FETs in the BD9571MWF-M, its circuit components are an inductor and capacitors used for smoothing.

Supply the 5 V that is generated by the primary power supply to the DC/DC converter power-supply input of the BD9571MWF-M and connect an input capacitor (C1). Connect an inductor (L1) to the SW_VD18 output pin of the DC/DC converter and also connect a smoothing capacitor (C2) to the stage following the inductor. The capacitance depends on the use case and may be changed.

Connect the D1.8V power supply with the FB_VD18 pin at a point close to the load to obtain good feedback signals.
(2) Output circuit from D3.3V

As D3.3V uses the VD33 channel of a DC/DC converter with FETs in the BD9571MWF-M, its circuit components are an inductor and capacitors used for smoothing.

Supply the 5 V that is generated by the primary power supply to the DC/DC converter power-supply input of the BD9571MWF-M and connect an input capacitor (C1). Connect an inductor (L1) to the SW_VD33 output pin of the DC/DC converter and also connect a smoothing capacitor (C2) to the stage following the inductor. The capacitance depends on the use case and may be changed.
Connect the D3.3V power supply with the FB_VD33 pin at a point close to the load to obtain good feedback signals.

(3) Output circuit from VLDO_2.5V

VLDO_2.5V uses the VD25 channel of the LDO of the BD9571MWF-M. Its circuit components are only capacitors used for smoothing.
Supply the 5 V that is generated by the primary power supply to the LDO power-supply input of the BD9571MWF-M and connect a smoothing capacitor (C1).
Connect a smoothing capacitor (C2) to the VD25 output line.

(4) Output circuit from VLDO_SD0, VLDO_SD1, VLDO_SD2, and VLDO_SD3

![Output Circuit from VLDO_SD0, VLDO_SD1, VLDO_SD2, and VLDO_SD3](image)

**Figure 2.5.1.4  Output Circuit from VLDO_SD0, VLDO_SD1, VLDO_SD2, and VLDO_SD3**

VLDO_SD0, VLDO_SD1, VLDO_SD2, and VLDO_SD3 respectively use the SD0, SD1, SD2, and SD3 channels of the LDO of the BD9571MWF-M. Their circuits components are only capacitors used for smoothing.

Only the SD_IN pin is used for the LDO power-supply input of the SD0, SD1, SD2, and SD3. Supply the 5 V that is generated by the primary power supply to this pin and connect an input capacitor (C1). Connect smoothing capacitors (C2, C3, C4, and C5) to the SD0, SD1, SD2, and SD3 output lines, respectively.
2.5.2 Peripheral Components

(1) Output section from D1.8V

<table>
<thead>
<tr>
<th>Table 2.5.2.1 Components in the D1.8V Output Section</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Part Name</strong></td>
</tr>
<tr>
<td>L1</td>
</tr>
<tr>
<td>C1</td>
</tr>
<tr>
<td>C2</td>
</tr>
</tbody>
</table>

Notes: 1. Value recommended by ROHM Co., Ltd.
2. The withstand voltage must be sufficient.

(2) Output section from D3.3V

<table>
<thead>
<tr>
<th>Table 2.5.2.2 Components in the D3.3V Output Section</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Part Name</strong></td>
</tr>
<tr>
<td>L1</td>
</tr>
<tr>
<td>C1</td>
</tr>
<tr>
<td>C2</td>
</tr>
</tbody>
</table>

Notes: 1. Value recommended by ROHM Co., Ltd.
2. The withstand voltage must be sufficient.

(3) Output section from VLDO_2.5V

<table>
<thead>
<tr>
<th>Table 2.5.2.3 Components in the VLDO_2.5V Output Section</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Part Name</strong></td>
</tr>
<tr>
<td>C1</td>
</tr>
<tr>
<td>C2</td>
</tr>
</tbody>
</table>

Note: * The withstand voltage must be sufficient.

(4) Output section from VLDO_SD0, VLDO_SD1, VLDO_SD2, and VLDO_SD3

<table>
<thead>
<tr>
<th>Table 2.5.2.4 Components in the Output Section from VLDO_SD0, VLDO_SD1, VLDO_SD2, and VLDO_SD3</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Part Name</strong></td>
</tr>
<tr>
<td>C1</td>
</tr>
<tr>
<td>C2</td>
</tr>
</tbody>
</table>

Note: * The withstand voltage must be sufficient.
2.5.3 PCB Design
2.5.3.1 DC/DC Converters (for D1.8V and D3.3V)

The design policies for wiring patterns from the output sections of the DC/DC converters to each device or circuit are the same as those in section 2.4.3, and the wiring patterns are placed in an inner layer adjacent to a GND layer.

On the other hand, since the BD9571MWF-M has internal FETs, the only main external components of the PMIC circuit from the DC/DC converters to the output capacitors are inductors and capacitors. Therefore, as the signals that are the sources of noise and paths for large currents are concentrated around the BD9571MWF-M, placing the inductors and capacitors near to each other is even more important.

The I/O power supplies will also be used for peripheral circuits and devices other than the SoC itself, so the power-supply patterns will have to be designed as planes that extend over wide ranges.

Make sure patterns are not given curved shapes. Doing so causes return currents that add to the generation of noise.

<Example of pattern design>

The design of the patterns for an evaluation board for the R-Car H3 SiP is taken as an example in this section and shown in the figure on the right as a six-layer board with plated through-holes. In terms of wiring, the top and bottom layers are used as wiring layers, the layers adjacent to these, the L2 and L5 layers are used as GND layers, and the power-supply patterns are placed in the L3 and L4 layers which are adjacent to the GND layers. D3.3V and D1.8V are also placed in the top layer and connected to the power-supply patterns in the L3 and L4 layers via through holes. Power is mainly supplied to the SiP’s peripheral circuits by the L3 layer and the L4 layer supplies power to the peripheral devices.

Based on the maximum current of each power supply, the widths of the wiring patterns and the numbers of via holes are basically as follows.

Note: In this example, a 1-mm trace width per 1 A is ensured under the condition of the copper wiring pattern being 35-μm thick.

- **D1.8V**
  - Width of the wiring patterns: 6.7 mm (at least 3 A is ensured)
  - Via holes: 0.6 mm × 6 (at least 3 A is ensured)
- **D3.3V**
  - Width of the wiring patterns: 6.5 mm (at least 3 A is ensured)
  - Via holes: 0.6 mm × 10 (at least 3 A is ensured)

Note: In this example, a 1-mm trace width per 1 A is ensured under the condition of the copper wiring pattern being 35-μm thick.

- **D1.8V**
  - Width of the wiring patterns: 6.7 mm (at least 3 A is ensured)
  - Via holes: 0.6 mm × 6 (at least 3 A is ensured)
- **D3.3V**
  - Width of the wiring patterns: 6.5 mm (at least 3 A is ensured)
  - Via holes: 0.6 mm × 10 (at least 3 A is ensured)
The values given on the previous page are design values for expanding the wiring patterns over a wide area in the power-supply planes. Design the wiring patterns to be wide enough to allow the maximum current required in the paths to the peripheral circuits and devices to flow and open the predetermined number of via holes.

The feedback signals of the I/O power supplies run via through holes where the power-supply line branches as monitoring points. This is to avoid the effects of local voltage drops in circuit terminations or devices on the voltages of all I/O power supplies. Therefore, the voltage drops must be separately confirmed for each circuit or device. The wiring patterns for the signals between the monitoring points and PMIC pins are placed in the bottom layer, on which the power supplies have little effect.

For the layout of peripheral devices other than the SoC, follow the guidelines for the individual devices when placing them.

The paths along which genuinely large currents are able to flow in the PMIC circuit are as follows.

Low -> High: Cin - PMIC - L - Cout - GND - Cin
High -> Low: GND - PMIC - L - Cout - GND

To suppress the generation of noise, components are placed and wiring patterns are designed to minimize the lengths of the above current loops.

For these power-supply paths, design the wiring patterns to be wide enough and place sufficient via holes along them.

Figure 2.5.3.2  Peripheral Components
2.5.3.2 LDO (VLDO_2.5V, VLDO_SD0, VLDO_SD1, VLDO_SD2, VLDO_SD3)

The design policies for wiring patterns from the output sections of the LDO power supplies to each device or circuit are the same as those in section 2.4.3, and the wiring patterns are placed in an inner layer adjacent to a GND layer.

However, the only external components used for the LDO are the input and output capacitors. There are no feedback signals.

The input capacitor is connected for bypassing the inrush current. The output capacitors are connected for use in phase compensation and improving load-transient response (smoothing). In both cases, parasitic resistance or parasitic inductance in patterns will increase the possibility of these components becoming ineffective. Therefore, the capacitors must be placed in the vicinity of the PMIC pins to minimize the lengths of the wiring patterns.

<Example of pattern design>
The design of the patterns for an evaluation board for the R-Car H3 SiP is taken as an example in this section and shown in the figure on the right as a six-layer board with plated through-holes. In terms of wiring, the top and bottom layers are used as wiring layers and the layers adjacent to these, the L2 and L5 layers are used as GND layers. Each power supply from the LDO is connected to three of the layers that are adjacent to GND layers through the 600-μm wide wiring patterns in the L3 layer. In addition to the output capacitors near the LDO, bypass capacitors near the pins of the devices to which power is supplied are also connected in the LDO circuits.

Based on the maximum current of each power supply and considering the current capacity, the width of the wiring patterns and the number of via holes are as follows.

Note: In this example, a 1-mm trace width per 1 A is ensured under the condition of the copper wiring pattern being 35-μm thick.

Width of the wiring patterns: 0.6 mm (at least 170 mA is ensured)
Via hole: 0.6 mm × 1 (at least 170 mA is ensured)

Figure 2.5.3.3 Layout of VLDO_2.5V, VLDO_SD0, VLDO_SD1, VLDO_SD2, and VLDO_SD3
2.6 DRAM Power Supplies from the Secondary Power Supply Block (BD9571MWF-M)

This section describes examples of the design of circuits related to the I/O power supplies (DDR0_1.1V and DDR1_1.1V) and core power supplies of DRAM (DDR0_1.8V and DDR1_1.8V) for the DRAM. Note that the specifications of the circuits and peripheral components comply with the recommendations made by ROHM. When designing the circuits around the SoC and peripheral DRAM following the smoothing capacitors, refer to the specifications of the SoC and DRAM and design the circuits to suit the specifications.

2.6.1 Examples of Circuits

(1) Output circuit from DDR0_1.1V and DDR1_1.1V

![Diagram](image)

**Figure 2.6.1.1 Output Circuit from DDR0_1.1V**
As DDR0_1.1V and DDR1_1.1V respectively use the DDR0 and DDR1 channels of a DC/DC converter with FETs in the BD9571MWF-M, their circuits require to consist of an inductor and capacitors used for smoothing.

Supply the 5 V that is generated by the primary power supply to the DC/DC converter power-supply input of the BD9571MWF-M and connect a smoothing capacitor (C1 or C7). Connect an inductor (L1 or L2) to the SW_DDR0 or SW_DDR1 output pin of the DC/DC converter and also connect smoothing capacitors (C2-C6 or C8-C12) to the stage following the inductor. The number of capacitors and the capacitance depend on the use case and may be changed. Connect the D1.8V power supply with the FB_DDR0 or FB_DDR1 pin at a point close to the load to obtain good feedback signals. Note that feedback signals from the output voltages of the DDR0 and DDR1 channels of the BD9571MWF-M are to be adjusted through voltage division by external resistors (R1 and R2 or R3 and R4).

(2) Output circuit from DDR0_1.8V and DDR1_1.8V
DDR0_1.8V and DDR1_1.8V respectively use the DDR0C and DDR1C channels of the LDO of the BD9571MWF-M. Their circuits consist of only capacitors used for smoothing.

Only the DDR_IN pin is used for the LDO power-supply input of the DDR0C and DDR1C. Supply the 5 V that is generated by the primary power supply to this pin and connect a smoothing capacitor (C1). Connect smoothing capacitors (C2 and C3) to the DDR0C and DDR1C output lines, respectively.
2.6.2 Peripheral Components

(1) Output section from DDR0_1.1V and DDR1_1.1V

Table 2.6.2.1 Components in the Output Section from DDR0_1.1V and DDR1_1.1V

<table>
<thead>
<tr>
<th>Part Name</th>
<th>Component</th>
<th>Qty</th>
<th>Parts</th>
<th>Value</th>
<th>Note</th>
</tr>
</thead>
<tbody>
<tr>
<td>L1, L2</td>
<td>Inductor</td>
<td>2</td>
<td>TFM201610ALMAR24MTAA#1</td>
<td>0.24 μH</td>
<td>Itemp = 6.2 A Isat = 6.5 A Rdc = 15 mΩ</td>
</tr>
<tr>
<td>C1, C7</td>
<td>Cin</td>
<td>2</td>
<td>Capacitor</td>
<td>1 μF</td>
<td>#2</td>
</tr>
<tr>
<td>C2, C3, C4, C5, C6, C8, C9, C10, C11, C12</td>
<td>Cout</td>
<td>10</td>
<td>Capacitor</td>
<td>4.7 μF</td>
<td>#3</td>
</tr>
<tr>
<td>R1, R3</td>
<td>FB resistor</td>
<td>2</td>
<td>Resistor</td>
<td>10 kΩ</td>
<td>#4</td>
</tr>
<tr>
<td>R2, R3</td>
<td>FB resistor</td>
<td>2</td>
<td>Resistor</td>
<td>15 kΩ</td>
<td>#4</td>
</tr>
</tbody>
</table>

Notes: 1. Value recommended by ROHM Co., Ltd.
2. The withstand voltage must be sufficient.
3. The number of capacitors and their capacitance depend on the use case and reductions may be possible.
4. The output voltage can be changed by adjusting the resistance (1.1 V for LPDDR4 and 1.35 V or 1.5 V for DDR3L or DDR3).

(2) Output section from DDR0_1.8V and DDR1_1.8V

Table 2.6.2.2 Components in the Output Section from DDR0_1.8V and DDR1_1.8V

<table>
<thead>
<tr>
<th>Part Name</th>
<th>Component</th>
<th>Qty</th>
<th>Part (or Parts)</th>
<th>Value</th>
<th>Note</th>
</tr>
</thead>
<tbody>
<tr>
<td>C1</td>
<td>Cin</td>
<td>1</td>
<td>Capacitor</td>
<td>1 μF</td>
<td>*</td>
</tr>
<tr>
<td>C2, C3</td>
<td>Cout</td>
<td>2</td>
<td>Capacitor</td>
<td>10 μF</td>
<td>*</td>
</tr>
</tbody>
</table>

Note: * The withstand voltage must be sufficient.
2.6.3 PCB Design

2.6.3.1 Example of SiP

Since the design policies for DDR0_1.1V and DDR1_1.1V are the same as those for the I/O power supplies (D1.8V and D3.3V), refer to section 2.5.3.1. Since the design policies for DDR0_1.8V and DDR1_1.8V are the same as those for the I/O power supplies (LDO output channels), refer to section 2.5.3.2.

The DDR0_1.1V and DDR1_1.1V power supplies and the DDR0_1.8V and DDR1_1.8V power supplies, which are DRAM power supplies, require independent and individual wiring patterns to prevent noise propagation between DRAM components and to implement the DRAM backup functions.

<Example of pattern design>
The design of the patterns for an evaluation board for the R-Car H3 SiP is taken as an example in this section and shown in the figure on the right as a six-layer board with plated through-holes.

In terms of wiring, the top and bottom layers are used as wiring layers, the layers adjacent to these, the L2 and L5 layers are used as GND layers, and the power-supply patterns are placed in the L3 and L4 layers which are adjacent to the GND layers. The main power-supply patterns around the BD9571MWF-M are placed in the top layer, and DDR0_1.1V and DDR1_1.1V are connected to the patterns in the L4 layer via through holes. DDR0_1.8V and DDR1_1.8V are similarly connected to the patterns in the L3 layer via through holes (via the L1 and L4 layers instead in regions where wiring is difficult).

Based on the maximum current of each power supply and considering the maximum current capacity, the widths of the wiring patterns and the numbers of via holes are as follows.

Note: In this example, a 1-mm trace width per 1 A is ensured under the condition of the copper wiring pattern being 35-μm thick.

- **DDR0_1.1V**
  - Width of the wiring patterns: 6.0 mm (at least 4 A is ensured)
  - Via holes: 0.6 mm × 13 (at least 4 A is ensured)
- **DDR1_1.1V**
  - Width of the wiring patterns: 4.0 mm (at least 4 A is ensured)
  - Via holes: 0.6 mm × 13 (at least 4 A is ensured)
- **DDR0_1.8V**
  - Width of the wiring patterns: 1.2 mm (at least 600 mA is ensured)
  - Via holes: 0.6 mm × 2 (at least 600 mA is ensured)
- **DDR1_1.8V**
  - Width of the wiring patterns: 1.2 mm (at least 600 mA is ensured)
  - Via holes: 0.6 mm × 2 (at least 600 mA is ensured)
The power-supply pins in the power-supply section containing the smoothing capacitors directly below the SiP are used as the starting points for the feedback signals. The wiring patterns for the feedback signals are placed in the bottom layer, on which the noise of the power supplies has little effect.

Figure 2.6.3.2  Layout of DDR0_1.1V, DDR1_1.1V, DDR0_1.8V, and DDR1_1.8V feedback (SiP)
2.6.3.2 Example of SoC

Since the design policies for wiring patterns from the output capacitors of the SoC to each device are the same as those for the SiP, refer to section 2.6.3.1.

<Example of pattern design>

The design of the patterns for an evaluation board for the R-Car M3 SoC is taken as an example in this section and shown in the figure on the right as an eight-layer board with plated through-holes. In terms of wiring, the top and bottom layers are used as wiring layers, the layers adjacent to these, the L2 and L7 layers are used as GND layers as reference, and the power-supply patterns are placed in the L4 and L5 layers which are adjacent to the GND layers. The main power-supply patterns around the BD9571MWF-M are placed in the top layer, and DDR0_1.1V and DDR1_1.1V are connected to the plane in the L4 layer while DDR0_1.8V and DDR1_1.8V are connected to the patterns in the L5 layer via through holes.

The policy regarding the widths of the wiring patterns and the numbers of via holes and their numerical values are the same as those in the example of design for the SiP.

The power-supply pins in the power-supply section containing the bypass capacitors directly below the SoC are used as monitoring points for the feedback signals. The wiring patterns that connect the monitoring points with the PMIC are placed in the bottom layer, on which the noise of the power supplies has little effect.

Figure 2.6.3.3 Layout of DDR0_1.1V, DDR1_1.1V, DDR0_1.8V, and DDR1_1.8V (SoC)
There are no changes in the design around the BD9571MWF-M for either the SiP or SoC.

The paths along which genuinely large currents are able to flow in the PMIC circuit are as follows.

Low -> High: Cin - PMIC - L - Cout - GND - Cin
High -> Low: GND - PMIC - L - Cout - GND

To suppress the generation of noise, components are placed and wiring patterns are designed to minimize the lengths of the above current loops.

For these power-supply paths, design the wiring patterns to be wide enough and place sufficient via holes along them.
2.7 Power-Supply Circuits for Peripheral Circuits
Refer to "R-Car Series, 3rd Generation Power-Supply Circuit Design Application Note".

2.8 Reset Circuit
This section consists of special notes on the reset signal of the BD9571MWF-M.

2.8.1 Specifications
The BD9571MWF-M keeps the reset signal at the low level until all power supplies are being output correctly and then de-asserts the reset signal. In addition to the power-on reset, the BD9571MWF-M includes a manual reset function where a reset signal can be generated by controlling the signal on the POFFB/MRB pin.

2.8.2 Circuit Configuration

![Reset Circuit (Example)](image)

The signal on the PRESETB pin is from an open-drain output, so it requires a pull-up resistor. The domain of PRESET# of the SoC is 1.8 V and so it has to be pulled up to D1.8V. When using the signal as a reset signal for other devices, design the reset circuit to suit the specifications of each device.

The manual reset function is controlled by the signal on the POFFB/MRB pin. In the example circuit, a physical switch is connected but this is not mandatory; design the circuit to suit your system. As the POFFB/MRB pin has an internal pull-down resistor, it need not be connected if the manual reset function is not to be used.

2.8.3 Peripheral Components

<table>
<thead>
<tr>
<th>Part Name</th>
<th>Component</th>
<th>Qty</th>
<th>Part</th>
<th>Value</th>
<th>Note</th>
</tr>
</thead>
<tbody>
<tr>
<td>R1</td>
<td>Pull-up resistor</td>
<td>1</td>
<td>Resistor</td>
<td></td>
<td>*</td>
</tr>
<tr>
<td>SW1</td>
<td>Manual reset</td>
<td>1</td>
<td></td>
<td>*</td>
<td></td>
</tr>
</tbody>
</table>

Note: * Design the circuit to suit the specifications of your system.
2.9 Power Supply Control Circuit

This section consists of special notes on the primary power supply block and BD9571MWF-M.

2.9.1 Specifications

Systems using this SoC require that the power-supply-related sequences between the primary power supply block and the BD9571MWF-M be observed. The BD9571MWF-M follows the sequences of turning the power supplies to the SoC on and off. However, the sequence for turning power off by the BD9571MWF-M does not proceed if the supply of power to the BD9571MWF-M itself is turned off. The sequence of turning the power supplies to the SoC off are not followed because all of the output power supplies are shut down at once. Therefore, control over the power-supply-related sequences of the primary power supply block and the BD9571MWF-M is required in terms of the following points.

- The BD9571MWF-M only outputs the power supplies after the primary power supplies have reached their output levels.
- The primary power supplies are only turned off after the other power supplies from the BD9571MWF-M have been turned off.

2.9.2 Circuit Configuration

No particular means or method for implementing the power-supply-related sequences of the primary power supply and the BD9571MWF-M is specified. Select a means or method that suits the specifications.

When the primary power-supply circuit consists of discrete components instead of an external controller, the sequences can be followed by incorporating the power supply that is to be shut off last by the BD9571MWF-M (this is DDR0_1.8V in the default state of the BD9571MWF-M) in the EN control section of the primary power supply block.

2.9.3 Peripheral Components

No particular means or method for implementing the power-supply-related sequences of the primary power supply and the BD9571MWF-M is specified. Select appropriate means or method that suits the specifications.

2.9.4 Calculating the Current from the Primary Power Supply

The specifications of the power-supply input (V5AIN) from the primary power supply to the BD9571MWF-M are defined in consideration of the power efficiency of the PMIC. Calculate the electric power necessary for the primary power supply by taking into account the power efficiency of the output side, $\eta$.

$$I_{\text{in}} = \frac{1}{\eta \cdot \text{Vin}} \left( V_{\text{out1}} \cdot I_{\text{out1}} + V_{\text{out2}} \cdot I_{\text{out2}} + V_{\text{out3}} \cdot I_{\text{out3}} + \ldots \right)$$

**Figure 2.9.4 Calculating the Current of the Primary Power Supply**
Related Documents

HDMI v1.4 Board Design Guideline
Design Guidelines for Serial Interface PCBs with Gen3
R-CarH3 SIP42p5sq PCB verification guide LPDDR4
R-CarH3 SIP42p5sq PCB verification guide Core
R-CarH3 FCBGA21p0sq PCB design_guide LPDDR4 10bu343 32x4
R-CarH3 FCBGA21p0sq PCB verification guide LPDDR4
R-CarH3 FCBGA21p0sq PCB verification guide Core v0p3
R-CarM3 FCBGA29p0sq PCB design_guide LPDDR4 8th 32x2
R-CarM3 FCBGA29p0sq PCB verification guide LPDDR4
R-CarM3 FCBGA29p0sq PCB verification guide Core LPDDR4
R-CarM3N FCBGA29p0sq PCB design_guide LPDDR4 8th 32x1
R-CarM3N FCBGA29p0sq PCB verification guide LPDDR4
R-CarM3N FCBGA29p0sq PCB design_guide DDR3 8th 16x2
R-CarM3N FCBGA29p0sq PCB verification guide DDR3
R-CarM3N FCBGA29p0sq PCB verification guide Core
R-CarH3N FCBGA29p0sq PCB design_guide LPDDR4 8th 32x2
R-CarH3N FCBGA29p0sq PCB verification guide LPDDR4
R-CarH3N FCBGA29p0sq PCB verification guide Core
## Revision History

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General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)
   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.

2. Processing at power-on
   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.

3. Input of signal during power-off state
   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.

4. Handling of unused pins
   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.

5. Clock signals
   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.

6. Voltage application waveform at input pin
   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between $V_{IL}$ (Max.) and $V_{IH}$ (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between $V_{IL}$ (Max.) and $V_{IH}$ (Min.).

7. Prohibition of access to reserved addresses
   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.

8. Differences between products
   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.
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