Application Note

Powering Xilinx Zynq with DA9061/2/3

AN-PM-087

Abstract

Xilinx® Zynq™ All-Programmable™ UltraScale+™ is complemented by the programmable architecture of Dialog power management ICs, providing the system developer with flexibility throughout the design cycle. This application note outlines how to determine the power requirements of a Zynq UltraScale+ MPSoC-based system and select a suitable PMIC from the Dialog DA9061, DA9062, and DA9063 family.

Contents

1 Terms and Definitions

ADAS	Advanced Driver Assistance Systems
GUI	Graphical User Interface
PMIC	Power Management Integrated Circuit
DA906x	Dialog DA9061, DA9062, DA9063, and DA9063L.
DVC	Dynamic Voltage Control
DVS	Dynamic Voltage Scaling. Analogous to DVC.
MPSoC	Multiprocessor System-on-Chip
OTP	One-Time Programmable (memory)
RTC	Real-Time Clock
SoC	System-on-Chip

2 References

[1] Xilinx Power Estimator (XPE), http://www.xilinx.com/products/technology/power/xpe.html [Accessed 4th Oct 2016]

[2] Philofsky, B., 'Seven Steps to an Accurate Worst-Case Power Analysis Using Xilinx Power Estimator (XPE)', WP353, v1.0, Xilinx Inc., 2008.

[3] DA9061, Datasheet, Dialog Semiconductor

[4] DA9062, Datasheet, Dialog Semiconductor

[5] DA9063, Datasheet, Dialog Semiconductor

[6] DA9063L, Datasheet, Dialog Semiconductor

[7] AN-PM-080, 'In-Circuit Programming of DA9061/2/3', Dialog Semiconductor, 2016

[8] UM-PM-008, SmartCanvas™ DA9061/2 User Manual, Dialog Semiconductor

3 Introduction

The Xilinx Zynq All-Programmable UltraScale+ MPSoC portfolio integrates the flexibility of software and hardware programmability of an FPGA. The Zynq processors are therefore ideally complemented by the software-configurable and programmable power management solution provided by the advanced architecture of Dialog PMICs.

The UltraSCale+ MPSoC processors require dedicated power management for a stable and reliable system. However, system power consumptions vary greatly due to the differing demands of the SoC and non-integrated peripherals. This application note outlines how to calculate the power demands of a Zynq system which then enables selection of a suitable system PMIC from the Dialog DA906x family. The features of the DA906x family enable significant power saving, such as Dynamic Voltage Control (DVC) which intelligently manages voltage changes. Section 4 describes the procedure, followed by examples in Section

4 Creating a Power Management Solution

A key point of this application note is that the choice of power management solution can only be determined after the power requirements of a system have been estimated. With FPGA-based processors, the power requirements may vary greatly. This means it is not possible for PMIC suppliers to provide a single power management reference design for these systems. Therefore the following procedure is recommended:

1. Calculate the system power requirements contributed by:
   a. the Zynq MPSoC
   b. other peripherals
2. Map the power requirements to the PMIC capabilities.

4.1 Calculate the Processor Power Requirements

The Zynq power requirements can be estimated using the ‘Xilinx Power Estimator’ (XPE). The XPE tool is available for download from the Xilinx website [1]. For the purposes of defining PMIC requirements, a worst-case analysis should be performed by setting the ‘Process’ variable to ‘maximum’. See the Xilinx application note [2] for further details.

The worst-case load currents should then be calculated for those peripherals not integrated into the SoC.

For each supply rail, the worst-case load current should be noted.

4.2 Map the Power Requirements to the PMIC Capabilities

The next step is to map the load currents onto PMIC supply rails. A worksheet to assist with this step is presented in Table 1. One or more products may be chosen from the DA906x family, listed below in order of increasing capability:

1. DA9061 PMIC supplying up to 6 A
2. DA9062 PMIC supplying up to 8.5 A
3. DA9063L High power PMIC supplying up to 13 A
4. DA9063 High power PMIC supplying up to 14 A

Several of the above system PMICs can be used together as a master system PMIC and slave, or can be supplemented by one or more of the following sub-PMICs:

1. DA9210 12 A buck with programmable control
2. DA9211 Multiphase 12 A buck with programmable control
3. DA9212 Multiphase 2 x 6 A bucks with programmable control
4. DA9213 Multiphase 20 A buck with programmable control
5. DA9214 Multiphase 2 x 10 A bucks with programmable control
6. DA9215 Multiphase 15 A and 5 A bucks with programmable control

The DA9062 is pin-compatible with the DA9061 and provides additional features often required by systems such as a real-time clock (RTC), a dual-phase (5 A) buck configuration, DDR memory termination (DA9062 VTT supply), and VTTR memory reference voltage.

Where current monitoring is required but not performed by a Zynq System Controller, the ADC and rail monitoring integrated into the DA9063 and DA9063L can be used.

Spare bucks can be used as part of the programmable logic (PL) solution, to drive additional peripherals, or to drive LDO VDDs which can improve system efficiency.

Dialog sub-PMICs are designed to operate as slaves to the system PMIC, with integrated control. Configuration of the system is no more complex than when a system PMIC is used alone. This also applies when two system PMICs are used together. If one or more discrete regulators are required to supplement the capabilities of the Dialog PMICs, then these can often be incorporated into the programmable start-up and shutdown sequences within the Dialog system PMIC by using the general purpose outputs (GPOs) which can be sequenced.

Table 1: Example Worksheet for Mapping System Power to PMIC Options (ZU9EG - Processing System (PS) only)

Zynq System Supply Name	Voltage (V)	Load (from XPE calculation) (A)	Mapping Option A (PMIC#[regulators])	Mapping Option B (PMIC[regulators])	Mapping Option C (PMIC[regulators])
VCC_PSINTFP + VCC_PSINTFP_DDR	0.85	4.70	DA9062_#1[Buck1+Buck2]	DA9062[Buck1+Buck2]	DA9063[BUCKCORE1+BUCKCORE2]
VCCDDR4	1.2	2.00	DA9062_#2[Buck 1]	DA9061[Buck2]	DA9063[BUCKPRO]
VCCO_DDR	1.1/1.2/1.35/1.5	1.80	DA9062_#1[Buck3]	DA9061[Buck1]	DA9063[BUCKMEM+BUCKIO]
VCC_PSINTLP	0.85	1.50	DA9062_#1[Buck 4]	DA9062[Buck3]	DA9063[BUCKPERI]
VCC_PSIO[0-2]	1.8/2.5/3.3	0.35	DA9062_#1[LDO1+LDO2]	DA9062[LDO1+LDO2]	DA9063[LDO3+LDO4]
VCC_PSIO[n]	1.8/2.5/3.3	0.10	DA9062_#2[LDO1]	DA9061[LDO1]	DA9063[LDO5]
VPS_MGTRAVCC	0.85	0.30	DA9062_#2[Buck 4]	DA9062[Buck4]	DA9063[LDO1+LDO2]
VCCAUX	1.8	0.2	DA9062_#1[LDO3]	DA9062[LDO3]	DA9063[LDO10]
VCC_PSDDR_PLL	1.8	0.20	DA9062_#1[LDO4]	DA9062[LDO4]	DA9063[LDO6]
VCC_PSPLL	1.2	0.07	DA9062_#2[LDO2]	DA9061[LDO2]	DA9063[LDO7]
VMGTRAVTT	1.8	0.03	DA9062_#2[LDO3]	DA9061[LDO3]	DA9063[LDO8]
spare			DA9062_#2[Buck 2]	DA9061[Buck3]	DA9063[LDO9]
spare			DA9062_#2[Buck 3]	DA9061[LDO4]	DA9063[LDO11]
spare			DA9062_#2[LDO4]		

4.3 Power-up Sequence

The sequence described in the Xilinx datasheets is readily programmed into the DA906x PMICs using Dialog's SmartCanvas™ GUI, see Appendix A. Sequencing of a slave PMIC or sub-PMICs can be included in the same sequence. The completed sequence is saved with other configuration settings into an ini file. After testing the configuration using the SmartCanvas™ Power Commander Mode, the ini file can then be used to program the PMIC OTP memory.

4.4 OTP Programming

Various options are available for OTP programming. The most suitable option depends on the number of devices, see Table 2. Details of the evaluation kits are available on the Dialog website and can be ordered via distributors.

Table 2: OTP Programming Options

Programming Method	Suitability	Volume (units)	Comments
Evaluation kit	Development of PMIC configuration using SmartCanvas software (Note 1) and 'Power Commander Mode'	1	Avoids the need to program the OTP. See the SmartCanvas user manual [8]
	Prototype builds or bespoke small volume manufacture	≤ 30	Evaluation kit and 'socket board' (Note 2)
In-circuit programming	Volume manufacturing	< 30k	See AN-PM-080 [7]
Dialog custom variant	High volume manufacturing	> 30k	Usually supplied directly from Dialog as a custom OTP variant.
Dialog standard variants	Platform-specific	≥ 1	Supplied with OTP programmed for specific platforms such as NXP i.MX 5 / 6, Atmel SAMA5, Renesas R-Car.

Note 1 SmartCanvas is the GUI software included with the Dialog PMIC Evaluation Kits. The software can be downloaded separately from the Dialog Support website.

Note 2 Sockets boards are 'DA9063-EVAL6', ' DA9061-SOCKETBOARD' and 'DA9062-SOCKETBOARD'

5 Power Solution Examples

The above procedure was used to create solutions for the following Xilinx processors.

5.1 ZU3EG

The following mapping was optimized for industrial networking applications.

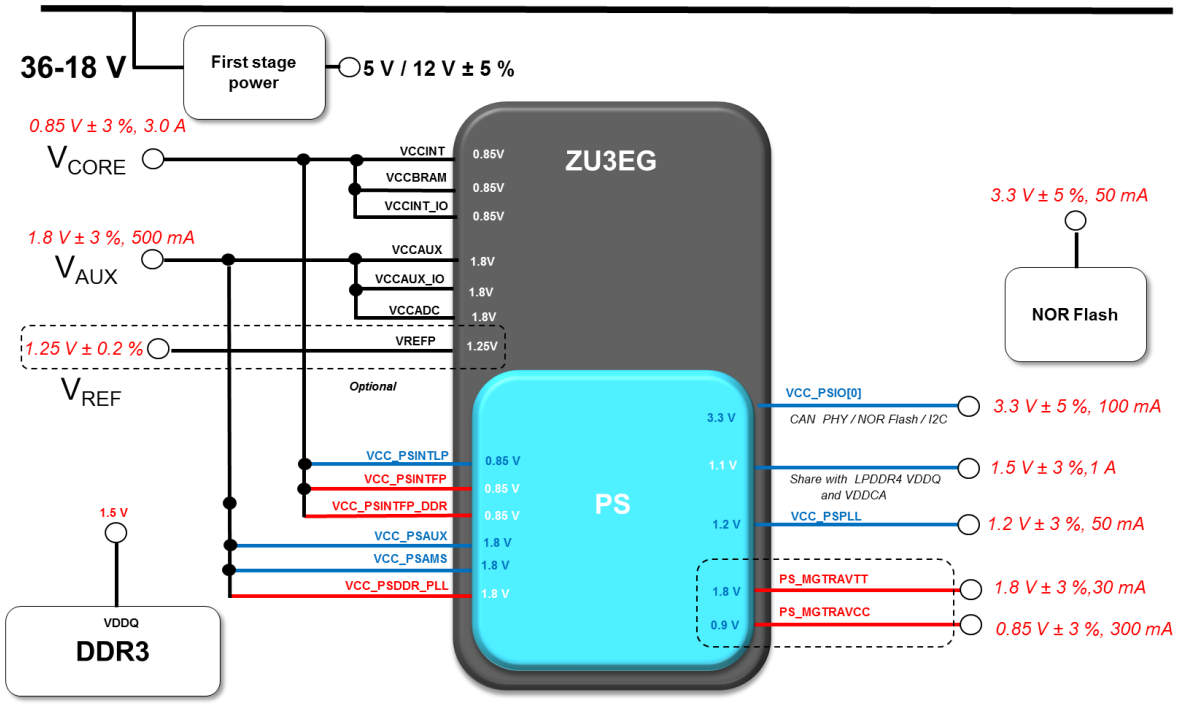

Figure 1. ZU3EG Supply Requirements

Table 3: DA9062 Mapping to ZU3EG (12 V to 5 V Input Regulator Not Shown)

Supply Rail	Voltage (V)	Load (A)	Regulator	Max Load (A)	DA9062 Power-up Sequence
V_{CORE}	0.8	3.0	Buck1 + Buck2	5.0	1
V_{AUX}	1.8	0.5	Buck4	1.5	2
VCC_PSPLL	1.2	0.05	LDO1	0.1	3
VCCO_PSDDR	1.5	1.0	Buck3	2.0	
VCC_PSIO[0]	3.3	0.2	LDO4	0.3	4
PS_MGTRAVTT	1.8	0.1	LDO2	0.3	
PSMGTRAVCC	0.85	0.3	LDO3	0.3	

5.2 ZU7EV

The following mapping was optimized for automotive ADAS applications.

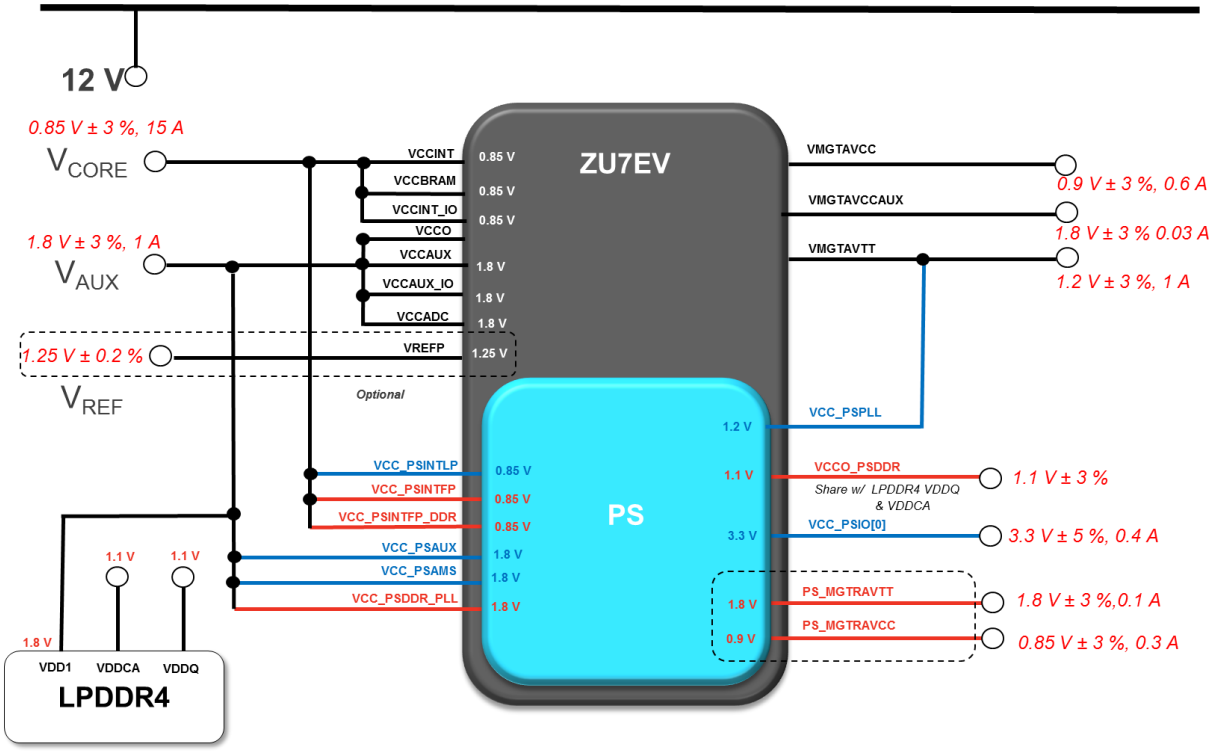

Figure 2. ZU7EV Supply Requirements

Table 4: DA9062 and DA9213 Mapping to ZU7EV (12 V to 5 V Input Regulator Not Shown)

Supply Rail	Voltage (V)	Load (A)		Device	Regulator	Max Load (A)	Power-up Sequence
V_{CORE}	0.85	15		DA9213		20	1
V_{AUX}	1.8	1		DA9062	Buck4	1.5	2
VMGTAVCC	0.9	0.6			Buck1	2.5	1
VMGTAVCCAUX	1.8	0.03			LDO2	0.3	
VMGTAVTT	1.2	1			Buck3	2.0	3
VCCO_PSDDR	1.1	TBA			Buck2	2.5	
VCC_PSIO[0]	3.3	0.4			LDO1 + LDO4	0.4	4
PS_MGTRAVTT	1.8	0.1			LDO2	0.3	
PSMGTRAVCC	0.85	0.3			LDO3	0.3	
VDDCA	1.1				Buck2	2.5	
VDDQ	1.1				Buck2	2.5	

5.3 ZU9CG

Mapping of the DA9063 system PMIC with DA9213 sub-PMIC is shown in Figure 3. The configuration for this mapping is given by Table 5. The designator 'User' means these are spare regulators that can be configured by the system developer.

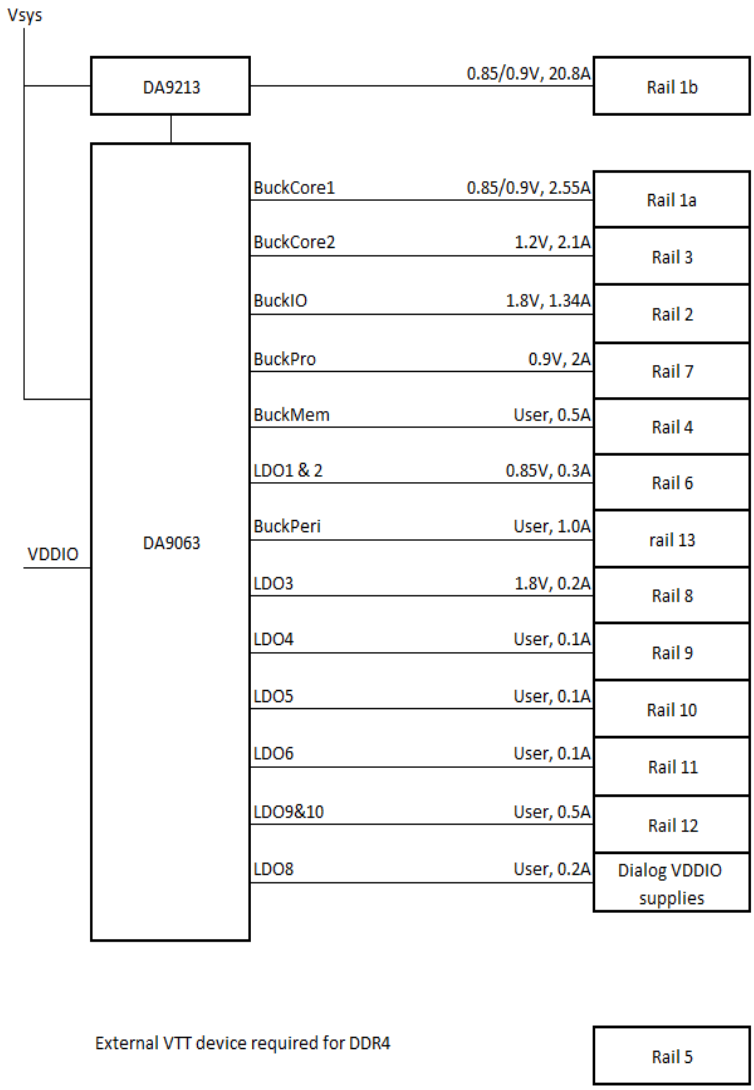

Figure 3. System Rail Mapping of DA9063 and DA9213 to ZU9CG

Table 5: DA9063 and DA9213 Mapping to ZU9CG (12 V to 5 V Input and DDR4 Regulators are Not Shown)

System Rail	ZU9CG Rail	Voltage (V)	ZU9CG Rail Load (A)	Total Load (A)
Rail 1a	VCC_PSINTFP	0.85/0.9	1.4	2.55
	VCC_PSINTLP	0.85/0.9	0.4	
	VCC_PSINTFP_DDR	0.85/0.9	0.75	
	VCCINT_VCU	0.85/0.9	-	
Rail 1b	VCCINT	0.85/0.9	20	20.8
	VCCINT_IO	0.85/0.9	0.2	
	VCCBRAM	0.85/0.9	0.6	
Rail 2	VCC_PSAUX	1.8	0.1	1.34
	VCC_PSDDR_PLL	1.8	0.1	
	VCC_PSADC	1.8	0.02	
	VCCAUX	1.8	0.9	
	VCCAUX_IO	1.8	0.2	
	VCCADC	1.8	0.02	
	DDR_VPP1	USER		
Rail 3	VMGTAVTT	1.2	2	2.1
	VMGTYAVTT	1.2	-	
	VCC_PSPLL	1.2	0.1	
	VCC_VCU_PLL	1.2	-	
	VCCO_PSDDR	USER	0.5	0.5
	DDR_VDD2	USER		
	DDR_VDDQ	USER		
Rail 5	DDR_VTT	USER		0
	DDR_VREF	USER		
Rail 6	VPS_MGTRAVCC	0.85	0.3	0.3
Rail 7	VMGTAVCC	0.9	2	2
	VMGTYAVCC	0.9	-	
Rail 8	VMGTVCCAUX	1.8	0.1	0.2
	VMGTYVCCAUX	1.8	-	
	VPS_MGTRAVTT	1.8	0.1	
Rail 9	VCCO_PSIO[0]	USER	0.1	0.1
Rail 10	VCCO_PSIO[1]	USER	0.1	0.1
Rail 11	VCCO_PSIO[2]	USER	0.1	0.1
Rail 12	HDIO VCCO	USER	0.5	0.5
Rail 13	HPIO VCCO	USER	1	1
	VCC_PSBATT	0	-	

6 Conclusions

The flexibility and programmability of Dialog PMICs make them an ideal partner to the Xilinx Zynq All-Programmable SoCs. System power requirements can be calculated using the Xilinx Power Estimator (XPE) tool from which a regulator mapping can be made to Dialog PMIC(s).

Appendix A SmartCanvas Software Overview

SmartCanvas is included in the Dialog DA906x evaluation kits and is the GUI used with the kit evaluation board. The GUI provides a visual representation of the device registers and of the PMIC operation state. The software (Figure 4) allows interaction with the PMIC, and can be used to read or write to device registers, for testing prototype configurations and to program socketed devices. The user manual [8] is accessible via the GUI 'Help' menu and is also available from the Dialog support site.

Power Commander Mode ('PC Mode') is a powerful feature of Dialog PMICs that allows prototyping of OTP configurations without having to burn a device's OTP. PC Mode starts a device using the configuration from an external ini file instead of the device's own programmed (or blank) configuration. These ini files are compatible with the In-Circuit Programmer and gang programmer, and therefore the same ini files can be used to program parts for volume manufacturing.

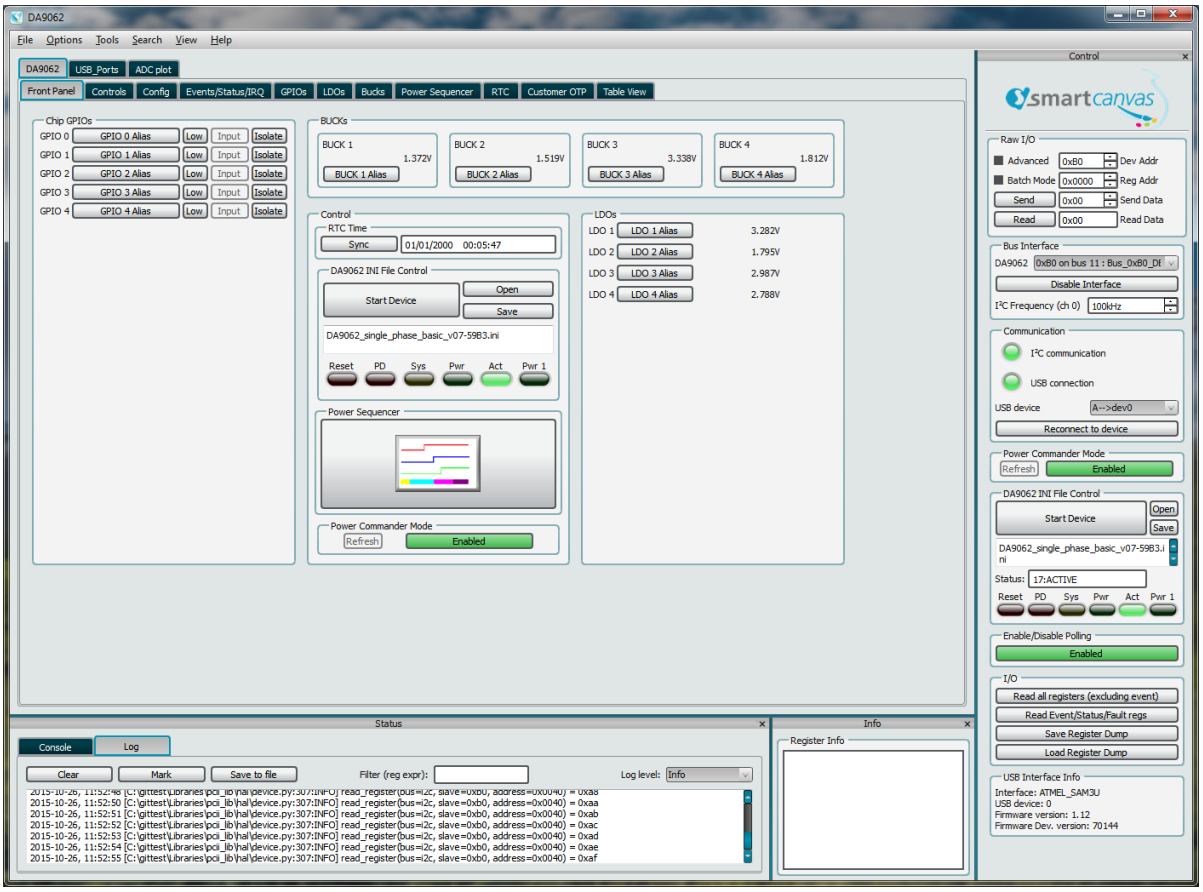

Figure 4: SmartCanvas Front Panel

Revision History

Revision	Date	Description
2.2	25-Feb-2022	File was rebranded with new logo, copyright and disclaimer
2.1	06-Feb-2017	Reviewer minor comments addressed
2.0	09-Jan-2017	Added section on Power Solution Examples
1.0	15-Nov-2016	Initial version.

Status Definitions

Status	Definition
DRAFT	The content of this document is under review and subject to formal approval, which may result in modifications or additions.
APPROVED or unmarked	The content of this document has been approved for publication.

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