Application Note

DA16200 Registers Map for Peripherals

AN-WI-011

Abstract

This document provides information about registers for various peripherals in DA16200

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1 Terms and Definitions

GPIO	General-Purpose Input/Output
I2S	Integrated Interchip Sound
SdeMMC	Secure Digital embedded MultiMedia Card
I2C	Inter Integrated Circuit
SPI	Serial Peripheral Interconnect
RTC	Real Time Clock
GPIOA	GPIO A group
GPIOB	GPIO B group
PWM	Pulse Width Modulation
RF	Radio Frequency
UART	Universal Asynchronous Receiver/Transmitter
HW	Hardware
FIFO	First In First Out
CTS	Clear to Send
DMA	Direct Memory Access
PLL	Phase Lock Loop
FNPLL	Fractional N PLL
AHB	Advanced High-performance Bus
CMD/RSP	Command/Response
CRC	Cyclic Redundancy Check
CSB	Chip Select Bit
IRQ	Interrupt Request

2 References

[1] UM-WI-002, DA16200 SDK Programmer's Guide, Dialog Semiconductor

[2] DA16200 Datasheet, Dialog Semiconductor

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3 Introduction

This document describes the registers for various peripherals in DA16200, such as GPIO, I2S, SDeMMC, I2C, SPI and RTC.

4 Register Map

4.1 GPIO Register

There are 15 GPIOs in DA16200. GPIOA[11:0] and GPIOC[8:6].

The GPIO features for this device are as follows:

- Input or output lines in a programmable direction
- Word and half word read/write access
- Address-masked byte writes to facilitate quick bit set and clear operations
- Address-based byte reads to facilitate quick bit test operations
- To make a GPIO pin an interrupt pin
- Possible to be output signal of PWM [3:0], external Interrupt, SPI_CSB [3:1], RF_SW [1:0] and UART_TXDOE [1:0] on any GPIO pin

Table 1: GPIO Registers Overview

Address	Register	Description
Common control for GPIO Pin Status		
0x5000_1208	FSEL_GPIO1	Function Selection of the GPIOA [14:0]
0x5000_120C	FSEL_GPIO2	Function Selection of the GPIOB [11:0] and GPIOC [8:0]
0x5000_1220	GPIO_DS	Driving Strength for GPIOA [14:0]
0x5000_1224	GPIO_SR	Slew Rate Control for GPIOA [14:0]
0x5000_1228	GPIO_PE_PS	Pull-up/Pull-down Control for GPIOA [14:0]
0x5000_122C	GPIO_IE_IS	Input enable/CMOS Control for GPIOA [14:0]
0x5000_1234	GPIO1_DS	Driving Strength for GPIOB [11:0]
0x5000_1238	GPIO1_SR	Slew Rate Control for GPIOB [11:0]
0x5000_123C	GPIO1_PE_PS	Pull-up/Pull-down Control for GPIOB [11:0]
0x5000_1240	GPIO1_IE_IS	Input enable/CMOS Control for GPIOB [11:0]
0x5000_1244	GPIO2_DS	Driving Strength for GPIOC [8:0]
0x5000_1248	GPIO2_SR	Slew Rate Control for GPIOC [8:0]
0x5000_124C	GPIO2_PE_PS	Pull-up/Pull-down Control for GPIOC [8:0]
0x5000_1250	GPIO2_IE_IS	Input enable/CMOS Control for GPIOC [8:0]
GPIO In/Out control		
0x4001_0000	DataIn0	GPIOA Input value
0x4001_0004	DataOut0	GPIOA Output value
0x4001_0008		reserved
0x4001_000C		reserved
0x4001_0010	DataOut_Set0	GPIOA Data output enable set
0x4001_0014	DataOut_Clr0	GPIOA Data output clear

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Address	Register	Description
0x4001_0018	AltFunc_Set0	GPIOA Alternate Function output enable set
0x4001_001C	AltFunc_Clr0	GPIOA Alternate Function output clear
0x4001_0020	IntrEn_Set0	GPIOA Interrupt set
0x4001_0024	IntrEn_Clr0	GPIOA Interrupt clear
0x4001_0028	IntrType_Set0	
0x4001_002C	IntrType_Clr0	
0x4001_0030	IntrPol_Set0	
0x4001_0034	IntrPol_Clr0	
0x4001_0038	IntrStatus0	
0x4001_003C	Func_Out_En0	Alternate Function output enable for GPIOA
0x4001_0FC0	PWM_OutSel0	PWM_OUT[3:0] port selection for GPIOA
0x4001_0FC4	mSPI_CS_OutSel0	mSPI_CSB[3:1] and Ext_Intr port selection for GPIOA
0x4001_0FC8	RF_SW_OutSel0	RF_SW[2:1] port selection for GPIOA
0x4001_0FCC	UART_OutSel0	UART_TXDOE[3:0] port selection for GPIOA
0x4001_1000	DataIn1	GPIOB Input value
0x4001_1004	DataOut1	GPIOB Output value
0x4001_1008		reserved
0x4001_100C		reserved
0x4001_1010	DataOut_Set1	GPIOB Data output enable set
0x4001_1014	DataOut_Clr1	GPIOB Data output clear
0x4001_1018	AltFunc_Set1	GPIOB Alternate Function output enable set
0x4001_101C	AltFunc_Clr1	GPIOB Alternate Function output clear
0x4001_1020	IntrEn_Set1	GPIOB Interrupt set
0x4001_1024	IntrEn_Clr1	GPIOB Interrupt clear
0x4001_1028	IntrType_Set1	
0x4001_102C	IntrType_Clr1	
0x4001_1030	IntrPol_Set1	
0x4001_1034	IntrPol_Clr1	
0x4001_1038	IntrStatus1	
0x4001_103C	Func_Out_En1	Alternate Function output enable for GPIOB
0x4001_1FC0	PWM_OutSel1	PWM_OUT[3:0] port selection for GPIOB
0x4001_1FC4	mSPI_CS_OutSel1	mSPI_CSB[3:1] and Ext_Intr port selection for GPIOB
0x4001_1FC8	RF_SW_OutSel1	RF_SW[2:1] port selection for GPIOB
0x4001_1FCC	UART_OutSel1	UART_TXDOE[3:0] port selection for GPIOB
0x4001_7000	DataIn2	GPIOC Input value
0x4001_7004	DataOut2	GPIOC Output value
0x4001_7008		reserved

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Address	Register	Description
0x4001_700C		reserved
0x4001_7010	DataOut_Set2	GPIOC Data output enable set
0x4001_7014	DataOut_Clr2	GPIOC Data output clear
0x4001_7018	AltFunc_Set2	GPIOC Alternate Function output enable set
0x4001_701C	AltFunc_Clr2	GPIOC Alternate Function output clear
0x4001_7020	IntrEn_Set2	GPIOC Interrupt set
0x4001_7024	IntrEn_Clr2	GPIOC Interrupt clear
0x4001_7028	IntrType_Set2	
0x4001_702C	IntrType_Clr2	
0x4001_7030	IntrPol_Set2	
0x4001_7034	IntrPol_Clr2	
0x4001_7038	IntrStatus2	
0x4001_703C	Func_Out_En2	Alternate Function output enable for GPIOC
0x4001_7FC0	PWM_OutSel2	PWM_OUT[3:0] port selection for GPIOC
0x4001_7FC4	mSPI_CS_OutSel2	mSPI_CSB[3:1] and Ext_Intr port selection for GPIOC
0x4001_7FC8	RF_SW_OutSel2	RF_SW[2:1] port selection for GPIOC
0x4001_7FCC	UART_OutSel2	UART_TXDOE[3:0] port selection for GPIOC

Table 2: FSEL_GPIO1 (0x5000_1208)

Bit	Mode	Symbol	Description	Reset
31:30	R/W		Pin function selection for GPIOA[15]	0x3F61_1389
29:28			Pin function selection for GPIOA[14]	
27:26			Pin function selection for GPIOA[13]	
25:24			Pin function selection for GPIOA[12]	
22:20			Pin function selection for GPIOA[11:10]	
19:16			Pin function selection for GPIOA[9:8]	
15:12			Pin function selection for GPIOA[7:6]	
11:8			Pin function selection for GPIOA[5:4]	
7:4			Pin function selection for GPIOA[3:2]	
3:0			Pin function selection for GPIOA[1:0]	

* See Figure 2

Table 3: FSEL_GPIO2 (0x5000_120C)

Bit	Mode	Symbol	Description	Reset
21:20	R/W	-	Pin function selection for GPIOC[8:6]	0x002E_AA00
19:18			Pin function selection for GPIOC[5:4]	
17:16			Pin function selection for GPIOC[3:2]	
15:14			Pin function selection for GPIOC[1:0]	
13:12			Pin function selection for GPIOB[11:8]	
11:10			Pin function selection for GPIOB[7:4]	

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Bit	Mode	Symbol	Description	Reset
9:8			Pin function selection for GPIOB[3:0]	
6:4			Pin function selection for GPIOC[14:13]	
3:0			Pin function selection for GPIOC[12:9]	

* See Figure 2

Table 4: GPIO_DS (0x5000_1220)

Bit	Mode	Symbol	Description	Reset
29:0	R/W		Driving Strength 00: 2 mA 01:8 mA (default) 10: 4 mA 11:12 mA [29:28] GPIOA14 [27:26] GPIOA13 [25:24] GPIOA12 [23:22] GPIOA11 [21:20] GPIOA10 [19:18] GPIOA9 [17:16] GPIOA8 [15:14] GPIOA7 [13:12] GPIOA6 [11:10] GPIOA5 [9:8] GPIOA4 [7:6] GPIOA3 [5:4] GPIOA2 [3:2] GPIOA1 [1:0] GPIOA0	0x5555_5555

Table 5: GPIO_SR (0x5000_1224)

Bit	Mode	Symbol	Description	Reset
14:0	R/W	-	Slew Rate control, Default = 0 (fast slew) [14] GPIOA14 [13] GPIOA13 … [1] GPIOA1 [0] GPIOA0	0x0000

Table 6: GPIO_PE_PS (0x5000_1228)

Bit	Mode	Symbol	Description	Reset
31:16	R/W	-	Pull-Up/Pull-Down Enable (active high) [14] GPIOA14 [13] GPIOA13 … [1] GPIOA1 [0] GPIOA0	0xFFFF
15:0	R/W	-	Pull Selection, Pull-Up = 1	0x0000

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Bit	Mode	Symbol	Description	Reset
			Pull-Down =0 [14] GPIOA14 [13] GPIOA13 … [1] GPIOA1 [0] GPIOA0	

Table 7: GPIO_IE_IS (0x5000_122C)

Bit	Mode	Symbol	Description	Reset
31:16	R/W	-	Input Enable (active high, default = 1) [30] GPIOA14 [29] GPIOA13 … [17] GPIOA1 [16] GPIOA0	0x7FFF
15:0	R/W	-	Input Selection: 0 CMOS, 1: Schmitt (default = 1) [14] GPIOA14 [13] GPIOA13 … [1] GPIOA1 [0] GPIOA0	0x7FFF

Table 8: GPIO1_DS (0x5000_1234)

Bit	Mode	Symbol	Description	Reset
23:0	R/W		Driving Strength 00: 2 mA 01:8 mA (default) 10: 4 mA 11:12 mA [23:22] GPIOB11 [21:20] GPIOB10 [19:18] GPIOB9 [17:16] GPIOB8 [15:14] GPIOB7 [13:12] GPIOB6 [11:10] GPIOB5 [9:8] GPIOB4 [7:6] GPIOB3 [5:4] GPIOB2 [3:2] GPIOB1 [1:0] GPIOB0	0x0055_5555

Table 9: GPIO1_SR (0x5000_1238)

Bit	Mode	Symbol	Description	Reset
11:0	R/W	-	Slew Rate control, Default = 0 (fast slew) [11] GPIOB11	0x0000

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Bit	Mode	Symbol	Description	Reset
			[10] GPIOB10 … [1] GPIOB1 [0] GPIOB0	

Table 10: GPIO1_PE_PS (0x5000_123C)

Bit	Mode	Symbol	Description	Reset
27:16	R/W	-	Pull-Up/Pull-Down Enable (active high) [27] GPIOB11 [26] GPIOB10 … [17] GPIOB1 [16] GPIOB0	0x0FFF
11:0	R/W	-	Pull Selection, Pull-Up = 1, Pull-Down =0 [11] GPIOB11 [10] GPIOB10 … [1] GPIOB1 [0] GPIOB0	0x0000

Table 11: GPIO1_IE_IS (0x5000_1240)

Bit	Mode	Symbol	Description	Reset
27:16	R/W	-	Input Enable (active high, default = 1) [27] GPIOB11 [26] GPIOB10 … [17] GPIOB1 [16] GPIOB0	0x0FFF
11:0	R/W	-	Input Selection: 0 CMOS 1: Schmitt (default = 1) [11] GPIOB11 [10] GPIOB10 … [1] GPIOB1 [0] GPIOB0	0x0FFF

Table 12: GPIO2_DS (0x5000_1244)

Bit	Mode	Symbol	Description	Reset
17:0	R/W		Driving Strength 00: 2 mA 01:8 mA (default) 10: 4 mA 11:12 mA [17:16] GPIOC8 [15:14] GPIOC7 [13:12] GPIOC6	0x0001_5555

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Bit	Mode	Symbol	Description	Reset
			[11:10] GPIOC5 [9:8] GPIOC4 [7:6] GPIOC3 [5:4] GPIOC2 [3:2] GPIOC1 [1:0] GPIOC0	

Table 13: GPIO2_SR (0x5000_1248)

Bit	Mode	Symbol	Description	Reset
8:0	R/W	-	Slew Rate control, Default = 0 (fast slew) [8] GPIOC8 [7] GPIOC7 … [1] GPIOC1 [0] GPIOC0	0x0000

Table 14: GPIO2_PE_PS (0x5000_124C)

Bit	Mode	Symbol	Description	Reset
24:16	R/W	-	Pull-Up/Down Enable (active high) [24] GPIOC8 [23] GPIOC7 … [17] GPIOC1 [16] GPIOC0	0x01FF
8:0	R/W	-	Pull Selection, Pull-Up = 1, Pull-Down =0 [8] GPIOC8 [7] GPIOC7 … [1] GPIOC1 [0] GPIOC0	0x0000

Table 15: GPIO2_IE_IS (0x5000_1250)

Bit	Mode	Symbol	Description	Reset
24:16	R/W	-	Input Enable (active high, default = 1) [24] GPIOC8 [23] GPIOC7 … [17] GPIOC1 [16] GPIOC0	0x01FF
8:0	R/W	-	Input Selection: 0 CMOS 1: Schmitt (default = 1) [8] GPIOC8 [7] GPIOC7 … [1] GPIOB1 [0] GPIOB0	0x01FF

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Table 16: DataIn0 (0x4001_0000)

Bit	Mode	Symbol	Description	Reset
15:0	R	-	GPIOA Input Data	0x0000

Table 17: DataOut0 (0x4001_0004)

Bit	Mode	Symbol	Description	Reset
15:0	R/W	-	GPIOA Output Data	0x0000

Table 18: DataOut_Set0 (0x4001_0010)

Bit	Mode	Symbol	Description	Reset
15:0	R/W	-	GPIOA Data Output Enable set 1 = Output enable 0 = Input enable	0x0000

Table 19: DataOut_Clr0 (0x4001_0014)

Bit	Mode	Symbol	Description	Reset
15:0	R/W	-	GPIOA Data Output clear 1 = Output clear	0x0000

Table 20: AltFunc_Set0 (0x4001_0018)

Bit	Mode	Symbol	Description	Reset
15:0	R/W	-	GPIOA Alternate Function Output enable set 1 = Output enable 0 = disable	0x0000

Table 21: AltFunc_Clr0 (0x4001_001C)

Bit	Mode	Symbol	Description	Reset
15:0	R/W	-	GPIOA Alternate Function Output clear 1 = Output clear	0x0000

Table 22: IntrEn_Set0 (0x4001_0020)

Bit	Mode	Symbol	Description	Reset
15:0	R/W	-	GPIOA Interrupt set 1 = Interrupt enable 0 = disable	0x0000

Table 23: IntrEn_Clr0 (0x4001_0024)

Bit	Mode	Symbol	Description	Reset
15:0	R/W	-	GPIOA Interrupt clear 1 = Interrupt clear	0x0000

Table 24: IntrType_Set0 (0x4001_0028)

Bit	Mode	Symbol	Description	Reset
15:0	R/W	-		0x0000

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Table 25: IntrType_Clr0 (0x4001_002C)

Bit	Mode	Symbol	Description	Reset
15:0	R/W	-		0x0000

Table 26: IntrPol_Set0 (0x4001_0030)

Bit	Mode	Symbol	Description	Reset
15:0	R/W	-		0x0000

Table 27: IntrPol_Clr0 (0x4001_0034)

Bit	Mode	Symbol	Description	Reset
15:0	R/W	-		0x0000

Table 28: IntrStatus0 (0x4001_0038)

Bit	Mode	Symbol	Description	Reset
15:0	R/W	-		0x0000

Table 29: Func_Out_En0 (0x4001_003C)

Bit	Mode	Symbol	Description	Reset
12:0	R/W	-	Alternate Function Output Enable for GPIOA 1 = enable 0 = disable [12]: UART2_TXDOE enable [11]: UART1_TXDOE enable [10]: UART0_TXDOE enable [9]: RF_SW2 enable [8]: RF_SW1 enable [7]: mSPI_CSB[3] enable [6]: mSPI_CSB[2] enable [5]: mSPI_CSB[1] enable [4]: Ext_Intr enable [3]: PWM_OUT[3] enable [2]: PWM_OUT[2] enable [1]: PWM_OUT[1] enable [0]: PWM_OUT[0] enable	0x0000

Table 30: PWM_OutSel0 (0x4001_0FC0)

Bit	Mode	Symbol	Description	Reset
15:0	R/W	-	PWM_OUT[3:0] port selection for GPIOA [15:12]: port selection of the PWM_OUT[3] [11: 8]: port selection of the PWM_OUT[2] [7: 4]: port selection of the PWM_OUT[1] [3: 0]: port selection of the PWM_OUT[0]	0x0000

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Table 31: mSPI_CS_OutSel0 (0x4001_0FC4)

Bit	Mode	Symbol	Description	Reset
15:0	R/W	-	mSPI_CSB[3:1] and Ext_Intr port selection for GPIOA [15:12]: port selection of the mSPI_CSB[3] [11: 8]: port selection of the mSPI_CSB[2] [7: 4]: port selection of the mSPI_CSB[1] [3: 0]: port selection of the Ext_Intr	0x0000

Table 32: RF_SW_OutSel0 (0x4001_0FC8)

Bit	Mode	Symbol	Description	Reset
7:0	R/W	-	RF_SW2/1 port selection for GPIOA [7: 4]: port selection of the RF_SW2 [3: 0]: port selection of the RF_SW1	0x0000

Table 33: UART_OutSel0 (0x4001_0FCC)

Bit	Mode	Symbol	Description	Reset
11:0	R/W	-	UART_TXDOE port selection for GPIOA [11: 8]: port selection of the UART2_TXDOE [7: 4]: port selection of the UART1_TXDOE [3: 0]: port selection of the UART0_TXDOE	0x0000

Table 34: DataIn1 (0x4001_1000)

Bit	Mode	Symbol	Description	Reset
15:0	R	-	GPIOB Input Data	0x0000

Table 35: DataOut1 (0x4001_1004)

Bit	Mode	Symbol	Description	Reset
15:0	R/W	-	GPIOB Output Data	0x0000

Table 36: DataOut_Set1 (0x4001_1010)

Bit	Mode	Symbol	Description	Reset
15:0	R/W	-	GPIOB Data Output Enable set 1 = Output enable 0 = Input enable	0x0000

Table 37: DataOut_Clr1 (0x4001_1014)

Bit	Mode	Symbol	Description	Reset
15:0	R/W	-	GPIOB Data Output clear 1 = Output clear	0x0000

Table 38: AltFunc_Set1 (0x4001_1018)

Bit	Mode	Symbol	Description	Reset
15:0	R/W	-	GPIOB Alternate Function Output enable set 1 = Output enable 0 = disable	0x0000

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Table 39: AltFunc_Clr1 (0x4001_101C)

Bit	Mode	Symbol	Description	Reset
15:0	R/W	-	GPIOB Alternate Function Output clear 1 = Output clear	0x0000

Table 40: IntrEn_Set1 (0x4001_1020)

Bit	Mode	Symbol	Description	Reset
15:0	R/W	-	GPIOB Interrupt set 1 = Interrupt enable 0 = disable	0x0000

Table 41: IntrEn_Clr1 (0x4001_1024)

Bit	Mode	Symbol	Description	Reset
15:0	R/W	-	GPIOB Interrupt clear 1 = Interrupt clear	0x0000

Table 42: IntrType_Set1 (0x4001_1028)

Bit	Mode	Symbol	Description	Reset
15:0	R/W	-		0x0000

Table 43: IntrType_Clr1 (0x4001_102C)

Bit	Mode	Symbol	Description	Reset
15:0	R/W	-		0x0000

Table 44: IntrPol_Set1 (0x4001_1030)

Bit	Mode	Symbol	Description	Reset
15:0	R/W	-		0x0000

Table 45: IntrPol_Clr1 (0x4001_1034)

Bit	Mode	Symbol	Description	Reset
15:0	R/W	-		0x0000

Table 46: IntrStatus1 (0x4001_1038)

Bit	Mode	Symbol	Description	Reset
15:0	R/W	-		0x0000

Table 47: Func_Out_En1 (0x4001_103C)

Bit	Mode	Symbol	Description	Reset
12:0	R/W	-	Alternate Function Output Enable for GPIOB 1 = enable 0 = disable [12]: UART2_TXDOE enable [11]: UART1_TXDOE enable [10]: UART0_TXDOE enable [9]: RF_SW2 enable	0x0000

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Bit	Mode	Symbol	Description	Reset
			[8]: RF_SW1 enable [7]: mSPI_CSB[3] enable [6]: mSPI_CSB[2] enable [5]: mSPI_CSB[1] enable [4]: Ext_Intr enable [3]: PWM_OUT[3] enable [2]: PWM_OUT[2] enable [1]: PWM_OUT[1] enable [0]: PWM_OUT[0] enable	

Table 48: PWM_OutSel1 (0x4001_1FC0)

Bit	Mode	Symbol	Description	Reset
15:0	R/W	-	PWM_OUT[3:0] port selection for GPIOB [15:12]: port selection of the PWM_OUT[3] [11: 8]: port selection of the PWM_OUT[2] [7: 4]: port selection of the PWM_OUT[1] [3: 0]: port selection of the PWM_OUT[0]	0x0000

Table 49: mSPI_CS_OutSel1 (0x4001_1FC4)

Bit	Mode	Symbol	Description	Reset
15:0	R/W	-	mSPI_CSB[3:1] and Ext_Intr port selection for GPIOB [15:12]: port selection of the mSPI_CSB[3] [11: 8]: port selection of the mSPI_CSB[2] [7: 4]: port selection of the mSPI_CSB[1] [3: 0]: port selection of the Ext_Intr	0x0000

Table 50: RF_SW_OutSel1 (0x4001_1FC8)

Bit	Mode	Symbol	Description	Reset
7:0	R/W	-	RF_SW2/1 port selection for GPIOB [7: 4]: port selection of the RF_SW2 [3: 0]: port selection of the RF_SW1	0x0000

Table 51: UART_OutSel1 (0x4001_1FCC)

Bit	Mode	Symbol	Description	Reset
11:0	R/W	-	UART_TXDOE port selection for GPIOB [11: 8]: port selection of the UART2_TXDOE [7: 4]: port selection of the UART1_TXDOE [3: 0]: port selection of the UART0_TXDOE	0x0000

Table 52: DataIn2 (0x4001_7000)

Bit	Mode	Symbol	Description	Reset
15:0	R	-	GPIOC Input Data	0x0000

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Table 53: DataOut2 (0x4001_7004)

Bit	Mode	Symbol	Description	Reset
15:0	R/W	-	GPIOC Output Data	0x0000

Table 54: DataOut_Set2 (0x4001_7010)

Bit	Mode	Symbol	Description	Reset
15:0	R/W	-	GPIOC Data Output Enable set 1 = Output enable 0 = Input enable	0x0000

Table 55: DataOut_Clr2 (0x4001_7014)

Bit	Mode	Symbol	Description	Reset
15:0	R/W	-	GPIOC Data Output clear 1 = Output clear	0x0000

Table 56: AltFunc_Set2 (0x4001_7018)

Bit	Mode	Symbol	Description	Reset
15:0	R/W	-	GPIOC Alternate Function Output enable set 1 = Output enable 0 = Disable	0x0000

Table 57: AltFunc_Clr2 (0x4001_701C)

Bit	Mode	Symbol	Description	Reset
15:0	R/W	-	GPIOC Alternate Function Output clear 1 = Output clear	0x0000

Table 58: IntrEn_Set2 (0x4001_7020)

Bit	Mode	Symbol	Description	Reset
15:0	R/W	-	GPIOC Interrupt set 1 = Interrupt enable 0 = Disable	0x0000

Table 59: IntrEn_Clr2 (0x4001_7024)

Bit	Mode	Symbol	Description	Reset
15:0	R/W	-	GPIOC Interrupt clear 1 = Interrupt clear	0x0000

Table 60: IntrType_Set2 (0x4001_7028)

Bit	Mode	Symbol	Description	Reset
15:0	R/W	-		0x0000

Table 61: IntrType_Clr2 (0x4001_702C)

Bit	Mode	Symbol	Description	Reset
15:0	R/W	-		0x0000

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Table 62: IntrPol_Set2 (0x4001_7030)

Bit	Mode	Symbol	Description	Reset
15:0	R/W	-		0x0000

Table 63: IntrPol_Clr2 (0x4001_7034)

Bit	Mode	Symbol	Description	Reset
15:0	R/W	-		0x0000

Table 64: IntrStatus2 (0x4001_7038)

Bit	Mode	Symbol	Description	Reset
15:0	R/W	-		0x0000

Table 65: Func_Out_En2 (0x4001_703C)

Bit	Mode	Symbol	Description	Reset
12:0	R/W	-	Alternate Function Output Enable for GPIOC 1 = enable 0 = disable [12]: UART2_TXDOE enable [11]: UART1_TXDOE enable [10]: UART0_TXDOE enable [9]: RF_SW2 enable [8]: RF_SW1 enable [7]: mSPI_CSB[3] enable [6]: mSPI_CSB[2] enable [5]: mSPI_CSB[1] enable [4]: Ext_Intr enable [3]: PWM_OUT[3] enable [2]: PWM_OUT[2] enable [1]: PWM_OUT[1] enable [0]: PWM_OUT[0] enable	0x0000

Table 66: PWM_OutSel2 (0x4001_7FC0)

Bit	Mode	Symbol	Description	Reset
15:0	R/W	-	PWM_OUT[3:0] port selection for GPIOC [15:12]: port selection of the PWM_OUT[3] [11: 8]: port selection of the PWM_OUT[2] [7: 4]: port selection of the PWM_OUT[1] [3: 0]: port selection of the PWM_OUT[0]	0x0000

Table 67: mSPI_CS_OutSel2 (0x4001_7FC4)

Bit	Mode	Symbol	Description	Reset
15:0	R/W	-	mSPI_CSB[3:1] and Ext_Intr port selection for GPIOC [15:12]: port selection of the mSPI_CSB[3] [11: 8]: port selection of the mSPI_CSB[2] [7: 4]: port selection of the mSPI_CSB[1] [3: 0]: port selection of the Ext_Intr	0x0000

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Table 68: RF_SW_OutSel2 (0x4001_7FC8)

Bit	Mode	Symbol	Description	Reset
7:0	R/W	-	RF_SW2/1 port selection for GPIOC [7: 4]: port selection of the RF_SW2 [3: 0]: port selection of the RF_SW1	0x0000

Table 69: UART_OutSel2 (0x4001_7FCC)

Bit	Mode	Symbol	Description	Reset
11:0	R/W	-	UART_TXDOE port selection for GPIOC [11: 8]: port selection of the UART2_TXDOE [7: 4]: port selection of the UART1_TXDOE [3: 0]: port selection of the UART0_TXDOE	0x0000

value / bit sel	0	1	2	3	4	5	6	7	8	9	10
FSEL_GPIO[31:30]	Semi-fixed pin : JTAG_01 TMS TCLK	D_SYS D_SYS_OUT[0] D_SYS_OUT[1]	GPIO(2) x GPIOA[15]	GPIO(2) x GPIOA[15]							
FSEL_GPIO[29:28] FSEL_GPIO[27:26] FSEL_GPIO[25:24]	UART2_01 I2S_CLK_In UART2_RXD UART2_TXD	BT(0:2) BT_sig2 (iBTPri) BT_sig1 (iBtAct) BT_sig0 (oWlanAct)	D_SYS D_SYS_CLK D_SYS_OUT[3] D_SYS_OUT[2]	GPIO(2) GPIOA[14] GPIOA[13] GPIOA[12]							
FSEL_GPIO[22:20]	G(1) + BT GPIOA[11] BT_sig2 (iBTPri)	G(1) + I2S GPIOA[11] I2S_CLK_In	G(1) + eMMC(6) GPIOA[11] mSDeMMC_WRP	sSPI (2:3) sSPI_MOSI sSPI_MISO	UART2 (0:1) UART2_RXD UART2_TXD	mSPI (4:5) E_SPI_IO3 E_SPI_IO2	GPIO(2) GPIOA[11] GPIOA[10]	GPIO(2) GPIOA[11] GPIOA[10]			
FSEL_GPIO[19:16]	5G control(45) 5GC_Sig[5] 5GC_Sig[4]	sSPI (2:3) sSPI_MOSI sSPI_MISO	eMMC (0:1) mSDeMMC_D0 mSDeMMC_D1	sSDIO (0:1) sSDIO_D0 sSDIO_D1	I2C_master mI2C_CLK mI2C_SDA	BT (0:1) BT_sig1 (iBtAct) BT_sig0 (oWlanAct)	mSPI (2:3) E_SPI_IO1 E_SPI_IO0	I2S(0:1) I2S_MCLK I2S_BCLK	GPIO(2) GPIOA[9] GPIOA[8]	GPIO(2) GPIOA[9] GPIOA[8]	
FSEL_GPIO[15:12]		sSPI (0:1) sSPI_CLK sSPI_CSB	eMMC (2:3) mSDeMMCIO_D2 mSDeMMCIO_D3	sSDIO (2:3) sSDIO_D2 sSDIO_D3	UART1 (0:1) UART1_RXD UART1_TXD	I2C slave sI2C_CLK sI2C_SDA	mSPI (0:1) E_SPI_CLK E_SPI_CSB	I2S(2:3) I2S_LRCK I2S_SDO	GPIO(2) GPIOA[7] GPIOA[6]	GPIO(2) GPIOA[7] GPIOA[6]	
FSEL_GPIO[11: 8]	5G control(01) 5GC_Sig[3] 5GC_Sig[2]	I2C slave sI2C_CLK sI2C_SDA	eMMC (4:5) mSDeMMC_CLK mSDeMMC_CMD	sSDIO (4:5) sSDIO_CLK sSDIO_CMD	UART1 (2:3) UART1_CTS UART1_RTS	I2C master mI2C_CLK mI2C_SDA	UART1 (0:1) UART1_RXD UART1_TXD	I2S(0:1) I2S_MCLK I2S_BCLK	GPIO(2) GPIOA[5] GPIOA[4]	GPIO(2) GPIOA[5] GPIOA[4]	
FSEL_GPIO[7: 4]	AD12 (2) X (Analog In) X (Analog In)	sSPI (0:1) sSPI_CLK sSPI_CSB	I2S (2:3) I2S_LRCK I2S_SDO	I2C slave sI2C_CLK sI2C_SDA	UART1 (0:1) UART1_RXD UART1_TXD		AD12(1) + GPIO(1) GPIO[3] X (Analog In)	AD12(1) + I2S_CLK I2S_CLK_In X (Analog In)	GPIO(2) GPIOA[3] GPIOA[2]	GPIO(2) GPIOA[3] GPIOA[2]	
FSEL_GPIO[3: 0]	AD12 (2) X (Analog In) X (Analog In)	sSPI (2:3) sSPI_MOSI sSPI_MISO	I2S (0:1) I2S_MCLK I2S_BCLK	I2C slave sI2C_CLK sI2C_SDA	UART1 (0:1) UART1_RXD UART1_TXD	I2C master mI2C_CLK mI2C_SDA	5G control(01) 5GC_Sig[1] 5GC_Sig[0]	AD12(1) + GPIO(1) GPIO[1] X (Analog In)	AD12(1) + WRP mSDeMMC_WRP X (Analog In)	GPIO(2) GPIOA[1] GPIOA[0]	GPIO(2) GPIO[1] GPIO[0]

Figure 1: PIN MUX Table

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bit sel \ value	0	1	2	3	4	5
FSEL_GPIO2[21:20]	JTAG(2:3) TDI TDO nTRST	G(1) + UART2 (0:1) GPIO[8] UART2_RXD UART2_TXD	GPIO(2) GPIOC[8] GPIOC[7] GPIOC[6]			
FSEL_GPIO2[19:18]	G(1) + I2S I2S_CLK_In GPIO[4]	UART2 (2:3) UART2_CTS UART2_RTS	GPIO(2) E_SPI_IO3 E_SPI_IO2	GPIO(2) GPIOC[5] GPIOC[4]		
FSEL_GPIO2[17:16]	UART1 (2:3) UART1_CTS UART1_RTS	5G control(45) 5GC_Sig[1] 5GC_Sig[0]	GPIO(2) GPIOC[3] GPIOC[2]			
FSEL_GPIO2[15:14]	UART1 (0:1) UART1_RXD UART1_TXD	I2C master mI2C_CLK mI2C_SDA	GPIO(2) GPIOC[1] GPIOC[0]			
FSEL_GPIO2[13:12]	I2S(0:3) I2S_LRCK I2S_SDO I2S_MCLK I2S_BCLK	QSPI (4:7) H_SPI_DIO7 H_SPI_DIO6 H_SPI_DIO5 H_SPI_DIO4	GPIOB(4) GPIOB[11] GPIOB[10] GPIOB[9] GPIOB[8]			
FSEL_GPIO2[11:10]	mSPI (0:3) E_SPI_IO1 (mSPI_MISO) E_SPI_IO0 (mSPI_MOSI) E_SPI_CSB[0] E_SPI_CLK	5G control(0:3) 5GC_Sig[5] 5GC_Sig[4] 5GC_Sig[3] 5GC_Sig[2]	GPIOB(4) GPIOB[7] GPIOB[6] GPIOB[5] GPIOB[4]	GPIOB(4) GPIOB[7] GPIOB[6] GPIOB[5] GPIOB[4]		
FSEL_GPIO2[9:8]	sSPI(0:3) sSPI_CLK sSPI_CSB sSPI_MOSI sSPI_MISO		GPIOB(4) GPIOB[3] GPIOB[2] GPIOB[1] GPIOB[0]	GPIOB(4) GPIOB[3] GPIOB[2] GPIOB[1] GPIOB[0]		
FSEL_GPIO2[6:4]	QSPI (4:5) F_IO3 (F_HOLD) F_IO2 (F_WP)	UART2 (0:1) UART2_TXD UART2_RXD		sSDIO(4:5) sSDIO_D3 sSDIO_D2	GPIO(2) GPIOC[14] GPIOC[13]	GPIO(2) GPIOC[14] GPIOC[13]
FSEL_GPIO2[3:0]	QSPI (3:0) F_IO1 (F_SI) F_IO0 (F_SO) F_CLK F_CSB[1]	sSPI (3:0) sSPI_MISO sSPI_MOSI sSPI_CLK sSPI_CSB	I2S(0:3) I2S_SDO I2S_LRCK I2S_MCLK I2S_BCLK	sSDIO(0:3) sSDIO_D1 sSDIO_D0 sSDIO_CLK sSDIO_CMD	GPIO(4) GPIOC[12] GPIOC[11] GPIOC[10] GPIOC[9]	GPIO(4) GPIOC[12] GPIOC[11] GPIOC[10] GPIOC[9]

Figure 2: PIN MUX Table (Continued)

Note 1 Black: input, red: output, violet: in/out.

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4.2 UART Register

There are three UARTs in DA162000. UART0 is a dedicated port for the debug console. The two other UARTs, namely UART1 and UART2, are available to the user. HW flow control is possible at UART1 but not at UART2.

RS485 and RS232 are supported in DA16200. The specifications supported for RS232 and RS485 are summarized as follows:

Specification	RS-232	RS-485
Differential	No	Yes
Operation Mode	Full duplex	Half duplex
Maximum Baud Rate	921600 Baud	5M Baud
Flow Control	Support	Support

Note 1 See the UART section in DA16200 SDK Programmer's Guide [1] for the pin configurations of the UARTs.

The base address of each UART is:

- UART0: 4001_2XXX
- UART1: 4000_7XXX
- UART2: 4000_9XXX

Note 1 All UARTs have the same bit map.

Table 70: UART Registers Overview

Offset	Register	Description
0x000	UART_DATA	UART Data Register
0x004	UART_RXSTS / UART_ERRCLR	UART Receive Status Register Error Clear Register
0x018	UART_FLAG	UART Flag Register
0x024	UART_INTBRDIV	UART Integer Baud Rate Divisor Register
0x028	UART_FRABRDIV	UART Fractional Baud Rate Divisor Register
0x02C	UART_LCNTRL	UART Line Control Register
0x030	UART_CNTRL	UART Control Register
0x034	UART_INTFLS	UART Interrupt FIFO Level Select Register
0x038	UART_INTMSKSC	UART Interrupt Mask Set/Clear Register
0x040	UART_INTMSKSTS	UART Masked Interrupt Status Register
0x044	UART_INTCLR	UART Interrupt Clear Register
0x048	UART_DMACNTRL	UART DMA Control Register
0x04C	UART_WAEN	UART Word Access Enable Register
0x054	UART_485EN	UART RS-485 Mode Enable Register

Table 71: UART_DATA (0x000)

Bit	Mode	Symbol	Description	Reset
15:12	-	-	Reserved	0x0

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Bit	Mode	Symbol	Description	Reset
11:8	RO	-	Error status for data read. These bits cannot be read when UART_WAEN is enabled. [11] Overrun Error [10] Break Error [9] Parity Error [8] Framing Error	0x0
7:0	R/W	DATA	Receive data bits for data read Transmit data bits for data write	0x00

Table 72: UART_RXSTS / UART_ERRCLR (0x004)

Bit	Mode	Symbol	Description	Reset
15:8	-	-	Reserved	0x00
7:0	WO	-	UART_ERRCLR, A write to this register clears every error. The value is not important	0x00
7:4	RO	-	UART_RXSTS, Reserved	0x0
3:0	RO	-	UART_RXSTS, UART error status [3] Overrun error [2] Break error [1] Parity error [0] Framing error	0x0

Table 73: UART_FLAG (0x018)

Bit	Mode	Symbol	Description	Reset
15:8	-	-	Reserved	0x00
7:4	RO	-	The status of FIFOs [7] TXFE, Transmit FIFO empty [6] RXFF, Receive FIFO full [5] TXFF, Transmit FIFO full [4] RXFE, Receive FIFO empty	0x9
3	RO	BUSY	UART busy. This bit is set to 1 as soon as the transmit FIFO becomes non-empty	0x0
2:0	-	-	Reserved	0x0

Table 74: UART_INTBRDIV (0x024)

Bit	Mode	Symbol	Description	Reset
15:0	R/W	IBRD	Integer baud rate divisor	0x0000

Table 75: UART_FRABRDIV (0x028)

Bit	Mode	Symbol	Description	Reset
15:6	-	-	Reserved	0x000
5:0	R/W	FBRD	Fractional baud rate divisor	0x00

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Table 76: UART_LCNTRL (0x02C)

Bit	Mode	Symbol	Description	Reset
15:8	-	-	Reserved	0x00
7	R/W	SPS	Stick parity select 0 = Stick parity disabled 1 = Either * If PARSEL bit is 0, the parity bit is transmitted and checked as a 1 * If PARSEL bit is 1, the parity bit is transmitted and checked as a 0	0x0
6:5	R/W	DTLEN	The number of data bits transmitted or received in a frame. b'11 = 8 bits b'10 = 7 bits b'01 = 6 bits b'00 = 5 bits	0x0
4	R/W	FIFOEn	FIFO Enable 0 = UART FIFO disabled 1 = UART Transmit and Receive FIFO enabled	0x0
3	R/W	TSTP	Two stop bits select 0 = Two bits are transmitted as stop bit 1 = One bit is transmitted as stop bit	0x0
2	R/W	PARSEL	Parity select: 0 = odd parity 1 = even parity	0x0
1	R/W	PAREn	Parity enable: 0 = Parity is disabled 1 = Parity is enabled	0x0
0	-		Reserved	0x0

Table 77: UART_CNTRL (0x030)

Bit	Mode	Symbol	Description	Reset
15	R/W	CTSEn	UART CTS hardware flow control enable 0 = CTS hardware flow control disabled 1 = CTS hardware flow control enabled	0x0
14	R/W	RTSEn	UART RTS hardware flow control enable 0 = RTS hardware flow control disabled 1 = RTS hardware flow control enabled	0x0
13:10	-	-	Reserved	0x0
9	R/W	RXEn	Receive enable 0 = Receive section of the UART disabled 1 = Receive section of the UART enabled	0x1
8	R/W	TXEn	Transmit enable 0 = Transmit section of the UART disabled 1 = Transmit section of the UART enabled	0x1
7:1	-	-	Reserved	0x00
0	R/W	UARTEn	UART enable	0x0

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Bit	Mode	Symbol	Description	Reset
			0 = UART is disabled 1 = UART is enabled	

Table 78: UART_INTFLS (0x034)

Bit	Mode	Symbol	Description	Reset
15:6	-	-	Reserved	0x000
5:3	R/W	RXIFLS	UART receive interrupt FIFO level select. The receive interrupt occurs as follows: b'000 = Receive FIFO ≥ 1/8 full b'001 = Receive FIFO ≥ 1/4 full b'010 = Receive FIFO ≥ 1/2 full b'011 = Receive FIFO ≥ 3/4 full b'100 = Receive FIFO ≥ 7/8 full b'101 b'111 = Reserved	0b010
2:0	R/W	TXIFLS	UART transmit interrupt FIFO level select. The transmit interrupt occurs as follows: b'000 = Transmit FIFO ≤ 1/8 full b'001 = Transmit FIFO ≤ 1/4 full b'010 = Transmit FIFO ≤ 1/2 full b'011 = Transmit FIFO ≤ 3/4 full b'100 = Transmit FIFO ≤ 7/8 full b'101 b'111 = Reserved	0b010

Table 79: UART_INTMSKSC (0x038)

Bit	Mode	Symbol	Description	Reset
15:11	-	-	Reserved	0x00
10:7	R/W	-	Error interrupt mask [10] = Overrun error interrupt mask [9] = Break error interrupt mask [8] = Parity error interrupt mask [7] = Framing error interrupt mask	0x0
6	R/W	RXTIM	Receive timeout interrupt mask	0x0
5	R/W	TXIM	Transmit interrupt mask	0x0
4	R/W	RXIM	Receive interrupt mask	0x0
3:0	-	-	Reserved	0x0

Table 80: UART_INTMSKSTS (0x040)

Bit	Mode	Symbol	Description	Reset
15:11	-	-	Reserved	0x00
10:7	RO	-	Error interrupt mask [10] = Overrun error interrupt mask [9] = Break error interrupt mask [8] = Parity error interrupt mask [7] = Framing error interrupt mask	0x0
6	RO	RXTIMS	Receive timeout masked interrupt status	0x0

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Bit	Mode	Symbol	Description	Reset
5	RO	TXIMS	Transmit masked interrupt status	0x0
4	RO	RXIMS	Receive masked interrupt status	0x0
3:0	-	-	Reserved	0x0

Table 81: UART_INTCLR (0x044)

Bit	Mode	Symbol	Description	Reset
15:11	-	-	Reserved	0x00
10:7	WO	-	Error interrupt mask [10] = Overrun error interrupt clear [9] = Break error interrupt clear [8] = Parity error interrupt clear [7] = Framing error interrupt clear	0x0
6	WO	RXTICLR	Receive timeout interrupt clear	0x0
5	WO	TXICLR	Transmit interrupt clear	0x0
4	WO	RXICLR	Receive interrupt clear	0x0
3:0	-	-	Reserved	0x0

Table 82: UART_DMACNTRL (0x048)

Bit	Mode	Symbol	Description	Reset
15:2	-	-	Reserved	0x0000
1	R/W	TXDMAEn	Transmit DMA enable 0 = Transmit DMA is disabled 1 = Transmit DMA is enabled	0x0
0	R/W	RXDMAEn	Receive DMA enable 0 = Receive DMA is disabled 1 = Receive DMA is enabled	0x0

Table 83: UART_WAEN (0x04C)

Bit	Mode	Symbol	Description	Reset
15:1	-	-	Reserved	0x0000
0	R/W	WA	UART word access enable register 0 = UART Word Access is disabled 1 = UART Word Access is enabled	0x1

Table 84: UART_485EN (0x054)

Bit	Mode	Symbol	Description	Reset
15:1	-	-	Reserved	0x0000
0	R/W	RS485En	UART RS-485 mode enable register 0 = UART RS-485 mode is disabled 1 = UART RS-485 mode is enabled	0x0

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4.3 I2S Register

DA16200 provides an I2S interface that has both I2S transmission and reception functions. However, the transmission and reception functions cannot be used at the same time. The transmit and receive functions can be selected by setting the register.

When the I2S clock divider register is used, the internal PLL clock can be variably applied to the I2S clock source. The available I2S clock source is 24/48 MHz. There is also a way to apply the I2S clock source directly from the outside with the use of the GPIO pin.

Table 85: I2S Registers Overview

Address	Register	Description
Common control for I2S Pin Status		
0x4001_4000	I2S_CTRL0	I2S Control Register 0
0x4001_4004	I2S_CTRL1	I2S Control Register 1
0x4001_4008	I2S_DATA	I2S Data Register
0x4001_400C	I2S_STATUS	I2S Status Register
0x4001_4010	Reserved	
0x4001_4014	I2S_IMASK	I2S Interrupt Mask Register
0x4001_4018	Reserved	
0x4001_401C	Reserved	
0x4001_4020	I2S_ICR	I2S Rx Overrun Interrupt Clear Register
0x4001_4024	I2S_DMACR	I2S DMA Enable Register
0x5000_1314	I2S_CLK_SEL	I2S Clock divider Register

Table 86: I2S_CTRL0 (0x4001_4000)

Bit	Mode	Symbol	Description	Reset
15:12	R/W	CLK_DIV	I2S_SCLK control factor 4'h0: I2SCLK/2 4'h1: I2SCLK/4 4'h3: I2SCLK/8 4'h7: I2SCLK/16	4'b0011
11	R/W	STEREO	1 = Stereo 0 = Mono	1'b0
10:9	R/W	PCM_BW	PCM bus width for Tx / Rx Tx Rx 2'b11: PCM_24 PCM_32 2'b10: PCM_20 PCM_24/PCM_20 2'b01: PCM_16 PCM_16 2'b00: PCM_8 PCM_8	2'b00
8	R/W	MUTE	If set, SDATA output assert “0”	1'b0
7	R/W	HALF_DELAY	Relationship between FS and SCLK 1: Falling edge	1'b0
6	R/W	PCMM	If set, PCM Mode is enabled	1'b1

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Bit	Mode	Symbol	Description	Reset
5	R/W	Right_Align	If set, PCM data output right is enabled	1'b0
4	R/W	ENDIAN	SDATA Output mode 1 = Big endian 0 = Little endian	1'b0
3	R/W	MCLK_INV	If set, MCLK inversion	1'b1
2	R/W	LRCK_INV	If set, LRCK inversion	1'b0
1	R/W	I2S_Enalbe	If set, I2S block is enabled	1'b0
0	R/W	CLK_DOWN	If set, output clock signals, LRCK/BCLK/SCLK, assert “0”	1'b0

Table 87: I2S_CTRL1 (0x4001_4004)

Bit	Mode	Symbol	Description	Reset
15:8	-	-	Reserved	
7	R/W	RxFIFO_Rst	Master Rx FIFO reset 0: reset 1: normal	1'b0
6	-	-		
5	R/W	Left_Justify	Rx decoding left justified	1'b0
4	R/W	Rx_Mode	Rx decoding edge 0: rising edge @SCLK 1: falling edge	1'b0
3	R/W	Mst_RxEn	Master Rx load enable signal 0: Tx enable 1: Rx enable	1'b0
2	-	-		
1	R/W	Rx_ChSel	Rx data channel selection 0=Rx decoding only Right channel 1=Rx decoding only Left channel	1'b0
0	R/W	LR_ChSel	Left/Right Channel selection 1: first data comes out LRCK high 0: first data comes out LRCK low duration	1'b0

Table 88: I2S_DATA (0x4001_4008)

Bit	Mode	Symbol	Description	Reset
31:0	R/W	I2S_DATA	I2S_DATA write data @ Tx read data @ Rx	32'b0000

Table 89: I2S_STATUS (0x4001_400C)

Bit	Mode	Symbol	Description	Reset
5:0	R	Status	[5]: Rx FIFO Not Empty [4]: Rx FIFO Full [2]: BUSY [1]: Tx FIFO Not FULL	

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Bit	Mode	Symbol	Description	Reset
			[0]: Tx FIFO EMPTY	

Table 90: I2S_IMASK (0x4001_4014)

Bit	Mode	Symbol	Description	Reset
3	R/W	TXIM	Tx FIFO Interrupt DMA TX request Mask When TX FIFO arrives at half size. 1 = Enable 0 = Disable	1'b0
2	R/W	RXIM	Rx FIFO Interrupt DMA RX request Mask When RX FIFO arrives at half size. 1 = Enable 0 = Disable	1'b0
1	R/W	RTIM	Rx Receive Timeout Interrupt Mask 1 = Enable 0 = Disable Reserved. Not used.	1'b0
0	R/W	RORIM	Rx Over Run Interrupt DMA RX request Mask When RX FIFO arrives at full size. 1 = Enable 0 = Disable	1'b0

Table 91: I2S_ICR (0x4001_4020)

Bit	Mode	Symbol	Description	Reset
0	R/W	RORIC	Rx Over Run Interrupt DMA RX request Clear	1'b0

Table 92: I2S_DMACR (0x4001_4024)

Bit	Mode	Symbol	Description	Reset
1	R/W	TXDMAE	Tx DMA Enable 1 = Enable 0 = Disable	1'b0
0	R/W	RXDMAE	Rx DMA Enable 1 = Enable 0 = Disable	1'b0

Table 93: I2S_CLK_SEL (0x5000_1314)

Bit	Mode	Symbol	Description	Reset
2:0	R/W	-	FNPLL frequency divider factor register 3'h0: no clock 3'h1: FNPLL 1/2 3'h2: FNPLL 1/4 3'h3: FNPLL 1/8	3'b000

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4.4 SDeMMC Register

The SD/eMMC host IP provides the function for DA16200 to access SD or eMMC cards. This SD/eMMC host IP only supports a 4-bit data bus and the maximum clock rate is 50 MHz.

Address	Register	Description
Common control for SDeMMC Pin Status		
0x5003_0000	HIF_CTRL0	I2S Control Register 0
0x5003_0004	HIF_EVNT_CTRL	I2S Control Register 1
0x5003_0008	HIF_INT_CTRL	I2S Data Register
0x5003_000C	HIF_CLK_CNT_CTRL	I2S Status Register
0x5003_0010	HIF_CMD_ARG	
0x5003_0014	HIF_CMD_IDX	I2S Interrupt Mask Register
0x5003_0018	HIF_CMD_ARGQ	
0x5003_001C	HIF_CND_IDXQ	
0x5003_0020	HIF_PAD_CTRL	I2S Rx Overrun Interrupt Clear Register
0x5003_0024	HIF_BLK_LG	I2S DMA Enable Register
0x5003_0028	HIF_BLK_CNT	
0x5003_002C	Reserved	
0x5003_0030	HIF_RSP_TMO_CNT	
0x5003_0034	HIF_RD_TMO_CNT	
0x5003_0038	HIF_WB_TMO_CNT	
0x5003_003C	HIF_RSP_CIX_ST	
0x5003_0040	HIF_RSP_ARG_0	
0x5003_0044	HIF_RSP_ARG_1	
0x5003_0048	HIF_RSP_ARG_2	
0x5003_004C	HIF_RSP_ARG_3	
0x5003_0050	HIF_AHB_SA	
0x5003_0054	HIF_AHB_EA	
0x5003_0058	Reserved	
0x5003_005C	Reserved	
0x5003_0060	HIF_BUS_ST	
0x5003_0064	HIF_SM_ST	
0x5003_0068	HIF_XTR_CNT	
0x5003_006C	HIF_ERR_CNT	

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Table 94: HIF_CTRL0 (0x5003_0000)

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Bit	Mode	Symbol	Description	Reset
31:16	-	-	Reserved	
15	R/W	ALL_RST	Reset All H/W Circuit Control 0: Normal Operation 1: Reset	1'b0
14	R/W	HIF_RST	Control Register and H/W Circuit Control 0: Normal Operation 1: Reset	1'b0
13	R/W	CSM_RST	Command State Machine Reset Control 0: Normal Operation 1: Reset	1'b0
12	R/W	DSM_RST	Data State Machine Reset Control 0: Normal Operation 1: Reset	1'b0
11	R/W	STOP_XTR	Immediately Stop the Ongoing Data Transfer 0: Normal Operation 1: Immediately Stop the Ongoing Data Transfer	1'b0
9:8	R/W	WR_STR_CTL[1:0]	Data Transfer Start Control for Write Operation 2'b0x: The starting of write data is triggered by TRIG bit of HIF_CMD_IDX register 2'b10: Not trigger the starting for write data operation 2'b11: Trigger the starting for write data operation	2'b00
7	R/W	HIF_PWR_CTL	Host Interface Power Control 0: Turn-off host interface power 1: Turn-on host interface power	1'b0
6	-	-	Reserved	
5	R/W	CDI_POL_CTL	Card Detect Input Polarity Control 0: low active 1: high active	1'b0
4	R/W	RD_CRC_CHK	Read Data CRC Check Control 0: Disable 1: Enable	1'b1
3	R/W	RSP_CRC_CK	Response CRC Check Control 0: Disable 1: Enable	1'b1
2	R/W	BUS_4BIT	4 Bit Data Bus Mode 0: 1-bit Mode 1: 4-bit Mode	1'b0
1	R/W	HIGH_SPD	High Speed Timing Mode 0: Default Speed Timing Mode (SDC and SDATA[3:0] signals output at clock falling edge) 1: High Speed Timing Mode (SDC and SDATA[3:0] signals output at clock rising edge)	1'b0
0	R/W	CDO_MODE	Command/Data Output Mode 0: Open Drain Mode 1: Push-Pull Mode	1'b0

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Table 95: HIF_EVNT_CTRL (0x5003_0004)

Bit	Mode	Symbol	Description	Reset
31	R	P_CD_IN_ST	Card Detect Pad Status	1'b0
30	R	P_WP_IN_ST	Write Protect Pad Status	1'b0
29	R/W	CD_IN_EST	Card Detect Event Status 0: No Event Generation 1: Event Generation	1'b0
28	R/W	WP_IN_EST	Write Protect Event Status 0: No Event Generation 1: Event Generation	1'b0
27	R/W	XTR_END_EST	Read/Write Data Transfer End Event Status 0: No Event Generation 1: Event Generation	1'b0
26	R/W	BLK_END_EST	Read/Write One Block Data Event Status 0: No Event Generation 1: Event Generation	1'b0
25	R/W	NG_CRCS_EST	Negative Write CRC Status Token Event Status 0: No Event Generation 1: Event Generation	1'b0
24	R/W	WDB_TMO_EST	Write Data Busy Time-out Event Status 0: No Event Generation 1: Event Generation	1'b0
23	R/W	RXT_END_EST	Read Data Transfer End Event Status 0: No Event Generation 1: Event Generation	1'b0
22	R/W	SRD_END_EST	Complete to Read Single Block Data Event Status 0: No Event Generation 1: Event Generation	1'b0
21	R/W	RD_CRCE_EST	Read Data CRC Error Event Status 0: No Event Generation 1: Event Generation	1'b0
20	R/W	RD_TMO_EST	Read Data Time-out Event Status 0: No Event Generation 1: Event Generation	1'b0
19	-	-	Reserved	1'b0
18	R/W	RSP_END_EST	Command/Response End Event Status 0: No Event Generation 1: Event Generation	1'b0
17	R/W	RP_CRCE_EST	Response CRC Error Event Status 0: No Event Generation 1: Event Generation	1'b0
16	R/W	RSP_TMO_EST	Response Time-out Event Status 0: No Event Generation 1: Event Generation	1'b0
15:14	-	-	Reserved	
13	R/W	CD_IN_ETE	Card Detect Event Control	1'b0

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Bit	Mode	Symbol	Description	Reset
			0: Disable 1: Enable	
12	R/W	WP_IN_ETE	Write Protect Event Control 0: Disable 1: Enable	1'b1
11	R/W	XTR_END_ETE	Read/Write Data Transfer End Event Control 0: Disable 1: Enable	1'b1
10	R/W	BLK_END_ETE	Read/Write One Block Data Event Control 0: Disable 1: Enable	1'b0
9	R/W	NG_CRCS_ETE	Negative Write CRC Status Token Event Control 0: Disable 1: Enable	1'b1
8	R/W	WDB_TMO_ETE	Write Data Busy Time-out Event Control 0: Disable 1: Enable	1'b0
7:6	-	-	Reserved	
5	R/W	RD_CRCE_ETE	Read Data CRC Error Event Control 0: Disable 1: Enable	1'b1
4	R/W	RD_TMO_ETE	Read Data Time-out Event Control 0: Disable 1: Enable	1'b1
3	-	-	Reserved	1'b1
2	R/W	RSP_END_ETE	Response End Event Control 0: Disable 1: Enable	1'b1
1	R/W	RP_CRCE_ETE	Response CRC Error Event Control 0: Disable 1: Enable	1'b1
0	R/W	RSP_TMO_ETE	Response Time-out Event Control 0: Disable 1: Enable	1'b1

Table 96: HIF_INT_CTRL (0x5003_0008)

Bit	Mode	Symbol	Description	Reset
31	R	HST_INT_ST	SD/eMMC Host Interrupt Status 0: No Interrupt Generation 1: Interrupt Generation	1'b0
30	-	-	Reserved	1'b0
29	R/W	CD_INT_ST	Card Detect Interrupt Status 0: No Interrupt Generation 1: Interrupt Generation	1'b0
28	R/W	WP_INT_ST	Write Protect Interrupt Status	1'b0

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Bit	Mode	Symbol	Description	Reset
			0: No Interrupt Generation 1: Interrupt Generation	
27	R/W	XTR_END_IST	Read/Write Data Transfer End Interrupt Status 0: No Interrupt Generation 1: Interrupt Generation	1'b0
26	R/W	BLK_END_IST	Read/Write One Block Data Interrupt Status 0: No Interrupt Generation 1: Interrupt Generation	1'b0
25	R/W	NG_CRCS_IST	Negative Write CRC Status Token Interrupt Status 0: No Interrupt Generation 1: Interrupt Generation	1'b0
24	R/W	WDB_TMO_IST	Write Data Busy Time-out Interrupt Status 0: No Interrupt Generation 1: Interrupt Generation	1'b0
23:22	-	-	Reserved	1'b0
21	R/W	RD_CRCE_IST	Read Data CRC Error Interrupt Status 0: No Interrupt Generation 1: Interrupt Generation	1'b0
20	R/W	RD_TMO_IST	Read Data Time-out Interrupt Status 0: No Interrupt Generation 1: Interrupt Generation	1'b0
19	-	-	Reserved	1'b0
18	R/W	RSP_END_IST	Command/Response End Interrupt Status 0: No Interrupt Generation 1: Interrupt Generation	1'b0
17	R/W	RD_CRCE_IST	Read Data CRC Error Interrupt Status 0: No Interrupt Generation 1: Interrupt Generation	1'b0
16	R/W	RSP_TMO_IST	Response Time-out Interrupt Status 0: No Interrupt Generation 1: Interrupt Generation	1'b0
15	R/W	HST_ENT_EN	SD/eMMC Host Interrupt Function Enable Control 0: Disable 1: Enable	1'b0
14	-	-	Reserved	
13	R/W	CD_INT_EN	Card Detect Interrupt Control 0: Disable 1: Enable	1'b0
12	R/W	WP_INT_EN	Write Protect Interrupt Control 0: Disable 1: Enable	1'b0
11	R/W	XTR_INT_EN	Read/Write Data Transfer End Interrupt Control 0: Disable 1: Enable	1'b0
10	R/W	BLK_INT_EN	Read/Write One Block Data Interrupt Control	1'b0

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Bit	Mode	Symbol	Description	Reset
			0: Disable 1: Enable	
9	R/W	NG_CRCS_INT	Negative Write CRC Status Token Interrupt Control 0: Disable 1: Enable	1'b0
8	R/W	WDB_TMO_INT	Write Data Busy Time-out Interrupt Control 0: Disable 1: Enable	1'b0
7:6	-	-	Reserved	
5	R/W	RD_CRCE_INT	Read Data CRC Error Interrupt Control 0: Disable 1: Enable	1'b0
4	R/W	RD_TMO_INT	Read Data Time-out Interrupt Control 0: Disable 1: Enable	1'b0
3	-	-	Reserved	1'b0
2	R/W	RP_DIRE_INT	Response Direction Bit Error Interrupt Control 0: Disable 1: Enable	1'b0
1	R/W	RP_CRCE_INT	Response CRC Error Interrupt Control 0: Disable 1: Enable	1'b0
0	R/W	RSP_TMO_INT	Response Time-out Interrupt Control 0: Disable 1: Enable	1'b0

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Table 97: HIF_CLK_CNT_CTRL (0x5003_000C)

Bit	Mode	Symbol	Description	Reset
31:23	-	-	Reserved	
22	R/W	STOP_HCLK	Enable to Stop SD/eMMC Interface Clock 0: Disable 1: Enable	1'b0
21	R/W	SYNC_STCTL	Synchronous Circuit Stage Control 0: 3-Stage Synchronizer (Low clock ratio) 1: 2-Stage Synchronizer (High clock ratio)	1'b0
20	R/W	HCLK_OE	HCLK Output Enable Control 0: Disable 1: Enable (Normal Operation)	1'b1
19	-	-	Reserved	
18:17	R/W	HCLK_CTL	Internal Host Clock Control 00: Turn off the internal host clock 01: Turn off the internal host clock immediately 10: Turn on the internal host clock immediately 11: Always turn on internal host clock	2'b11
16	R	HCLK_SW	SW Host Clock Control **Note:** S/W can program this bit to high/low, to toggle the internal host clock when HCLK_CTL[1:0] = 2'b00	1'b0
15:0	R/W	HCLK_CT_CNT	Host Clock Control Count Register This control register specifies the number of host clock to enable or stop the host clock signal	16'h0

Table 98: HIF_CMD_ARG (0x5003_0010)

Bit	Mode	Symbol	Description	Reset
31:0	R/W	HCLK_CMD_ARG	This register specifies the value of SD/eMMC command argument	32'h0

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Table 99: HIF_CMD_IDX (0x5003_0014)

Bit	Mode	Symbol	Description	Reset
31:16	-	-	Reserved	
15	R/W	CMDQ_TRIG	Trigger to transfer the value of Command Index and Argument registers into Command Index Queue and Command Argument Queue registers. The trigger (transfer) operation is only active when the value of this bit is high, and the status of command queue is not busy (QBUSY_ST)	1'b0
14	R/W	CMD_TCTL	Command Trigger Control 0: Start a new command immediately when the command trigger (CMDQ_TRIG) bit was set 1: Only start a new command when the command trigger (CMDQ_TRIG) bit was set and the previous response result has been read	1'b0
13	R/W	STB_CTL	Command Start Bit and Transmission Bit Control 0: The start bit and transmission bit of the SD/eMMC command is automatically generated by H/W circuit 1: The start bit and transmission bit of the SD/eMMC command refers to the STR_BIT and TRM_BIT of this control register	1'b0
12:11	R/W	RSP_TYPE	Response Type Control 00: No Response 01: R3 Response 10: Short Response (Total: 48 bits) 11: Long Response (Total: 136 bits)	2'b00
10:9	R/W	DATA_TYPE	Data Type Control 0x: Command only (without data transfer) 10: Command with single/multiple read data 11: Command with single/multiple write data	2'b00
8	-	-	Reserved	
7	R/W	STR_NIT	This register specifies the value of the start bit of SD/eMMC command if STB_CTL bit is set to high. Otherwise, it is not used	1'b0
6	R/W	TRM_BIT	This register specifies the value of the transmission bit of SD/eMMC command if STB_CTL bit is set to high. Otherwise, it is not used	1'b1
5:0	R/W	HIF_CMD_IDX	This register specifies the value of the SD/eMMC command index	6'h0

Table 100: HIF_CMD_ARGQ (0x5003_0018)

Bit	Mode	Symbol	Description	Reset
31:0	R	HCLK_CMD_ARG	This register is a queue to receive the value of the SD/eMMC command argument register when the trigger (transfer) operation is active	32'h0

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Table 101: HIF_CMD_IDXQ (0x5003_001C)

Bit	Mode	Symbol	Description	Reset
31:16	-	-	Reserved	
15	R	QBUSY_ST	Busy status of the current command queue 0: completed 1: ongoing	1'b0
14	R	CMD_TCTLQ	Command Trigger Control Queue 0: Start a new command immediately when the command trigger (CMDQ_TRIG) bit was set 1: Only start a new command when the command trigger (CMDQ_TRIG) bit was set and the previous response result has been read	1'b0
13:12	R	RSP_TYPEQ	Response Type Control Queue 0x: No Response 10: Short Response (Total: 48 bits) 11: Long Response (Total: 136 bits)	2'b00
11	R	STB_CTL	Command Start Bit and Transmission Bit Control Queue 0: The start bit and transmission bit of the SD/eMMC command is automatically generated by H/W circuit 1: The start bit and transmission bit of the SD/eMMC command refers to the STR_BIT and TRM_BIT of this control register	1'b0
10:8	R	DATA_TYPEQ	Data Type Control Queue 0xx: Command only (without data transfer) 100: Command with single read data 101: Command with multiple read data 110: Command with single write data 111: Command with multiple write data	3'b000
7	R	STR_NITQ	This register specifies the value of the start bit of SD/eMMC command if STB_CTL bit is set to high. Otherwise, it is not used	1'b0
6	R	TRM_BITQ	This register specifies the value of the transmission bit of SD/eMMC command if STB_CTL bit is set to high. Otherwise, it is not used	1'b1
5:0	R	HIF_CMD_IDXQ	This register specifies the value of the SD/eMMC command index	6'h0

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Table 102: HIF_PAD_CTRL (0x5003_0020)

Bit	Mode	Symbol	Description	Reset
31:30	-	-	Reserved	
29:28	R/W	HCOE_DLY	Output Enable Delay Control for Host Command signal 00: No delay 01: 1-unit delay 10: 2-unit delay 11: 3-unit delay	2'b00
27:26	R/W	HCO_DLY	Output Delay Control for Host Command signal 00: No delay 01: 1-unit delay 10: 2-unit delay 11: 3-unit delay	2'b00
25:24	R/W	HCI_DLY	Input Delay Control for Host Command signal 00: No delay 01: 1-unit delay 10: 2-unit delay 11: 3-unit delay	2'b00
23:22	R/W	HDATI_ST	Input Schmitt Trigger Level Control for Host Data signals	2'b00
21:20	R/W	HDAT_PUD	Host Data signals Pull-Up/Down Control 00: No Pull-Up/Down 01: Pull-Down 10: Pull-Up 11: Keeper	2'b00
19:16	R/W	HDATO_DS	Output Drive Strength Control for Host Data Signals	2'b00
15:14	R/W	HCMDI_ST	Input Schmitt Trigger Level Control for Host Data signals	2'b00
13:12	R/W	HDAT_PUD	Host Command signals Pull-Up/Down Control 00: No Pull-Up/Down 01: Pull-Down 10: Pull-Up 11: Keeper	2'b00
11:8	R/W	HCMDO_DS	Output Drive Strength Control for Host Command Signals	4'h0
7:6	-	-	Reserved	
5:4	R/W	HCLK_PUDC	Host Clock signals Pull-Up/Down Control 00: No Pull-Up/Down 01: Pull-Down 10: Pull-Up 11: Keeper	2'b00
3:0	R/W	HCLK_DS	Host Clock Control Count Register Output Drive Strength Control for Host Clock Signals	4'h0

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Table 103: HIF_BLK_LG (0x5003_0024)

Bit	Mode	Symbol	Description	Reset
31:28	-	-	Reserved	
27:16	R/W	HIF_BLK_LG	Block Length Register This register specifies the length (unit: byte) of each block for read/write data transfer	8'h0
15:6	-	-	Reserved	
5:4	R/W	HDOE_DLY	Output Enable Delay Control for Host Data signals 00: No delay 01: 1-unit delay 10: 2-unit delay 11: 3-unit delay	2'b00
3:2	R/W	HDO_DLY	Output Delay Control for Host Data signals 00: No delay 01: 1-unit delay 10: 2-unit delay 11: 3-unit delay	2'b00
1:0	R/W	HDI_DLY	Input Delay Control for Host Data signals 00: No delay 01: 1-unit delay 10: 2-unit delay 11: 3-unit delay	2'b00

Table 104: HIF_BLK_CNT (0x5003_0028)

Bit	Mode	Symbol	Description	Reset
31:24	-	-	Reserved	
23:0	R/W	HIF_BLK_CNT	Block Count Register	24'h0

Table 105: HIF_RSP_TMO_CNT (0x5003_0030)

Bit	Mode	Symbol	Description	Reset
31:8	-	-	Reserved	
7:0	R/W	RSP_TMO_CNT	This register specifies the number of host clock cycles for the response time-out interrupt. If the host cannot receive the response, it does not return to the host before the specified clock cycles	8'h40

Table 106: HIF_RD_TMO_CNT (0x5003_0034)

Bit	Mode	Symbol	Description	Reset
31:0	R/W	RD_TMO_CNT	Read Data Time-Out Count Register This register specifies the number of host clock cycles for the read data time-out interrupt if the read data does not return to the host before the specified clock cycles	8'h0040_0000

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Table 107: HIF_WB_TMO_CNT (0x5003_0038)

Bit	Mode	Symbol	Description	Reset
31:0	R/W	WB_TMO_CNT	Read Data Time-Out Count Register This register specifies the number of host clock cycles for the read data time-out interrupt if the read data does not return to the host before the specified clock cycles	32'h0A00_0000

Table 108: HIF_RSP_CIX_ST (0x5003_003C)

Bit	Mode	Symbol	Description	Reset
31:8	-	-	Reserved	
7	R	RSP_STR_B	Status of the Start bit of the received response R2 Response: RSP[135] Other Responses: RSP[47]	1'b0
6	R	RSP_DIR_B	Status of the Direction (Transmission) bit of the received response R2 Response: RSP[134] Other Responses: RSP[46]	1'b0
5:0	R	RSP_CMD_IDX	Status of the Command Index of the received response R2 Response: RSP[133:128] Other Responses: RSP[45:40]	6'h0

Table 109: HIF_RSP_ARG_0 (0x5003_0040)

Bit	Mode	Symbol	Description	Reset
31:0	R	RSP_ARG_0	Status of the received response argument-0 R2 Response: RSP[127:96] Other Responses: RSP[39:8]	32'h00

Table 110: HIF_RSP_ARG_1 (0x5003_0044)

Bit	Mode	Symbol	Description	Reset
31:0	R	RSP_ARG_1	Status of the received response argument-1 R2 Response: RSP[95:64] Other Responses: Reserved	32'h00

Table 111: HIF_RSP_ARG_2 (0x5003_0048)

Bit	Mode	Symbol	Description	Reset
31:0	R	RSP_ARG_2	Status of the received response argument-2 R2 Response: RSP[63:32] Other Responses: Reserved	32'h00

Table 112: HIF_RSP_ARG_3 (0x5003_004C)

Bit	Mode	Symbol	Description	Reset
31:0	R	RSP_ARG_3	Status of the received response argument-3 R2 Response: RSP[31:0] Other Responses: Reserved	32'h00

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Table 113: HIF_AHB_SA (0x5003_0050)

Bit	Mode	Symbol	Description	Reset
31:0	R	HIF_AHB_SA	This register specifies the start address of AHB bus for data transfer	32'h00

Table 114: HIF_AHB_EA (0x5003_0054)

Bit	Mode	Symbol	Description	Reset
31:0	R	HIF_AHB_EA	This register specifies the end address of AHB bus for data transfer	32'h00

Table 115: HIF_BUS_ST (0x5003_0060)

Bit	Mode	Symbol	Description	Reset
31:8	-	-	Reserved	
7	R/W	RSP_RET_ST	Receive the response from the device 0: Not receive 1: Receive	1'b0
6	R	CMD_BUSY	CMD/RSP Status Machine Busy Status 0: Not ongoing command/response (Idle) 1: Have ongoing command/response (Busy)	1'b0
5	R	DAT_BUSY	Data Status Machine Busy Status 0: Not ongoing data transfer (Idle) 1: Have ongoing data transfer (Busy)	1'b0
4	R	HCMD_ST	Status of Host Interface CMD signal	1'b0
3:0	R	RSP_CMD_IDX	Status of Host Interface Data signals	4'h0

Table 116: HIF_SM_ST (0x5003_0064)

Bit	Mode	Symbol	Description	Reset
31:16	R	HIF_DAT_CNT	Data Count Status	16'h0
15:13	-	-	Reserved	
12:8	R	HIF_DAT_SM	Data State Machine Status	5'h0
7:5	-	-	Reserved	
4:0	R	HIF_CMD_SM	CMD/RSP State Machine Status	5'h0

Table 117: HIF_XTR_CNT (0x5003_0068)

Bit	Mode	Symbol	Description	Reset
31:24	-	-	Reserved	
23:0	R	RSP_TMO_CNT	Transferred Data Block Count Status This register reports the number of the transferred data blocks. The value of this counter will be cleared after a new read/write command has been sent	24'h00

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Table 118: HIF_ERR_CNT (0x5003_006C)

Bit	Mode	Symbol	Description	Reset
31:25	-	-	Reserved	
24	R/W	ERR_CNT_FG	Error Count Flag Read: 0: No data CRC error 1: Data CRC error (Read CRC error or Non-positive Write CRC status token) Write: Clear the error count flag for allowing to record the data error block count 0: No effect 1: Clear the error count flag for allowing to record the data error block count when the data CRC error was occurred	1'b0
23:0	R	HIF_ERR_CNT	ERR Data Block Count Status This register recorded the number of the error data blocks. When the first data error occurred (Read CRC error or received the non-Positive Write CRC Status Token) during the read/write data transfer, the value of the transferred data block count will be recorded into this register. S/W needs to write “1” into the CLE_ERR_CNT bit to clear the internal flag that it controls, to record the error block count or not when the data error was occurred	24'h00

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4.5 SPI and I2C Register

DA16200 includes I2C master and slave functions. Four ranges of clock speed are supported: standard (100 kHz), fast (400 kHz), fast plus (1.0 MHz) and High Speed (3.4 MHz) mode for both Master and Slave mode.

DA16200 also supports SPI master and Slave functions. To use DA16200 as an SPI master, the CSB signal can be used with any of the GPIO pins. CSB [3:1] can be selected from the GPIO special function by setting the registers in the GPIO.

The SPI slave interface supports that an external host can control the DA16200. The range of the SPI clock speed is the same as that of the internal bus clock speed. There is a separate communication protocol for SPI slave. See section 9.3 SPI slave in the DA16200 datasheet [2] for more detailed information.

Table 119: SPI and I2C Registers Overview

Address	Register	Description
Common control for SPI and I2C Pin Status		
0x5008_023C	SPI_INTR_STATUS_REG	SPI Interrupt Status Register
0x5008_0240	SPI_CTRL_REG	SPI Control Register
0x5008_0244	I2C_CTRL_REG	I2C Control Register
0x5008_0248	SPI_LENGTH_REG	SPI Length Register
0x5008_024C	I2C_BUFFER_ADDR_REG	I2C Buffer Address Register
0x5008_0250	SPI_BASE_ADDR_REG	SPI Base Address Register
0x5008_0254	CMD_ADDR_REG	Command Address Register
0x5008_0258	RESP_ADDR1_REG	Response Address1 Register
0x5008_025C	RESP_ADDR2_REG	Response Address2 Register
0x5008_0260	AT_CMD_BASE_REG	AT Command Base Address Register
0x5008_0264	AT_CMD_REF_REG	AT Command Base Address Register
0x5008_0264	SPI_TIMER_REG	SPI Timer Register

Table 120: SPI_INTR_STATUS_REG (0x5008_023C)

Bit	Mode	Symbol	Description	Reset
15:13	R/W	INTR	SPI slave interrupt status register bit[15]: Command interrupt status/clear bit[14]: AT Command interrupt status/clear bit[13]: Processing end interrupt status/clear	0x0
12:0	R/W	-	Reserved	0x000

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Table 121: SPI_CTRL_REG (0x5008_0240)

Bit	Mode	Symbol	Description	Reset
15	R/W	CmdIntr	Command interrupt enable 1: Enable 0: Disable	1'b0
14	R/W	ATIntr	AT Command interrupt enable 1: Enable 0: Disable	1'b0
13	R/W	PEIntr	Processing end interrupt enable 1: Enable 0: Disable	1'b0
12	R/W	Prot	Protocol mode 1: 8-byte 0: 4-byte (default)	1'b0
11	R/W	SW_Rst	SPI block software reset 1: Normal 0: Reset state	1'b1
10	R/W		MISO Output mode selection 1: Normal 0: Half Pre output	1'b1
9	R/W	-	Reserved	1'b0
8	R/W	Endian	Endian mode for Data	1'b1
7:6	R/W	MODE	Define the SPI mode (CPOL, CPHA) 0: new data on falling, capture on rising, Clk low in idle state 1: new data on rising, capture on falling, Clk low in idle state 2: new data on rising, capture on falling, Clk high in idle state 3: new data on falling, capture on rising, Clk high in idle state	2'b00
5:4	R/W	ChipID		2'b00
3:2	R/W	DBusW	Data bus width 00 = 8-bit 01 = 16-bit 10 = 32-bit (default) 11 = not used	2'b10
1:0	R/W	ABusW	Address bus width 00 = 8-bit 01 = 16-bit 10 = 24-bit 11 = 32-bit (default)	2'b11

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Table 122: I2C_CTRL_REG (0x5008_0244)

Bit	Mode	Symbol	Description	Reset
7	R/W	SW_Rst	I2C block software reset 1: Normal 0: Reset state	1'b0
6	R/W	Endian	Endian mode for Data	1'b1
5:4	R/W	ChipID	Device ID for lower 2-bit	2'b00
3:2	R/W	DBusW	Data bus width 00 = 8-bit 01 = 16-bit 10 = 32-bit (default) 11 = not used	2'b10
1:0	R/W	ABusW	Address bus width 00 = 8-bit 01 = 16-bit 10 = 24-bit 11 = 32-bit (default)	2'b11

Table 123: SPI_LENGTH_REG (0x5008_0248)

Bit	Mode	Symbol	Description	Reset
23:0	R/W	Length	SPI reference length at read access	0x0100

Table 124: I2C_BUFFER_ADDR_REG (0x5008_024C)

Bit	Mode	Symbol	Description	Reset
31:0	R/W	Length	I2C buffer address	0x0000

Table 125: SPI_BASE_ADDR_REG (0x5008_0250)

Bit	Mode	Symbol	Description	Reset
15:0	R/W	BaseAddr	When SPI protocol 4-byte is set Upper 2-byte Address value is written in this field	0x0000

Table 126: CMD_ADDR_REG (0x5008_0254)

Bit	Mode	Symbol	Description	Reset
31:0	R/W	CmdAddr	Write/Read Request If accessed, internal interrupt should be generated	0x0000

Table 127: RESP_ADDR1_REG (0x5008_0258)

Bit	Mode	Symbol	Description	Reset
31:0	R/W	RespAddr	Response register #1	0x0000

Table 128: RESP_ADDR2_REG (0x5008_025C)

Bit	Mode	Symbol	Description	Reset
31:0	R/W	RespAddr	Response register #2	0x0000

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Table 129: AT_CMD_BASE_REG (0x5008_0260)

Bit	Mode	Symbol	Description	Reset
31:0	R/W	ATCmd	AT command base address Indicates the AT command reference register	0x0000

Table 130: AT_CMD_REF_REG (0x5008_0264)

Bit	Mode	Symbol	Description	Reset
31:0	R/W	ATCmd	AT command reference register Indicates the SRAM address that external AP will access	0x0000

Table 131: SPI_TIMER_REG (0x5008_0268)

Bit	Mode	Symbol	Description	Reset
31:0	R/W	Timer	Optional	0x1000

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4.6 RTC Register

DA16200 provides RTC functions. Clock source for RTC can be selected with a register between 32 KHz OSC and 32 KHz XTAL. There is a 36-bits free-running counter in the RTC block making it a reference time. RTC block controls sleep and wake up operation of DA16200. And it also controls internal power on/off for each HW blocks.

Table 132: RTC Register Overview

Address	Registers	Description
0x50091000	wakeup_counter0	Wakeup counter [31:0]
0x50091004	wakeup_counter1	Wakeup counter [35:32]
0x50091008	gpio_wakeup_config	Wakeup by GPIO config register
0x5009100C	gpio_wakeup_control	Wakeup by GPIO control register
0x50091010	rtc_control	RTC control register
0x50091014	xtal_control	32 kHz XTAL control register
0x50091018	retention_control	Retention memory power control register
0x5009101C	dc_power_control	DCDC control register
0x50091020	ldo_control	Control LDOs
0x50091024	reserved	Reserved
0x50091028	wakeup_source	Wake up source
0x5009102C	reserved	Reserved
0x50091030	AO indicator	Indicate retention memory contents
0x50091034	reserved	Reserved
0x50091038	counter0	Real time counter [31:0]
0x5009103C	counter1	Real time counter [35:32]
0x50091040	ldo_status	LDO status register
0x50091044	ldo_pwr_control	uLDO control register
0x50091048	reserved	Reserved
0x5009104C	bor_circuit	Brown and Black out control register
0x50091050	reserved	Reserved
0x50091054	reserved	Reserved
0x50091058	reserved	Reserved
0x5009105C	watchdog_cnt	RTC watch dog counter

Table 133: wakeup_counter0 (0x50091000)

Bit	Mode	Symbol	Description	Reset
31:0	R/W		Set to RTC timer value which is expected to wakeup	0x00000000

Table 134: wakeup_counter1 (0x50091004)

Bit	Mode	Symbol	Description	Reset
3:0	R/W		Set to RTC timer value which is expected to wakeup	0x0

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Table 135: gpio_wakeup_config (0x50091008)

Bit	Mode	Symbol	Description	Reset
25:16	R/W		Wake-up source selection. (Note 1) [16] 0: GPIOA4 1: GPIOC0 [17] 0: GPIOA5 1: GPIOC1 [18] 0: GPIOA6 1: GPIOC2 [19] 0: GPIOA7 1: GPIOC3 [20] 0: GPIOA8 1: GPIOC4 [21] 0: GPIOA9 1: GPIOC6 [22] 0: GPIOA10 1: GPIOC7 [23] 0: GPIOA11 1: GPIOC8 [24] 0: GPIOC5 1: GPIOA12 [25] 0: GPIOA13 1: GPIOA14	0x000
12:10	R/W	-	Edge selection of RTC_WAKEUP2/3/4 (Note 2). [12] RTC_WKAEUP4 [11] RTC_WAKEUP3 [10] RTC_WAKEUP2 0: rising edge 1: falling edge	0x0
9:0	R/W	-	edge sel: selected signal by [25:16] 0: rising edge 1: falling edge	0x000

Note 1 GPIOA[11:0] and GPIOC[8:6] can be used in 6x6.

Note 2 RTC_WAKEUP and RTC_WAKEUP2 can be used in 6x6.

Table 136: gpio_wakeup_control (0x5009100C)

Bit	Mode	Symbol	Description	Reset
28:26	R/W	-	Wakeup enable (Note 1). [28] RTC_WAKEUP4 [27] RTC_WAKEUP3 [26] RTC_WAKEUP2 0: wakeup disable 1: wakeup enable	0x0
25:16	R/W	-	Wakeup enable of selected signal by gpio_wakeup_config[25:16] 0: wakeup disable 1: wakeup enable	0x000
13:10	R	-	Indicate wake up source [13] RTC_WAKEUP4 [12] RTC_WAKEUP3 [11] RTC_WAKEUP2 [10] RTC_WAKE_UP 1: indicates wake up from that port	0x0
9:0	R	-	Indicate GPIO wakeup source 9:0 1: indicates wakeup from that port	0x000

Note 1 RTC_WAKEUP and RTC_WAKEUP2 can be used in 6x6.

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Table 137: rtc_control (0x50091010)

Bit	Mode	Symbol	Description	Reset
6	R/W	-	Wakeup enable for RTC_WAKEUP 0: wakeup disable 1: wakeup enable	1'b0
5	R/W	-	Brown out interrupt enable field 0: no interrupt will be enabled 1: when event, IRQ will be generated	1'b0
4	R/W	-	Black out interrupt enable field 0: no interrupt will be enabled 1: when event, IRQ will be generated	1'b0
3	R/W	-	RTC Watch-Dog Count 0: count disable 1: count enable	1'b0
2	R/W	-	RTC_WAKEUP input polarity selection 0: rising edge 1: falling edge	1'b0
1	R/W	-	RTC_WAKEUP interrupt enable (Normal mode) 0: no interrupt will be enabled 1: when event, IRQ will be generated	1'b0
0	R/W	-	Power down enable 0: no effect 1: go to power down mode	1'b0

Table 138: xtal_control (0x50091014)

Bit	Mode	Symbol	Description	Reset
10	R/W	-	VBAT BIAS current control (0: max current, 1: min current)	1'b0
9:8	R/W	-	XTAL LDO current control (0: max current, 3: min current)	2'b00
7:5	R/W	-	40M XTAL LDO output voltage control	3'b100
4	R/W	-	EN_XR_BAT External resistor enable 0: Internal resistor used 1: External resistor used	1'b0
3:2	R/W	-	CLK_SEL1:0 Select clock source (default 32 kHz OSC) 0: 32 kHz OSC 1: 32 kHz Crystal 2: for Test	2'b00
1	R/W	-	EN_XTAL_BAT 32 kHz Crystal Power on/off (default:1) (0: off, 1: on)	1'b1
0	R/W	-	PDB_OSC 32 kHz Oscillator Power on/off (default:1) (0: off, 1: on)	1'b1

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Table 139: retention_control (0x50091018)

Bit	Mode	Symbol	Description	Reset
27:24	R/W	-	GPIO retention control bit [27] FDIO region [26] GPIOC [25] GPIOA [24] reserved 0: disable 1: enable	4'b0000
22:16	R/W	-	RET_RET[6:0] Retention memory Retention mode enable 0: disable 1: enable	7'b0000000
14:8	R/W	-	RET_SLR[6:0] Retention memory Sleep mode enable (when memory sleep, Memory's content will be lost) 0: disable 1: enable	7'b0000000
7:4	R/W	-	Power down information	4'b0000
2	R/W	-	PDB_ISO_shared_io (GPIOA0~3) 0: isolation enable, cannot access to GPIOA0~3 1: isolation disable, access to GPIOA0~3	1'b1
1	R/W	-	RTM_INFORM	1'b0
0	R/W	-	PDB_ISO default 0 1: Isolation disable, access to Retention Memory 0: Isolation enable, cannot access to Retention Memory	1'b0

Table 140: dc_power_control (0x5009101C)

Bit	Mode	Symbol	Description	Reset
1	R/W	-	Auto Power On Enable 0: no effect 1: when set to “1”, go to sleep and wake up automatically, all register values will be reset value.	1'b0
0	R/W	-	DCDC1.2 power off 0: no effect 1: when set “1”, DCDC1.2 Off	1'b0

Table 141: ldo_control (0x50091020)

Bit	Mode	Symbol	Description	Reset
9	R/W	-	PDB_IP1_LDO (IQADC/DAC power control) 0: IP1 LDO power off 1: IP1 LDO power on	1'b0
8	R/W	-	PDB_RF_LDO 0: RF LDO power off 1: RF LDO power on	1'b0

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Bit	Mode	Symbol	Description	Reset
7	R/W	-	DIG_LDO_CNTL (to IP4 block) 0: DIG LDO power off 1: DIG LDO power on	1'b1
6	R/W	-	DCDC_CNTL_XTAL (to RF block) 0: DIG LDO power off 1: DIG LDO power on	1'b1
5	R/W	-	PDB_uLDO for retention memory power supply LDO control 0: LDO off 1: LDO on	1'b0
4	R/W	-	PDB_IP3_OTP: OTP power switch 0: OTP block power off 1: OTP block power on	1'b1
3	R/W	-	OTP_PWRPRDY: indicates OTP power stable 0: OTP block power is not ready 1: OTP block power is stable	1'b1
2	R/W	-	LDO_PLL1: for PLL power 0: PLL LDO off 1: PLL LDO on	1'b0
1		-	Reserved	
0	R/W	-	PDB_XTAL_NOISE_REDU: XTAL noise reduction circuit 0: no effect 1: noise reduction circuit on	1'b0

Table 142: wakeup_source (0x50091028)

Bit	Mode	Symbol	Description	Reset
11:8	R	-	ADC Sensor Wakeup status: indicates ADC wakeup source pin [11]: Sensor Wakeup GPIOA3 [10]: Sensor Wakeup GPIOA2 [9]: Sensor Wakeup GPIOA1 [8]: Sensor Wakeup GPIOA0	4'h0
6	R/W	-	DWAKE source detect Read case: 1 indicates wakeup source from GPIOs Write case: 0: wait for event 1: source clear	1'b0
5	R/W	-	Pulse CNT detect Read case: 1 indicates wakeup source from pulse CNT function Write case: 0: wait for event 1: source clear	1'b0
4	R/W	-	Sensor (ADC) detect Read case: 1 indicates wakeup source from ADC sensor function	1'b0

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Bit	Mode	Symbol	Description	Reset
			Write case: 0: wait for event 1: source clear	
3	R/W	-	WatchDog detect Read case: 1 indicates wakeup source from RTC watch dog Write case: 0: wait for event 1: source clear	1'b0
2	R/W	-	POR indicator Read case: 1 indicates wakeup source from POR port Write case: 0: wait for event 1: source clear	1'b0
1	R/W	-	FRC compare detect Read case: 1 indicates wakeup from RTC count meet the wanted value Write case: 0: wait for event 1: source clear	1'b0
0	R/W	-	Ext Wakeup signal detect Read case: 1 indicates wakeup source from RTC_WAKEUPx pins Write case: 0: wait for event 1: source clear	1'b0

Table 143: AO indicator (0x50091030)

Bit	Mode	Symbol	Description	Reset
3	R/W	-	AO register restore enable (REM to AO) 0: no effect 1: indicates some contents are in retention memory which should be restored when wake up	1'b0
[2:0]			Reserved	3'b000

Table 144: counter0 (0x50091038)

Bit	Mode	Symbol	Description	Reset
31:0	R	-	RTC free running counter read value [31:0]	0x00

Table 145: counter1 (0x5009103C)

Bit	Mode	Symbol	Description	Reset
3:0	R	-	RTC free running counter read value [35:32]	0x00

Table 146: ldo_status (0x50091040)

Bit	Mode	Symbol	Description	Reset
13	R	-	IP1_LDO_RDY	1'b0

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Bit	Mode	Symbol	Description	Reset
			1: IP1_LDO is ready	
12	R	-	DCDC_RDY 1: DCDC is ready	1'b0
11	R	-	F_LDO_RDY 1: Flash LDO is ready	1'b0
10	R	-	DIG_LDO_RDY 1: DIG LDO is ready	1'b0
9	R	-	RF_LDO_RDY 1: RF LDO is ready	1'b0
8	R	-	XTAL40M_RDY 1: XTAL 40 Mhz clock is ready	1'b0
7	R	-	Reserved	
6	R	-	Reserved	
5	R	-	Reserved	
4	R	-	Reserved	
3	R	-	XTAL_RDY 1: XTAL 32 Khz is ready	1'b0
2	R	-	Reserved	
1	R	-	Reserved	
0	R	-	Wake up source from RTC_WAKEUP pin	1'b0

Table 147: ldo_pwr_control (0x50091044)

Bit	Mode	Symbol	Description	Reset
29	R/W	-	DCDC_ST_BYP 0: soft start bypass disable 1: soft start bypass enable	1'b0
28:24	R/W	-	DCDC_ST_CTRL[4:0] DCDC soft start timing control delay time	5'b01011
21	R/W	-	IP2_MON_PATH_CTRL 0: LDO and low frequency path 1: RF clock path	1'b0
20:18	R/W	-	IP2_MON_CTRL For testing purpose	3'b0
17:16	R/W	-	RTC_XTAL32K_GM XTAL 32 Khz gain control	2'b11
15:14	R/W	-	RTC_OSC32K_ICTRL Osc32K sleep current control, 00: min ~ 11: max	2'h0
13:12	R/W	-	RTC_XTAL32K_ICTRL Xtal32K sleep current control, 00: min ~ 11: max	2'b01
11:10	R/W	-	RTC_uLDO_LICTRL uLDO sleep current control, 00: min~ 11: max	2'b01
9:8	R/W	-	RTC_uLDO_HICTRL uLDO speed up control	2'b11

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Bit	Mode	Symbol	Description	Reset
			00 low speed 11 high speed	
7:4	R/W	-	RTC_uLDO_VCTRL: uLDO output voltage control 4'b0001 (1.12V) ~ 4'b1111 (0.8V)	4'b0001
1	R/W	-	PDB_TEST_BUF: IP2 test buffer enable	1'b0
0	R/W	-	RTC clock inversion: for test purpose 0: bypass 1: inversion	1'b0

Table 148: bor_circuit (0x5009104C)

Bit	Mode	Symbol	Description	Reset
14	R	-	BR status read 1: Brown Out event occurred	
13	R	-	BL status read 1: Black Out event occurred	
12	R/W	-	BR_HYS_CTRL 0: hysteresis 100 mV (Default) 1: hysteresis 150 mV	1'b0
11	R/W	-	BL_HYS_CTRL 0: hysteresis 100 mV (Default) 1: hysteresis 150 mV	1'b0
10	R/W	-	reserved	1'b0
9	R/W	-	BR_OUT_EN (brown out) 0: BR logic disable 1: BR logic enable	1'b0
8	R/W	-	BL_OUT_EN (black out) 0: BL logic disable 1: BL logic enable	1'b0
7:4	R/W	-	BR_OUT_CTRL	4'b0111
3:0	R/W	-	BL_OUT_CTRL	4'b0101

Table 149: watchdog_cnt (0x5009105C)

Bit	Mode	Symbol	Description	Reset
6:5	R	-	WatchDog Count read value	
4:0	R/W	-	Free Running Counter[35:14] bit selection	0x00

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4.7 External Interrupt Control Register

External interrupt signal in GPIO Alternative function (see bit[4] in the Table 29) can be configured and set with this register.

Table 150: External Interrupt Control Register Overview

Address	Registers	Description
0x50001200	EXT_INTB_CTRL	External Interrupt Control [7:0]
0x50001204	EXT_INTB_SET	External Interrupt Set [0]

Table 151: EXT_INTB_CTRL (0x50001200)

Bit	Mode	Symbol	Description	Reset
7:2	R/W	-	Pulse duration. (unit: 256 CPU clocks.) Valid when edge mode.	6'b100000
1	R/W	-	Interrupt mode 0: level mode 1: edge mode	1'b0
0	R/W		Interrupt Polarity 0: low active 1: high active	1'b0

Table 152: EXT_INTB_SET (0x50001204)

Bit	Mode	Symbol	Description	Reset
0	R/W	-	external interrupt set register. When level mode, set '1' for trigger and '0' for clear. When edge mode, just set '1' and will be cleared automatically after pulse width.	1'b0

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Revision History

Revision	Date	Description
1.3	25-Mar-2022	Update logo, disclaimer, copyright.
1.2	31-Mar-2021	Editorial + 4.7 External Interrupt Control Register
1.1	27-Jan-2021	Table 90 and Table 91 Changed description.
1.0	19-Nov-2020	First Release.

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DA16200 Registers Map for Peripherals

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