Summary

This application note describes an operation example using Single Edge Nibble Transmission (RSENT) of RH850/E2x.

Although the operation example written in this application note was checked in software, be sure to check your operating environment when you use it.
# Table of Contents

1. Introduction .................................................................................................................. 3  
   1.1 Functionality to Be Used ......................................................................................... 3  
   1.2 Functional Overview of RSENT ............................................................................... 3  
   1.3 Communication Format ......................................................................................... 3  

2. Operation Example of RSENT ..................................................................................... 4  
   2.1 Specification Overview ............................................................................................. 4  
   2.2 System Configuration .............................................................................................. 4  
   2.3 Software Description ............................................................................................... 4
1. Introduction

This application note describes the usage of Single Edge Nibble Transmission (RSENT) of RH850/E2x and provides its sample software.

1.1 Functionality to Be Used

RH850/E2x hardware functionality used in this application note is shown below:

- Single Edge Nibble Transmission (RSENT)

1.2 Functional Overview of RSENT

The RSENT interface supports the following functions defined by the standard specification SAE J2716_201604:

- Triple speed expansion tick time: Clock cycle (1 μs to 90 μs)
- Variable data transmission rate
  - 24.7 kbps to 64.9 kbps: Based on 6 nibble data at 3 μs clock rate
  - 74.1 kbps to 194.7 kbps: Based on 6 nibble data at 1 μs clock rate
- Unidirectional communication: Between a sensor and the MCU
- Bidirectional communication: Between a sensor and the MCU (supported in SPC mode)
- Single edge data transmission: Coded by the temporal distance of two serially-detected falling edges on a data line
- Transmission frame with up to 8 data nibbles + status / communication nibbles
- Data transmission protected with CRC is available
- Calibration phrase in each data frame
- 1-wire interface
- Multiple sensors can be connected to each RSENT channel that has the standard expansion function
- Received data from sensors is detected by software or DMA
- Timestamp function is supported: Master mode can only be set for RSENT0. Slave mode alone can be set for other RSENT modules.

1.3 Communication Format

Figure 1-1 shows the communication format used in this operation example.

- 6 data nibbles
- Pause pulse absent
- 1 tick = 3 μs

![Figure 1-1 Communication Format](image-url)
2. Operation Example of RSENT

2.1 Specification Overview
This section describes a receive operation using RSENT0.

Assign the P02_8 pin to RSENT0RX, enable a receive interrupt and operation, and store the receive data in variables in the receive interrupt.

![Receive Operation Diagram](image)

Figure 2-1 Receive Operation

2.2 System Configuration
Figure 2-2 shows the system configuration.

![System Configuration Diagram](image)

Figure 2-2 System Configuration

2.3 Software Description
- Module description
The list of modules in this operation example is shown below:

<table>
<thead>
<tr>
<th>Module name</th>
<th>Label name</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>Main routine</td>
<td>main_pe0</td>
<td>Performs various settings and starts applications.</td>
</tr>
<tr>
<td>RSENT initialization routine</td>
<td>rsent_init</td>
<td>Performs RSENT0 initial settings.</td>
</tr>
<tr>
<td>Interrupt initialization routine</td>
<td>inic_init</td>
<td>Performs interrupt function initial settings.</td>
</tr>
<tr>
<td>Port initialization routine</td>
<td>port_init</td>
<td>Performs port initial settings.</td>
</tr>
<tr>
<td>Interrupt processing routine</td>
<td>rsent0_int</td>
<td>An interrupt function which stores the receive data in variables.</td>
</tr>
</tbody>
</table>
- Register settings

The register settings of each function in this operation example are shown below:

**Table 2-2**  RSENT0 Register Settings

<table>
<thead>
<tr>
<th>Register name</th>
<th>Set value</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>MSR_KCPROT</td>
<td>0xA5A5A501</td>
<td>Module standby register: To enable write access to protected registers</td>
</tr>
<tr>
<td></td>
<td>0xA5A5A500</td>
<td>Module standby register: To disable write access to protected registers</td>
</tr>
<tr>
<td>MSR_RSENT</td>
<td>0xFFFFFFFE</td>
<td>Puts RSENT0 in operating mode.</td>
</tr>
<tr>
<td>RSENT0MDC</td>
<td>0x00000001↓</td>
<td>Changes RSENT0 to CONFIGURATION mode</td>
</tr>
<tr>
<td></td>
<td>0x00000005</td>
<td>Changes RSENT0 to OPERATION ACTIVE mode</td>
</tr>
<tr>
<td>RSENT0CC</td>
<td>0x0000064A</td>
<td>Slow channel CRC check: Disabled</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Fast channel CRC check: Disabled</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Serial message format: Short serial message format</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Pause pulse configuration: Pause pulse absent</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Number of data nibbles: 6 data nibbles</td>
</tr>
<tr>
<td>RSENT0BRP</td>
<td>0x00020401</td>
<td>Time tick integer: 3 μs</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Sample clock division value: 5</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Sample clock multiplication value: 2</td>
</tr>
<tr>
<td>RSENT0IDE</td>
<td>0x00000001</td>
<td>Fast channel receive interrupt enable: Interrupt enabled</td>
</tr>
</tbody>
</table>

**Table 2-3**  Interrupt Register Settings

<table>
<thead>
<tr>
<th>Register name</th>
<th>Set value</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>EIBD422</td>
<td>0x00000000</td>
<td>Interrupts are bound to PE0 (CPU0).</td>
</tr>
<tr>
<td>EIC422</td>
<td>0x0040</td>
<td>Table reference method / Priority level 0</td>
</tr>
</tbody>
</table>

**Table 2-4**  Port Register Settings

<table>
<thead>
<tr>
<th>Register name</th>
<th>Set value</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>PKC_CPROT</td>
<td>0xA5A5A501</td>
<td>Enables write access of the PWE (Port Write Enable) register.</td>
</tr>
<tr>
<td></td>
<td>0xA5A5A500</td>
<td>Disables write access of the PWE (Port Write Enable) register.</td>
</tr>
<tr>
<td>PWE</td>
<td>0x00000004</td>
<td>Enables write access for port group P02 registers.</td>
</tr>
<tr>
<td></td>
<td>0x00000000</td>
<td>Disables write access for port group P02 registers.</td>
</tr>
<tr>
<td>PCR02_8</td>
<td>0x00000054</td>
<td>P02_8: RSENT0RX</td>
</tr>
</tbody>
</table>
Operation flowchart
The operation flowchart of this operation example is shown below.

![Operation Flowchart](image-url)
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- Renesas Electronics Website
  http://japan.renesas.com/
- Contact
  http://japan.renesas.com/contact/

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<table>
<thead>
<tr>
<th>Rev.</th>
<th>Issued Date</th>
<th>Page</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.00</td>
<td>August 6, 2018</td>
<td>—</td>
<td>New Release</td>
</tr>
</tbody>
</table>
General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Handling of Unused Pins
   — Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.
   The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on
   — The state of the product is undefined at the moment when power is supplied.
   The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses
   — Access to reserved addresses is prohibited.
   The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals
   — After applying a reset, only release the reset line after the operating clock signal has become stable.
   When switching the clock signal during program execution, wait until the target clock signal has stabilized. When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products
   — Before changing from one product to another, i.e. to one with a different type number, confirm that the change will not lead to problems.
   The characteristics of MPU/MCU in the same group but having different type numbers may differ because of the differences in internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to products of different type numbers, implement a system-evaluation test for each of the products.
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(Rev.3.0-1 November 2016)