Summary

This document describes notes on using CADC in RH850/E2x-FCC1 or E2M.

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1. Usage Notes on CADC

1.1 Notes on Board Design

Figure 1 shows an example of a CADC circuit connection. Isolate digital and analog circuits as much as possible when you design a board layout. Also, make a best effort to avoid such a layout as signal lines of digital and analog circuits are intersected, or they are put in proximity to each other. Otherwise, induction may occur, leading to malfunction of analog circuits or a negative effect on A/D conversion values.

Never fail to separate an analog input pin, analog reference voltage (ADSVREFH and ADSVREFL), analog power supply (ADSVCC), and analog GND (ADSVSS) from digital circuits. Apply the same signal level for ADSVSS and ADSVREFL when they are connected to the board. Also, connect the analog GND (ADSVSS) to the on-board digital GND (VSS) only at one point.

1.2 Recommended Example of Capacitor Insertion

Figure 1 shows an example of capacitor insertion.

Note: There is no need of a trace to ADSVCL when your board does not incorporate DSADC.

C1: Preventive measures against surge and noise (0.1 uF)
Connect a protective capacitor (C1) between ADSVCC-ADSVSS, and between ADSVREFH-ADSVREFL to prevent analog input pins from being destroyed by abnormal voltage, such as an excessive surge. Put C1 as close as possible to the LSI for better denoising.

C2: Countermeasures against power supply stabilizing capacitor and mutual interference (10 to 100 uF)
Place a power supply stabilizing capacitor C2.
C3: Denoising of input pins (1 to 100 nF)
   Refer to Section 1.3 for C3 and Rext.

- Measures against full-scale errors
  Unstable ADSVREFH may lead to the deterioration of full-scale errors. Decrease the
  trace impedance of ADSVREFH or increase the ADSVREFH–ADSVREFL capacitance (C1)
  to improve the stability.

- Measures against offset errors
  Make such a pattern design as reduces and equalizes the impedance of traces between
  ADSVSS and the analog GND / ADSVREFL and the analog GND in order to make a
  potential difference between ADSVSS and ADSVREFL, the cause of offset errors, as
  small as possible.

1.3 Sampling Error by External Circuits

An analog input pin of the CADC has input impedance $R_i$ (Figure 2). When the resistance
value $R_{ext}$ of external circuits is large, the input signal is multiplied by $R_i/(R_{ext} + R_i)$ and a gain
error is generated, because the signal input to the CADC is divided between $R_{ext}$ and $R_i$. To
reduce the gain error, $R_{ext}$ should be as small as possible. Configure the cutoff frequency $F_c$
based on the signal frequency, since the anti-aliasing filter for the CADC input signal consists of
$R_{ext}$ and C3.

$$F_c = \frac{1}{2\pi R_{ext} C_3}$$

When $R_{ext}$ is set to 50 [Ω] and C3 to 4.7 [nF], the cutoff frequency will be 677 [kHz].
1.4 Notes on Using Pin for Both Analog and Digital Use

If the digital input/output signal is multiplexed to an analog input pin, the pin can be also used for general-purpose digital input/output. Changes in the level of the digital input/output signal during an A/D conversion may reduce the conversion accuracy. Noise from the operation of a digital pin near an analog input pin may also result in a negative effect on the conversion accuracy. Follow the following instructions so that the digital input/output pin will not have an adverse influence on the A/D conversion result:

Notes on analog input pins
(a) Place the capacitor of the RC circuit as close to the LSI pin as possible to prevent a negative effect on the conversion accuracy of an analog pin. Use your board to evaluate to what extent the accuracy is retained, since it depends on the board design.

Notes on digital pins near analog pins
(a) When a pin is not used for digital input, disable the digital input function of the pin by using port functions.
(b) Do not include overshoot or undershoot in the digital signal input to a digital input pin.
(c) To suppress the charge-discharge current, design your board so as to decrease the load capacitance connected to an output pin.
(d) When you use a digital pin, lower its output driving ability (drive strength) to avoid an adverse influence on an analog pin.
1.5 Configuration Example for Battery Voltage Input

When you directly input the battery voltage to an analog pin, make sure that the value is within the injection current limits $I_{\text{max}}$ and the pin voltage limits $V_{\text{max}}$. Otherwise, the value in the injection current that exceeds $I_{\text{max}}$ may increase the pin voltage, resulting in destruction of the MCU. When a high voltage is directly input to a pin, convert the voltage with a voltage divider not to exceed the limits of the injection current and the pin voltage, as shown in Figure 3, Analog Input Pin Configuration Example 1.

![Analog Input Pin Configuration Example 1](image)

Figure 3
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General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Handling of Unused Pins
   — Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.
   The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on
   — The state of the product is undefined at the moment when power is supplied.
   The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.
   In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses
   — Access to reserved addresses is prohibited.
   The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals
   — After applying a reset, only release the reset line after the operating clock signal has become stable.
   When switching the clock signal during program execution, wait until the target clock signal has stabilized. When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products
   — Before changing from one product to another, i.e. to one with a different type number, confirm that the change will not lead to problems.
   The characteristics of MPU/MCU in the same group but having different type numbers may differ because of the differences in internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to products of different type numbers, implement a system-evaluation test for each of the products.
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