### Introduction

**[Purpose]**

Making the best use of the video and display IP modules in third-generation R-Car series products and of the bandwidth of the system bus can achieve a flow of video data that brings out the maximum performance of third-generation R-Car series products.

To achieve this goal, this document describes concepts of deriving performance and bandwidth from each of the video and display IP modules along with concrete examples of their application, and gives sample calculations of bandwidth.

This document helps the user to examine how to implement the desired flows of video data through third-generation R-Car series products.

**[Target Readers]**

Readers of this document are assumed to have general knowledge in the fields and specific technologies listed below.

- Engineering, logic circuits, and microcontrollers.
- The functionality of the multiple processor cores of R-Car H3, R-Car M3-W, R-Car M3-N, R-Car E3, and R-Car D3 products.

**Target Devices**

- Version 2.0 and 3.0 of the R-Car H3
- Version 1.1 of the R-Car M3-W
- Version 1.x of the R-Car M3-N
- Version 1.x of the R-Car E3
- Version 1.x of the R-Car D3
Contents

1. Target LSIs .......................................................................................................................... 4

2. Positioning of This Document .......................................................................................... 5

3. Introduction ......................................................................................................................... 8
   3.1 Overview of Guidelines for Each IP Module .................................................................. 9
   3.2 QoS Settings and IP Processing Time ........................................................................... 10
   3.3 Summary — Procedure for Calculating Performance and Bandwidth of Each Video and Display IP Module ................................................................................................. 11

4. Upper Limits on Bus Bandwidths Related to Video and Display IP Modules .............. 12
   4.1 Third-generation R-Car Series Bus System and Upper Limits on Bandwidths .......... 12

5. Guidelines for Performance of the Video and Display IP Modules ............................ 22
   5.1 Terms Used in Guidelines .............................................................................................. 22
   5.2 Relationships between Data Types and Color Depths ................................................. 25
   5.3 VSPD and DU .................................................................................................................. 27
      5.3.1 A) Maximum Performance ...................................................................................... 27
      5.3.2 B) Concepts of Deriving Performance .................................................................. 33
      5.3.3 C) Concepts of Deriving Bandwidth ..................................................................... 34
      5.3.4 D) Example of Bandwidth Calculation .................................................................. 35
   5.4 VSPB and VSPBS ............................................................................................................. 36
      5.4.1 A) Maximum Performance ...................................................................................... 36
      5.4.2 B) Concepts of Deriving Performance .................................................................. 52
      5.4.3 C) Concepts of Deriving Bandwidth ..................................................................... 54
      5.4.4 D) Examples of Bandwidth Calculation .................................................................. 57
   5.5 VSPI .................................................................................................................................... 67
      5.5.1 A) Maximum Performance ...................................................................................... 67
      5.5.2 B) Concepts of Deriving Performance .................................................................. 72
      5.5.3 C) Concepts of Deriving Bandwidth ..................................................................... 74
      5.5.4 D) Example of Bandwidth Calculation .................................................................. 77
   5.6 VCP4 and iVDP1C ............................................................................................................. 86
      5.6.1 A) Maximum Performance ...................................................................................... 86
      5.6.2 B) Concepts of Deriving Performance .................................................................. 96
      5.6.3 C) Concepts of Deriving Bandwidth ..................................................................... 107
   5.7 CSI2 and VIN .................................................................................................................. 110
      5.7.1 A) Maximum Performance ...................................................................................... 110
      5.7.2 B) Concepts of Deriving Performance .................................................................. 120
      5.7.3 C) Concepts of Deriving Bandwidth ..................................................................... 125
      5.7.4 D) Example of Bandwidth Calculation .................................................................. 128
5.8  FDP ................................................................................................................................. 129  
5.8.1  A) Maximum Performance ......................................................................................... 129  
5.8.2  B) Concepts of Deriving Performance ........................................................................ 130  
5.8.3  C) Concepts of Deriving Bandwidth ............................................................................ 132  
5.8.4  D) Examples of Bandwidth Calculation ..................................................................... 135  
5.8.5  Usage Notes .................................................................................................................. 144  

6.  References .......................................................................................................................... 145
1. **Target LSIs**

2. Positioning of This Document

In third-generation R-Car series products, the bandwidth can be independently specified for each IP module, and bandwidth arbitration is controlled by the QoS controller. The user needs to determine the required bandwidth for each IP module when specifying parameters for QoS control.

Figure 2-1 shows the procedure for developing a system around a third-generation R-Car series product, including modification of the QoS parameter settings.

**Step 1:** Examine the use case considering the maximum performance and the upper limit of bandwidth of each IP module, and then determine the QoS parameters suitable for the use case.

**Step 2:** Specify the QoS parameters through the QoS driver.

**Steps 3 and 4:** Check that the use case works on the target system by using the bandwidth monitoring tool. Based on the results of this check on the target system, go back to step 1 to adjust QoS parameters.

This document is used to examine the use case in step 1; this describes concepts of calculating the maximum performance and bandwidth only for the IP modules used in the flow of video data, which occupies most of the bus bandwidth. Figure 2-2 gives an overview of step 1 (use case examination).
Figure 2-1 Procedure for Developing a System around a Third-Generation R-Car Series Product
Step 1 (use case examination) shown in Figure 2-1, Procedure for Developing a System around a Third-Generation R-Car Series Product, consists of two parts as shown in Figure 2-2. In part 1, specify the bandwidths for the video and display IP modules with reference to this application note.

Then, in part 2, enter the bandwidths for the video and display IP modules and the bandwidths for other IP modules in the QoS parameter setting sheet to generate the QoS parameter setting values. For part 2, refer to the Guide to Setting QoS Parameters.

Notes:
1. VSPD/DU, VSPB, VSPI, VCP4/iVDP1C, CSI2/VIN, and FDP
2. The descriptions in the application note “Flow of Video Data” are represented in the form of the bandwidth calculation sheet.

Figure 2-2  Overview of Step 1: Use Case Examination
3. Introduction

This application note summarizes the specifications regarding the performance of the IP modules related to the flow of video data. The IP modules related to the flow of video data are collectively called the video and display IP modules. Table 3-1 shows the video and display IP modules and the IP modules covered in this application note. The video and display IP modules not covered in this application note will be covered in the subsequent versions.

Table 3-1 Video and Display IP Modules and IP Modules Covered in This Application Note

<table>
<thead>
<tr>
<th>Video and Display IP Module</th>
<th>IP Module Covered in This Application Note</th>
</tr>
</thead>
<tbody>
<tr>
<td>VSPD/DU, VSPB/VSPBS, VSPI, VCP4/iVDP1C, CSI2/VIN, FDP, IMR, HDMI</td>
<td>VSPD/DU, VSPB/VSPBS, VSPI, VCP4/iVDP1C, CSI2/VIN, FDP</td>
</tr>
</tbody>
</table>

This document is attached with the video and display bandwidth calculation sheet, in which bandwidths are calculated based on the descriptions in this application note. The target IP modules in the calculation sheet are also the video and display IP modules covered in this application note.

Each of third-generation R-Car series products has a theoretical upper limit on the DDR bandwidth and this limit should be considered when examining the flow of video data. For example, if all video and display IP modules operate at the maximum performance, the total bus bandwidth used will exceed the upper limit and the flow of video data will not work in this case.

First, this document describes the upper limit on the bus bandwidth related to the video and display IP modules.

This document then gives IP performance guidelines A) to C) shown below for each of the video and display IP modules. When examining the flow of video data, calculate the bandwidth used by the video and display IP modules according to the guidelines A) to C) and check that the calculated value does not exceed the upper limit of the bus bandwidth.

- A) Maximum performance
- B) Concepts of deriving performance
- C) Concepts of deriving bandwidth

Section 3.1 gives an overview of guidelines A) to C).
3.1 Overview of Guidelines for Each IP Module

A) Maximum Performance

The specifications related to the maximum performance of each IP module are represented in the units shown in Table 3-2.

<table>
<thead>
<tr>
<th>IP</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>VSPD and DU</td>
<td>• Dot clock frequency: MHz</td>
</tr>
<tr>
<td></td>
<td>• Number of input planes</td>
</tr>
<tr>
<td>VSPB and VSPBS, VSPI, FDP</td>
<td>• Pixel rate: Mpixel/s</td>
</tr>
<tr>
<td></td>
<td>• Frame rate: fps</td>
</tr>
<tr>
<td>VCP4 and iVDP1C</td>
<td>• Pixel rate: Mpixel/s</td>
</tr>
<tr>
<td></td>
<td>• Frame rate: fps</td>
</tr>
<tr>
<td>CSI2</td>
<td>• Data transfer rate: Gbit/s</td>
</tr>
<tr>
<td>VIN</td>
<td>• Video clock frequency: MHz</td>
</tr>
</tbody>
</table>

B) Concepts of Deriving Performance

When multiple sequences operate, calculate the required performance for operation from the image size, frame rate, etc. for each sequence. The total of performance values for all IP modules should not exceed the maximum performance shown in A).

C) Concepts of Deriving Bandwidth

For comparison with the upper limit on the bus bandwidth for the video and display IP modules, calculate the required bandwidth for each IP module. In third-generation R-Car series products, the bandwidth can be independently specified for each IP module, and bandwidth arbitration is controlled by the QoS controller. To generate parameters for QoS control, use the calculated bandwidth for each IP module. Note that the time of processing in the video and display IP modules can become longer depending on the settings of the parameters (bandwidths) used for QoS control. For details, see section 3.2.
3.2 QoS Settings and IP Processing Time

In third-generation R-Car series products, the bandwidth can be independently specified for each IP module, and bandwidth arbitration is controlled by the QoS controller. The user needs to determine the required bandwidth for each IP module when specifying parameters for QoS control.

The processing time in a video and display IP module can become longer depending on the QoS parameter setting (bandwidth). Figure 3-1 shows three cases (1) to (3) in which the same processing is executed with different QoS settings.

In the bar graph for each of the cases, the vertical axis indicates the performance of each IP module and the horizontal axis indicates the processing time in each IP module. As the same processing is executed in all three cases, the amount of processed data (the area of each bar) is the same for all cases.

In case (3) in Figure 3-1, the QoS parameters are specified so that the performance of the IP module becomes 1/2 of the maximum performance. The processing time in the IP module becomes twice as large as that in case (2), which is the standard case.

In case (1) in Figure 3-1, the QoS parameters are specified so that the performance of the IP module becomes 1.5 times as large as the maximum performance. In this case, however, the IP module works at the maximum performance, and the processing time in the IP module is the same as in case (2).

When using video and display IP modules, the processing time in the IP modules depends on the QoS setting values. Calculate required bandwidths and modify QoS setting as necessary with reference to this application note.

![Figure 3-1 Relationship between QoS Settings and IP Processing Time](image)

**Figure 3-1 Relationship between QoS Settings and IP Processing Time**
3.3 Summary — Procedure for Calculating Performance and Bandwidth of Each Video and Display IP Module

Follow the procedure shown in Figure 3-2 to determine the operating conditions and calculate the bandwidth value for each IP module.

---

Notes:
1. VSPD/DU, VSPB/VSPBS, VSPI, VCP4/iVDP1C, CSI2/VIN, and FDP
2. The descriptions in the application note “Flow of Video Data” are represented in the form of the bandwidth calculation sheet.

---

Figure 3-2 Procedure for Calculating Performance and Bandwidth of Each Video and Display IP Module
4. **Upper Limits on Bus Bandwidths Related to Video and Display IP Modules**

4.1 **Third-generation R-Car Series Bus System and Upper Limits on Bandwidths**

In the third-generation R-Car series bus system, multiple domains are connected to the main memory domain AXI bus and have the following limits.

(i) Upper limit on the bandwidth for connection between domains
   The bandwidth for connection between each domain and the main memory domain AXI bus has an upper limit depending on the width of the connected bus.

(ii) Upper limit on the bandwidth for the main memory domain AXI
   The bandwidth for the main memory domain AXI has an upper limit depending on the bus width.

(iii) Theoretical upper limit on the DDR bandwidth for access from the video and display IP modules
   Each video and display IP module belongs to the VP, VC, or VIO domain. These domains have an upper limit on the total bandwidth for access to DDR depending on the theoretical DDR bandwidth.

(1) **Version 1.1 of the R-Car M3-W**

The relationship among the IP modules, the main memory domain AXI, and the domains are shown below.

![Schematic Diagram of Third-generation R-Car Series Bus System](image-url)
Table 4-1  Relationship among Main Memory Domain AXI, Domains, and Instances of IP Modules

<table>
<thead>
<tr>
<th>Main Memory Domain AXI/Connected Bus</th>
<th>Domain/Connected Bus</th>
<th>Instance of IP Module</th>
</tr>
</thead>
<tbody>
<tr>
<td>Main memory domain AXI/1</td>
<td>VC/0</td>
<td>VSPi0, VDPB, VCPLF, iVDP1C, FDP0, IMR0, IMR1</td>
</tr>
<tr>
<td></td>
<td>VIO/0</td>
<td>VSPD0 to VSPD3, VIN0 to VIN7, VSPB</td>
</tr>
</tbody>
</table>

The bandwidth for read access through the bus connected with the following domain must not exceed the upper limit on the bandwidth for connection between domains.

Table 4-2  Condition for Checking the Upper Limit on the Bandwidth for Connection between Domains

<table>
<thead>
<tr>
<th>Limit No.</th>
<th>Item</th>
<th>Domain/Connected Bus</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>(i)</td>
<td>Checking the upper limit on the bandwidth for connection between domains</td>
<td>VIO/0</td>
<td>The total bandwidth for read access from the instance of the IP module in the domain shown to the left should be no more than 10 Gbytes/s.</td>
</tr>
</tbody>
</table>

The total bandwidth of the video and display IP modules must not exceed the theoretical upper limit on the DDR bandwidth.

Table 4-3  Condition for Checking the Theoretical Upper Limit on the DDR Bandwidth for Access from the Video and Display IP Modules

<table>
<thead>
<tr>
<th>Limit No.</th>
<th>Item</th>
<th>Video and Display IP Module</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>(iii)</td>
<td>Checking the theoretical upper limit on the DDR bandwidth for access from the video and display IP modules</td>
<td>VSPD/DU, VSPB, VSPi, VCP4/iVDP1C, CSI2/VIN, FDP, IMR, HDMI</td>
<td>The total bandwidth for the IP modules shown to the left should be 55% or less of the theoretical DDR bandwidth. Example of theoretical DDR bandwidth in third-generation R-Car series products: Version 1.1 of the R-Car M3-W (LPDDR4 3200 Mbps × 2 channels): 25.6 Gbytes/s</td>
</tr>
</tbody>
</table>

Note: * Based on evaluation in 2-ch. split mode.
(2) Version 2.0 and 3.0 of the R-Car H3

The relationship among the IP modules, the main memory domain AXI, and the domains are shown below.

![Diagram of R-Car Series, 3rd Generation Bus System](image)

**Figure 4-2 Schematic Diagram of Third-generation R-Car Series Bus System**

**Table 4-4 Relationship among Main Memory Domain AXI, Domains, and Instances of IP Modules**

<table>
<thead>
<tr>
<th>Main Memory Domain AXI/Connected Bus</th>
<th>Domain/Connected Bus</th>
<th>Instance of IP Module</th>
</tr>
</thead>
<tbody>
<tr>
<td>Main memory domain AXI/2</td>
<td>VP/0</td>
<td>VSPBC, VSPi0, FDP0</td>
</tr>
<tr>
<td></td>
<td>VP/1</td>
<td>VSPBD, VSPi1, FDP1</td>
</tr>
<tr>
<td></td>
<td>VC/0</td>
<td>VDBP, VCPLF, IMR0, IMR1</td>
</tr>
<tr>
<td></td>
<td>VC/1</td>
<td>VCPLF, VDPi1C, IMR2, IMR3</td>
</tr>
<tr>
<td>Main memory domain AXI/3</td>
<td>VIO/0</td>
<td>VSPDL, VSPD1, VIN0 to VIN3</td>
</tr>
<tr>
<td></td>
<td>VIO/1</td>
<td>VSPD2, VIN4 to VIN7</td>
</tr>
</tbody>
</table>
The bandwidth for read access through the buses connected with the following domain must not exceed the upper limit on the bandwidth for connection between domains.

### Table 4-5 Conditions for Checking the Upper Limit on the Bandwidth for Connection between Domains

<table>
<thead>
<tr>
<th>Limit No.</th>
<th>Item</th>
<th>Domain/Connected Bus</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>(i)</td>
<td>Checking the upper limit on the bandwidth between the</td>
<td>VP/0</td>
<td>The total bandwidth for read access from the instance of the IP module in the domain shown to the left should be no more than 10 Gbytes/s.</td>
</tr>
<tr>
<td></td>
<td>bandwidth on the buses connected with the main</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>memory domain AXI</td>
<td>VP/1</td>
<td>The total bandwidth for read access from the instance of the IP module in the domain shown to the left should be no more than 10 Gbytes/s.</td>
</tr>
<tr>
<td></td>
<td>must not exceed the upper limit on the bandwidth</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>for connection between domains.</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

The bandwidth for read access through the buses connected with the main memory domain AXI must not exceed the upper limit on the bandwidth for the main memory domain AXI.

### Table 4-6 Conditions for Checking the Upper Limit on the Bandwidth for Main Bus

<table>
<thead>
<tr>
<th>Limit No.</th>
<th>Item</th>
<th>Main Memory Domain AXI/Connected Bus</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>(ii)</td>
<td>Checking the upper limit on the bandwidth for the</td>
<td>AXI/2</td>
<td>The total bandwidth for read access from the instance of the IP module in the main memory domain AXI shown to the left should be no more than 18 Gbytes/s.</td>
</tr>
<tr>
<td></td>
<td>main memory domain AXI</td>
<td>AXI/3</td>
<td>The total bandwidth for read access from the instance of the IP module in the main memory domain AXI shown to the left should be no more than 18 Gbytes/s.</td>
</tr>
<tr>
<td></td>
<td>must not exceed the upper limit on the bandwidth</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>for access from the main memory domain AXI</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

The total bandwidth of the video and display IP modules must not exceed the theoretical upper limit on the DDR bandwidth.

### Table 4-7 Condition for Checking the Theoretical Upper Limit on the DDR Bandwidth for Access from the Video and Display IP Modules

<table>
<thead>
<tr>
<th>Limit No.</th>
<th>Item</th>
<th>Video and Display IP Module</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>(iii)</td>
<td>Checking the theoretical upper limit on the DDR</td>
<td>VSPD/DU, VSPB, VSP1, VCP4/iVDP1C,</td>
<td>The total bandwidth for the IP modules shown to the left should be 55% or less of the theoretical DDR bandwidth.*</td>
</tr>
<tr>
<td></td>
<td>bandwidth for access from the video and display IP</td>
<td>CSI2/VIN, FDP, IMR, HDMI</td>
<td>Example of theoretical DDR bandwidth in third-generation R-Car series products: Version 2.0 and 3.0 of the R-Car H3 (LPDDR4 3200 Mbps × 4 channels): 51.2 Gbytes/s</td>
</tr>
<tr>
<td></td>
<td>modules</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Note: * Based on evaluation in 4-ch. split mode.
(3) **Version 1.x of the R-Car M3-N**

The relationship among the IP modules, the main memory domain AXI, and the domains are shown below.

![Figure 4-3 Schematic Diagram of Third-generation R-Car Series Bus System](image-url)

**Figure 4-3** Schematic Diagram of Third-generation R-Car Series Bus System
The total bandwidth of the video and display IP modules must not exceed the theoretical upper limit on the DDR bandwidth.

Table 4-9  Condition for Checking the Theoretical Upper Limit on the DDR Bandwidth for Access from the Video and Display IP Modules

<table>
<thead>
<tr>
<th>Limit No.</th>
<th>Item</th>
<th>Video and Display IP Module</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>(iii)</td>
<td>Checking the theoretical upper limit on the DDR bandwidth for access from the video and display IP modules</td>
<td>VSPD/DU, VSPB, VSPI, VCP4/iVDP1C, CSI2/VIN, FDP, IMR, HDMI</td>
<td>The total bandwidth for the IP modules shown to the left should be 55% or less of the theoretical DDR bandwidth.* Example of theoretical DDR bandwidth in third-generation R-Car series products: Version 1.x of the R-Car M3-N (LPDDR4 3200 Mbps × 1 channel): 12.8 Gbytes/s</td>
</tr>
</tbody>
</table>

Note: * Based on evaluation for the case of linear mapping.
(4) **Version 1.x of the R-Car E3**

The relationship among the IP modules, the main memory domain AXI, and the domains are shown below.

**Figure 4-4  Schematic Diagram of Third-generation R-Car Series Bus System**
The total bandwidth of the video and display IP modules must not exceed the theoretical upper limit on the DDR bandwidth.

### Table 4-10 Relationship among Main Memory Domain AXI, Domains, and Instances of IP Modules

<table>
<thead>
<tr>
<th>Main Memory Domain AXI/Connected Bus</th>
<th>Domain/Connected Bus</th>
<th>Instance of IP Module</th>
</tr>
</thead>
<tbody>
<tr>
<td>Main memory domain AXI/1</td>
<td>VP/0</td>
<td>VSPB, VSPI, FDP</td>
</tr>
<tr>
<td></td>
<td>VC/0</td>
<td>VDPB, VCPLF, iVDP1C, IMR0</td>
</tr>
<tr>
<td></td>
<td>VIO/0</td>
<td>VSPD0, VSPD1, VIN4, VIN5</td>
</tr>
</tbody>
</table>

### Table 4-11 Condition for Checking the Theoretical Upper Limit on the DDR Bandwidth for Access from the Video and Display IP Modules

<table>
<thead>
<tr>
<th>Limit No.</th>
<th>Item</th>
<th>Video and Display IP Module</th>
<th>Description</th>
</tr>
</thead>
</table>
| (iii)     | Checking the theoretical upper limit on the DDR bandwidth for access from the video and display IP modules | VSPD/DU, VSPB, VSPI, VCP4/VDP1C, CSI2/VIN, FDP, IMR, HDMI | The total bandwidth for the IP modules shown to the left should be 55% or less of the theoretical DDR bandwidth.*  
Example of theoretical DDR bandwidth in third-generation R-Car series products: Version 1.x of the R-Car E3 (DDR3L 1866 Mbps x 1 channel): 7.4 Gbytes/s |

Note: * Based on evaluation for the case of linear mapping.
(5) Version 1.x of the R-Car D3

The relationship among the IP modules, the main memory domain AXI, and the domains are shown below.

---

**Figure 4-5  Schematic Diagram of Third-generation R-Car Series Bus System**
The total bandwidth of the video and display IP modules must not exceed the theoretical upper limit on the DDR bandwidth.

Table 4-12  Relationship among Main Memory Domain AXI, Domains, and Instances of IP Modules

<table>
<thead>
<tr>
<th>Main Memory Domain AXI/Connected Bus</th>
<th>Domain/Connected Bus</th>
<th>Instance of IP Module</th>
</tr>
</thead>
<tbody>
<tr>
<td>Main memory domain AXI/1</td>
<td>VP/0</td>
<td>VSPBS</td>
</tr>
<tr>
<td></td>
<td>VC/0</td>
<td>IMR0</td>
</tr>
<tr>
<td></td>
<td>VIO/0</td>
<td>VSPD0, VSPD1, VIN4</td>
</tr>
</tbody>
</table>

Table 4-13  Condition for Checking the Theoretical Upper Limit on the DDR Bandwidth for Access from the Video and Display IP Modules

<table>
<thead>
<tr>
<th>Limit No.</th>
<th>Item</th>
<th>Video and Display IP Module</th>
<th>Description</th>
</tr>
</thead>
</table>
| (iii)     | Checking the theoretical upper limit on the DDR bandwidth for access from the video and display IP modules | VSPD/DU, VSPBS, VIN, IMR    | The total bandwidth for the IP modules shown to the left should be 55% or less of the theoretical DDR bandwidth.*  
Example of theoretical DDR bandwidth in third-generation R-Car series products: Version 1.x of the R-Car D3 (DDR3L 1866 Mbps × 1 channel): 3.7 Gbytes/s |

Note:  * Based on evaluation for the case of linear mapping.
5. Guidelines for Performance of the Video and Display IP Modules

5.1 Terms Used in Guidelines

Table 5-1 Terms Used in Guidelines

<table>
<thead>
<tr>
<th>Term</th>
<th>Description</th>
<th>Remarks</th>
</tr>
</thead>
<tbody>
<tr>
<td>Performance</td>
<td>Number of pixels processed per second. Unit: Mpixel/s.</td>
<td>In some image formats handled in the video and display IP modules, the number of bytes per pixel does not match the total number of bits for the colors (RGB or YCbCr) composing a pixel. For details, refer to the table &quot;Packed Formats for RPF Input&quot; in the description of the RPFn input format registers (VI6_RPFn_INFMT) in section 32, Video Signal Processor (VSP2), in the hardware manual.</td>
</tr>
<tr>
<td>Bandwidth</td>
<td>Amount of data transferred per second. Unit: Mbyte/s.</td>
<td></td>
</tr>
<tr>
<td>Color depth, bpp</td>
<td>Number of bytes per pixel that depends on the image format handled in the video and display IP modules. Unit: Byte/pixel.</td>
<td></td>
</tr>
<tr>
<td>Dot clock frequency</td>
<td>Pixel transfer rate in the DU represented in frequencies. Unit: MHz.</td>
<td></td>
</tr>
<tr>
<td>Video clock frequency</td>
<td>Pixel transfer rate in the VIN represented in frequencies. Unit: MHz.</td>
<td></td>
</tr>
<tr>
<td>Full HD</td>
<td>Images having a resolution of 1920 pixels × 1080 pixels.</td>
<td></td>
</tr>
</tbody>
</table>
### Table 5-2 Terms Used in Guidelines

<table>
<thead>
<tr>
<th>Term</th>
<th>Description</th>
<th>Remarks</th>
</tr>
</thead>
<tbody>
<tr>
<td>RPF</td>
<td>Abbreviation for the read pixel formatter, which is a functional block that can be used in the VSPI, VSPB, VSPD, and FDP. This block captures images into the IP modules.</td>
<td>For details, refer to section 32, Video Signal Processor (VSP2), and section 33, Fine Display Processor (FDP1), in the hardware manual.</td>
</tr>
<tr>
<td>Virtual RPF</td>
<td>A type of input image handled in the IP modules. No bus bandwidth is used for the processing to input this image.</td>
<td>For details, refer to section 32, Video Signal Processor (VSP2), in the hardware manual.</td>
</tr>
<tr>
<td>CLU, LUT, and OSD-CLUT</td>
<td>Abbreviations for the cubic lookup table, lookup table, and on-screen display color lookup table, respectively, which are functional blocks or functions that can be used in any of the VSPI, VSPB, and VSPD. These are used to handle index images or the color adjustment function.</td>
<td>For details, refer to the block diagrams in section 32, Video Signal Processor (VSP2), in the hardware manual.</td>
</tr>
<tr>
<td>UDS and SRU</td>
<td>Abbreviations for the up/down-scaler and super resolution unit, respectively, which are functional blocks or functions that can be used in the VSPI. These are used to upscale or downscale images or execute the super resolution processing.</td>
<td>For details, refer to the block diagrams in section 32, Video Signal Processor (VSP2), in the hardware manual.</td>
</tr>
<tr>
<td>Display list</td>
<td>Collective name for the functions that control the VSPI, VSPB, and VSPD through a list.</td>
<td>For details, refer to section 32.3.3, Display List, under the section on Video Signal Processor (VSP2) in the hardware manual.</td>
</tr>
<tr>
<td>YCbCr planar</td>
<td>This refers to the following among the image formats handled in the VSPB. YCbCr4:4:4 planar YCbCr4:2:2 planar (YV16) YCbCr4:2:0 planar (YV12, YU12)</td>
<td>For details, refer to the table &quot;Packed YCbCr Formats for RPF Input&quot; in the description of the RPFn input format registers (VI6_RPFn_INFMT) in section 32, Video Signal Processor (VSP2), in the hardware manual.</td>
</tr>
<tr>
<td>32-bpp ARGB</td>
<td>An image format handled in the VSP. This is an RGB format having 32-bit data per pixel. Specifically, this refers to the cases where the RPF input image format setting value (RDFMT) described in chapter 32, Video Signal Processor (VSP2), in the hardware manual is any of the following. 0x07 to 0x0E, 0x13, 0x14, 0x16, 0x17, 0x22, and 0x23</td>
<td>For details, refer to the table &quot;Packed Formats for RPF Input&quot; in the description of the RPFn input format registers (VI6_RPFn_INFMT) in section 32, Video Signal Processor (VSP2), in the hardware manual.</td>
</tr>
<tr>
<td>Alpha plane</td>
<td>This refers to the following among the alpha formats available in the VSP. 1-bit plane α 8-bit plane α</td>
<td>For details, refer to the description of the RPFn α plane selection control registers (VI6_RPFn_ALPH_SEL) in section 32, Video Signal Processor (VSP2), in the hardware manual.</td>
</tr>
<tr>
<td>Term</td>
<td>Description</td>
<td>Remarks</td>
</tr>
<tr>
<td>------</td>
<td>-------------</td>
<td>---------</td>
</tr>
<tr>
<td>Data types</td>
<td>Color formats for images handled in the VSPI, VSPB, VSPBS, VSPD, and FDP. When calculating the performance and bandwidth values, note that the color depth expected from the color format does not match the actual input/output color depth in some cases for these data types. For the relationships between the color formats and input/output color depths, refer to section 5.2, Relationships between Data Types and Color Depths, in this application note.</td>
<td>For details, refer to the table &quot;Video Channels and Supported Interfaces&quot; in section 26.3.1, Input Interface, under the section on Video Input Module (VIN) in the hardware manual.</td>
</tr>
<tr>
<td>Data types</td>
<td>Color formats for images handled in the interface between the CSI2 and VIN. When calculating the bandwidth values, note that the number of bits per pixel does not match the total number of bits for the colors (RGB or YCbCr) composing a pixel in some cases for these data types. The number of bits per pixel depends on the data type as follows. RGB-888: 24 bits 10-bit YCbCr-422: 20 bits 8-bit YCbCr-422: 16 bits RAW8: 8 bits</td>
<td></td>
</tr>
<tr>
<td>Video formats</td>
<td>Formats used in the external devices, which are input to the CSI2 and VIN and output from the VSPD and DU. The numbers of valid pixels per frame, scanning mode, and frame rate are shown in each format name. In the interlaced format, one frame is divided into two fields for even-numbered and odd-numbered lines in the vertical direction. For example, in the 1920 × 1080p60 format, 60 fields of 1920 × 540 valid pixels are transferred per second between each IP module and an external device.</td>
<td></td>
</tr>
<tr>
<td>IP converter</td>
<td>Abbreviation for the interlaced-to-progressive converter. For details, refer to section 33.1.1, Features, under the section on Fine Display Processor (FDP1) in the hardware manual.</td>
<td></td>
</tr>
</tbody>
</table>
5.2 Relationships between Data Types and Color Depths

Table 5-4 to Table 5-6 show the relationships between the major data types handled in the video and display IP modules and the input/output color depths. When the alpha plane is included in the input to or output from an IP module, add one byte/pixel to the input and output color depths as shown in Table 5-5.

Table 5-4 Relationships between Data Types and Color Depths

<table>
<thead>
<tr>
<th>IP Module</th>
<th>Data Type</th>
<th>Input Color Depth (byte/pixel)</th>
<th>Output Color Depth (byte/pixel)</th>
<th>Remarks</th>
</tr>
</thead>
<tbody>
<tr>
<td>VSPD</td>
<td>YUV420 semi-planar</td>
<td>2</td>
<td>1.5</td>
<td>Equivalent to YCbCr4:2:0 in the hardware manual.</td>
</tr>
<tr>
<td>VSPB</td>
<td>YUV422 semi-planar</td>
<td>2</td>
<td>2</td>
<td></td>
</tr>
<tr>
<td>VSPBS</td>
<td>YUV444 semi-planar</td>
<td>3</td>
<td>3</td>
<td></td>
</tr>
<tr>
<td>VSP</td>
<td>YUV420 interleaved</td>
<td>3</td>
<td>3</td>
<td></td>
</tr>
<tr>
<td>FDP</td>
<td>YUV422 interleaved</td>
<td>2</td>
<td>2</td>
<td></td>
</tr>
<tr>
<td></td>
<td>YUV444 interleaved</td>
<td>3</td>
<td>3</td>
<td></td>
</tr>
<tr>
<td></td>
<td>YUV420 planar</td>
<td>2</td>
<td>1.5</td>
<td></td>
</tr>
<tr>
<td></td>
<td>YUV422 planar</td>
<td>2</td>
<td>2</td>
<td></td>
</tr>
<tr>
<td></td>
<td>YUV444 planar</td>
<td>3</td>
<td>3</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Packed RGB 32 bits/pel</td>
<td>4</td>
<td>4</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Packed RGB 24 bits/pel</td>
<td>3</td>
<td>3</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Packed RGB 16 bits/pel</td>
<td>2</td>
<td>2</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Packed RGB 8 bits/pel</td>
<td>1</td>
<td>1</td>
<td></td>
</tr>
<tr>
<td>CLUT</td>
<td></td>
<td>1</td>
<td>1</td>
<td>Equivalent to CLUT_DATA in the hardware manual.</td>
</tr>
</tbody>
</table>
### Table 5-5  Relationships between Data Types and Color Depths

<table>
<thead>
<tr>
<th>IP Module</th>
<th>Data Type</th>
<th>Input Color Depth (byte/pixel)</th>
<th>Remarks</th>
</tr>
</thead>
<tbody>
<tr>
<td>VSPD</td>
<td>YUV420 semi-planar + alpha plane</td>
<td>2 + 1</td>
<td>Equivalent to YCbCr4:2:0 in the hardware manual.</td>
</tr>
<tr>
<td>VSPB</td>
<td>YUV422 semi-planar + alpha plane</td>
<td>2 + 1</td>
<td></td>
</tr>
<tr>
<td>VSPBS</td>
<td>YUV444 semi-planar + alpha plane</td>
<td>3 + 1</td>
<td></td>
</tr>
<tr>
<td>VSPI</td>
<td>YUV422 interleaved + alpha plane</td>
<td>2 + 1</td>
<td></td>
</tr>
<tr>
<td>FDP</td>
<td>YUV420 interleaved + alpha plane</td>
<td>3 + 1</td>
<td></td>
</tr>
<tr>
<td></td>
<td>YUV444 interleaved + alpha plane</td>
<td>3 + 1</td>
<td></td>
</tr>
<tr>
<td></td>
<td>YUV420 planar + alpha plane</td>
<td>2 + 1</td>
<td></td>
</tr>
<tr>
<td></td>
<td>YUV422 planar + alpha plane</td>
<td>2 + 1</td>
<td></td>
</tr>
<tr>
<td></td>
<td>YUV444 planar + alpha plane</td>
<td>3 + 1</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Packed RGB 32 bits/pel + alpha plane</td>
<td>4 + 1</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Packed RGB 24 bits/pel + alpha plane</td>
<td>3 + 1</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Packed RGB 16 bits/pel + alpha plane</td>
<td>2 + 1</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Packed RGB 8 bits/pel + alpha plane</td>
<td>1 + 1</td>
<td></td>
</tr>
<tr>
<td></td>
<td>CLUT + alpha plane</td>
<td>1 + 1</td>
<td>Equivalent to CLUT_DATA in the hardware manual.</td>
</tr>
</tbody>
</table>

### Table 5-6  Relationships between Data Types and Color Depths

<table>
<thead>
<tr>
<th>IP Module</th>
<th>Data Type</th>
<th>Output Color Depth (byte/pixel)</th>
</tr>
</thead>
<tbody>
<tr>
<td>VIN</td>
<td>YC: YCbCr-422, Y(8)/C(8)</td>
<td>2</td>
</tr>
<tr>
<td></td>
<td>YC: YCbCr-422, Y(10)/C(10)</td>
<td>4</td>
</tr>
<tr>
<td></td>
<td>YC: YCbCr-422, Y(12)/C(12)</td>
<td>4</td>
</tr>
<tr>
<td></td>
<td>YC separation: YCbCr-422, Y(8)/C(8)</td>
<td>2</td>
</tr>
<tr>
<td></td>
<td>YC separation: YCbCr-420, Y(8)/C(8)</td>
<td>1.5</td>
</tr>
<tr>
<td></td>
<td>YC separation: YCbCr-422, Y(10)/C(10)</td>
<td>4</td>
</tr>
<tr>
<td></td>
<td>YC separation: YCbCr-422, Y(12)/C(12)</td>
<td>4</td>
</tr>
<tr>
<td></td>
<td>YC separation: YCbCr-422, Y(10)/C(8)</td>
<td>3</td>
</tr>
<tr>
<td></td>
<td>YC separation: YCbCr-422, Y(12)/C(8)</td>
<td>3</td>
</tr>
<tr>
<td></td>
<td>RGB-565</td>
<td>2</td>
</tr>
<tr>
<td></td>
<td>ARGB-1555</td>
<td>2</td>
</tr>
<tr>
<td></td>
<td>RGB-888</td>
<td>4</td>
</tr>
<tr>
<td></td>
<td>ARGB-8888</td>
<td>4</td>
</tr>
</tbody>
</table>
5.3 VSPD and DU

5.3.1 A) Maximum Performance

(1) Version 1.1 of the R-Car M3-W

The maximum dot clock frequency and the maximum input and data rate of VSPD through each channel are given in Table 5-7. The maximum input and data rate depends on each channel (DU0 to DU2).

The input and data rate of VSPD is as follows. For each channel, the input and data rate should not exceed the maximum input data rate.

Input and data rate (Mbyte/s) = Dot clock [MHz] \times \text{The sum of bpp values of planes for blending (*) [byte/pixel]}

Note: * The plane where virtual RPF is used is excluded.

![Block Diagram of VSPD and DU (Version 1.1 of the R-Car M3-W)](image)

<table>
<thead>
<tr>
<th>Display Channel</th>
<th>Maximum Dot Clock Frequency (MHz)</th>
<th>Maximum Input and Data Rate ( (\text{Mbyte/s}) ) (Dot clock frequency condition is shown in parentheses.)</th>
<th>Examples of Video Formats for Dot Clock Frequency Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>DU0 (LVDS)</td>
<td>148.5</td>
<td>(148.5 \times 12 ) (at up to 148.5 MHz)</td>
<td>(1920 \times 1080p60)</td>
</tr>
<tr>
<td>DU1 (HDMI)</td>
<td>297</td>
<td>(148.5 \times 12 ) (at up to 148.5 MHz) (97 \times 4 ) (at 148.6 MHz to 297 MHz)</td>
<td>(1920 \times 1080p60)</td>
</tr>
<tr>
<td>DU2 (DRGB)</td>
<td>100</td>
<td>(100 \times 12 ) (at up to 100 MHz)</td>
<td>(1280 \times 800p60)</td>
</tr>
</tbody>
</table>
(2) Version 2.0 and 3.0 of the R-Car H3

The maximum dot clock frequency and the maximum input and data rate of VSPD through each channel are given in Table 5-8. The maximum input and data rate depends on each channel (DU0 to DU3).

The input and data rate of VSPD is as follows. For each channel, the input and data rate should not exceed the maximum input data rate.

Input and data rate (Mbyte/s) = Dot clock [MHz] × The sum of bpp values of planes for blending (*) [byte/pixel]

Note: * The plane where virtual RPF is used is excluded.

![Block Diagram of VSPD and DU](image)

**Figure 5-2 Block Diagram of VSPD and DU (Version 2.0 and 3.0 of the R-Car H3)**

<table>
<thead>
<tr>
<th>Display Channel</th>
<th>Maximum Dot Clock Frequency (MHz)</th>
<th>Maximum Input and Data Rate (Mbyte/s) (Dot clock frequency condition is shown in parentheses.)</th>
<th>Examples of Video Formats for Dot Clock Frequency Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>DU0 (LVDS)</td>
<td>148.5</td>
<td>148.5 × 16* (at up to 148.5 MHz)</td>
<td>1920 × 1080p60</td>
</tr>
<tr>
<td>DU3 (DRGB)</td>
<td>100</td>
<td>100 × 16* (at up to 100 MHz)</td>
<td>1280 × 800p60</td>
</tr>
<tr>
<td>DU1 (HDMI0)</td>
<td>297</td>
<td>148.5 × 16 (at up to 148.5 MHz) 148.5 × 16 (at 148.6 MHz to 297 MHz)</td>
<td>1920 × 1080p60 3840 × 2160p30</td>
</tr>
<tr>
<td>DU2 (HDMI1)</td>
<td>297</td>
<td>148.5 × 16 (at up to 148.5 MHz) 297 × 8 (at 148.6 MHz to 297 MHz)</td>
<td>1920 × 1080p60 3840 × 2160p30</td>
</tr>
</tbody>
</table>

Note: * The total number of the planes for blending in DU0 and DU3 can never be greater than 5. The sum of input and data rate in DU0 and DU3 can never be greater than 148.5 × 16.
Version 1.x of the R-Car M3-N

The maximum dot clock frequency and the maximum input and data rate of VSPD through each channel are given in Table 5-9. The maximum input and data rate depends on each channel (DU0, DU1, DU3).

The input and data rate of VSPD is as follows. For each channel, the input and data rate should not exceed the maximum input data rate.

Input and data rate (Mbyte/s) = Dot clock [MHz] × The sum of bpp values of planes for blending (*) [byte/pixel]

Note: * The plane where virtual RPF is used is excluded.

---

Table 5-9  Maximum Performance of VSPD and DU (Version 1.x of the R-Car M3-N)

<table>
<thead>
<tr>
<th>Display Channel</th>
<th>Maximum Dot Clock Frequency (MHz)</th>
<th>Maximum Input and Data Rate (Mbyte/s) (Dot clock frequency condition is shown in parentheses.)</th>
<th>Examples of Video Formats for Dot Clock Frequency Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>DU0 (LVDS)</td>
<td>148.5</td>
<td>148.5 × 12 (at up to 148.5 MHz)*</td>
<td>1920 × 1080p60</td>
</tr>
<tr>
<td>DU3 (DRGB)</td>
<td>100</td>
<td>100 × 12 (at up to 100 MHz)*</td>
<td>1280 × 800p60</td>
</tr>
<tr>
<td>DU1 (HDMI0)</td>
<td>297</td>
<td>148.5 × 12 (at up to 148.5 MHz)</td>
<td>1920 × 1080p60</td>
</tr>
<tr>
<td></td>
<td></td>
<td>297 × 4 (at 148.6 MHz to 297 MHz)</td>
<td>3840 × 2160p30</td>
</tr>
</tbody>
</table>

Note: * The total number of the planes for blending in DU0 and DU3 can never be greater than 5. The sum of input and data rate in DU0 and DU3 can never be greater than 148.5 × 12. The sum of input and data rate in all DUs can never be greater than 148.5 × 18.
The maximum dot clock frequency and the maximum input and data rate of VSPD through each channel are given in Table 5-10. The maximum input and data rate depends on each channel (DU0, DU1).

The input and data rate of VSPD is as follows. For each channel, the input and data rate should not exceed the maximum input data rate.

Input and data rate (Mbyte/s) = Dot clock [MHz] \times \text{The sum of bpp values of planes for blending (*) [byte/pixel]}

Note: * The plane where virtual RPF is used is excluded.

<table>
<thead>
<tr>
<th>Display Channel</th>
<th>Maximum Dot Clock Frequency (MHz)</th>
<th>Maximum Input and Data Rate (Mbyte/s) (Dot clock frequency condition is shown in parentheses.)</th>
<th>Examples of Video Formats for Dot Clock Frequency Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>DU0 (LVDS0)</td>
<td>111.75*</td>
<td>111.75 \times 8 (at up to 111.75 MHz)*</td>
<td>1920 \times 720p60</td>
</tr>
<tr>
<td>DU1 (LVDS1)</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>DU0 (DRGB)</td>
<td>74.25</td>
<td>74.25 \times 8 (at up to 74.25 MHz)</td>
<td>1280 \times 720p60</td>
</tr>
<tr>
<td>DU1 (DRGB)</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Note: * If either of the following conditions is satisfied, the maximum dot clock frequency is 100 MHz and the maximum input and data rates, which correspond to that frequency, are 100 \times 8 \text{ Mbyte/s.}

Condition 1: Data are input in the specified format with a separate alpha plane.

This is the case where at least one RPF in the VSPD is handling either of the following input formats.

- 32-bpp ARGB + alpha plane
- YCbCr planar + alpha plane

Condition 2: Data are input in the specified format with a separate alpha plane.

This is the case where at least one RPF in the VSPD is handling either of the following input formats.

- YCbCr4:4:4 semi-planar + alpha plane
- YCbCr4:2:2 semi-planar + alpha plane
(5) Version 1.x of the R-Car D3

The maximum dot clock frequency and the maximum input and data rate of VSPD through each channel are given in Table 5-11. The maximum input and data rate depends on each channel (DU0, DU1).

The input and data rate of VSPD is as follows. For each channel, the input and data rate should not exceed the maximum input data rate.

Input and data rate (Mbyte/s) = Dot clock [MHz] × The sum of bpp values of planes for blending (*) [byte/pixel]

Note: * The plane where virtual RPF is used is excluded.

![Block Diagram of VSPD and DU (Version 1.x of the R-Car D3)](image)

Note: * Data can neither be output through both LVDS0 and DRGB from DU0 nor through both LVDS1 and DRGB from DU1.

**Figure 5-5** Block Diagram of VSPD and DU (Version 1.x of the R-Car D3)
### Table 5-11 Maximum Performance of VSPD and DU (Version 1.x of the R-Car D3)

<table>
<thead>
<tr>
<th>Display Channel</th>
<th>Maximum Dot Clock Frequency (MHz)</th>
<th>Maximum Input and Data Rate (Mbyte/s)</th>
<th>Examples of Video Formats for Dot Clock Frequency Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>DU0 (LVDS0)</td>
<td>111.75<em>1</em>2</td>
<td>111.75 * 8 (at up to 111.75 MHz)<em>1</em>2</td>
<td>1920 × 720p60</td>
</tr>
<tr>
<td>DU1 (LVDS1)</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>DU0 (DRGB)</td>
<td>29.5</td>
<td>29.5 * 8 (at up to 29.5 MHz)</td>
<td>800 × 480p60</td>
</tr>
<tr>
<td>DU1 (DRGB)</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Notes:**
1. The maximum number of planes for blending in one DU is 2. The sum of input and data rate in all DUs can never be greater than 1130 (= 111.75 × 8 + 29.5 × 8).
2. If the following condition is satisfied, the maximum dot clock frequency is 100 MHz and the maximum input and data rates, which correspond to that frequency, are 100 × 8 Mbyte/s.
   - Condition: Data are input in the specified format with a separate alpha plane.
   - This is the case where at least one RPF in the VSPD is handling either of the following input formats.
     - 32-bpp ARGB + alpha plane
     - 24-bpp RGB + alpha plane
     - YCbCr 444 interleave + alpha plane
     - YCbCr planar + alpha plane
     - YCbCr semi-planar + alpha plane
5.3.2 B) Concepts of Deriving Performance

An approximate dot clock frequency can be obtained from the resolution and frame rate for each display channel. Examples in standard video formats, such as those promulgated by SMPTE or VESA, are shown in the table below. (Entries under "Total Number of Pixels Horizontally" and "Total Number of Lines" represent the sizes including the blanking periods.)

Table 5-12 Examples in Standard Video Formats

<table>
<thead>
<tr>
<th>Video Format</th>
<th>Number of Valid Pixels Horizontally</th>
<th>Number of Valid Lines</th>
<th>Total Number of Pixels Horizontally</th>
<th>Total Number of Lines</th>
<th>Frame Rate (Hz)</th>
<th>Dot Clock Frequency (MHz)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1280 × 720p60</td>
<td>1280</td>
<td>720</td>
<td>1650</td>
<td>750</td>
<td>60</td>
<td>74.25</td>
</tr>
<tr>
<td>1920 × 1080i60</td>
<td>1920</td>
<td>1080</td>
<td>2200</td>
<td>1125</td>
<td>30</td>
<td>74.25</td>
</tr>
<tr>
<td>1920 × 1080p60</td>
<td>1920</td>
<td>1080</td>
<td>2200</td>
<td>1125</td>
<td>60</td>
<td>148.5</td>
</tr>
</tbody>
</table>

In development of the target board, the actual dot clock frequency is determined by the specifications of the external device connected to each display channel and the DU register settings related to the dot clock frequency. Consult with those who manage the related requirements to determine the dot clock frequency for each display channel.
5.3.3 C) Concepts of Deriving Bandwidth

The VSPD reads display data from external memory. To prevent underflows of the display data, the maximum bandwidth (referred to as the peak bandwidth) instead of the average bandwidth during the display period of frames is required. The peak bandwidth per output channel is obtained as follows. As this expression shows, the peak bandwidth increases with the number of planes for blending being processed in the VSPD. The bandwidth for a VSPD that has two LIFs and outputs data to two DUs is the sum total of the bandwidth calculated based on the given dot clock frequency.

[When display data is output to one DU]

Peak bandwidth (Mbyte/s) = Dot clock frequency [MHz] × \( \sum BPPin[n] \)

\( BPPin[n] (n = 0, 1, ..., 4) \): Number of bytes per pixel in input plane n

[When display data is output to two DUs]

When the VSPD outputs data to the first DU via LIF0 and to the second DU via LIF1, the peak bandwidth is calculated as follows:

Peak bandwidth (Mbyte/s) = Dot clock frequency [MHz] of the first DU \( \times \sum BPPin[n] \) of LIF0 +

Dot clock frequency [MHz] of the second DU \( \times \sum BPPin[n] \) of LIF1

\( BPPin[n] (n = 0, 1, ..., 4) \): Number of bytes per pixel for plane n that is input to LIFm (m = 0, 1)
### 5.3.4 D) Example of Bandwidth Calculation

The bandwidth required for VSPD operation is the peak bandwidth per output channel. The following shows an example of calculation.

**Example: DU channel 1**

Calculation for dot clock frequency = 148.5 MHz, frame rate = 60 fps, input image size = Full HD, color depth = 4 bytes/pixel, and 2-plane blending

Peak bandwidth (byte/s) = dot clock frequency (MHz) × Σn BPPin[n] (byte/pixel)

= 148.5 × 8 = 1188 (Mbytes/s)

Dot clock frequency = 148.5 MHz

Σn BPPin[n] = BPPin[0] + BPPin[1] = 4 + 4 (bytes/pixel) = 8 (bytes/pixel)

When the required bandwidth calculated is specified for a QoS parameter, the IP module operates as shown in Figure 5-6.

![Figure 5-6 VSPD and DU Operation with Sample QoS Setting](image-url)
5.4 **VSPB and VSPBS**

The IP module that is mounted depends on the type of the LSI chip.


VSPBS: Version 1.x of the R-Car D3

5.4.1 **A) Maximum Performance**

(1) **Version 1.1 of the R-Car M3-W**

Performance of the VSPB required for a use case must satisfy both conditions (a) and (b) for the maximum performance of the VSPB described below.

(a) **Maximum performance of the VSPB for pixel rate**

The maximum performance per VSPB interface for pixel rate is given below.

- When none of conditions 1 to 4 shown in Figure 5-7 are met:
  - 500 Mpixel/s (equivalent to Full HD at 240 fps)
- When condition 1 shown in Figure 5-7 is met:
  - 250 Mpixel/s (equivalent to Full HD at 120 fps)
- When any of conditions 2 to 4 shown in Figure 5-7 is met:
  - 375 Mpixel/s (equivalent to Full HD at 180 fps)

If a display list is used for dynamically changing the CLU, LUT, or OSD-CLUT table, subtract the following value from the maximum performance for pixel rate.

- CLU: 170 (kpixels) \times \text{frame rate} (fps)
  
  (Example: For a frame rate of 60 fps, 10.2 Mpixel/s)

- LUT: 4.5 (kpixels) \times \text{frame rate} (fps)
  
  (Example: For a frame rate of 60 fps, 270 kpixels/s)

- OSD-CLUT (per RPF): 4.5 (kpixels) \times \text{frame rate} (fps)
  
  (Example: For a frame rate of 60 fps, 270 kpixels/s)

(b) **Maximum performance of the VSPB for frame rate**

- The maximum performance for frame rate per VSPB interface is 480 fps.
- The total frame rate for all sequences that a single VSPB interface processes through time division must be no greater than 480 fps.
Procedure for deriving the maximum performance for pixel rate

Figure 5-7 shows the procedure for deriving the maximum performance of the VSPB for pixel rate. For details of the conditions, refer to description in (d).

Figure 5-7  Procedure for Deriving Maximum Performance of VSPB for Pixel Rate
(d) Detailed conditions for determining the maximum performance for pixel rate

Details of conditions 1 to 4 described in Figure 5-7 are given below.

Condition 1: Data are input in the specified format (format 1) with a separate alpha plane.
This is the case where at least one RPF in the VSPB is handling any of the following input formats.
- 32-bpp ARGB + alpha plane
- YCbCr planar + alpha plane

Condition 2: Data are input in the specified format (format 2) with a separate alpha plane.
This is the case where at least one RPF in the VSPB is handling any of the following input formats.
- YCbCr4:4:4 semi-planar + alpha plane
- YCbCr4:2:2 semi-planar + alpha plane

Condition 3: The sum of BPP values of input formats handled by all RPFs in the VSPB is greater than 16.
The following shows a case of input formats for RPF0 to RPF4 where the sum of BPP values of all RPFs* is 17.
- RPF0 = YCbCr4:2:2 semi-planar (2 bytes/pixel)
- RPF1 = YCbCr4:2:2 semi-planar + alpha plane (3 bytes/pixel)
- RPF2 = 32-bpp ARGB (4 bytes/pixel)
- RPF3 = 32-bpp ARGB (4 bytes/pixel)
- RPF4 = 32-bpp ARGB (4 bytes/pixel)

Condition 4: A specified condition is satisfied for YCbCr planar input.
This is the case where the RPFs in the VSPB satisfy either of the following conditions.
- Two or more RPFs are in the YCbCr planar format.
- One RPF is in the YCbCr planar format and the total number of RPFs* is five planes.

Note: * The plane where virtual RPF is used is excluded.
(2) Version 2.0 and 3.0 of the R-Car H3

The maximum performance of the VSPB depends on the number of VSPBs that are simultaneously operating, i.e. on whether (i) one VSPB is operating or (ii) two VSPBs are simultaneously operating. The following describes the two cases separately.

The maximum performance of the VSPB should be switched simultaneously with switching of the QoS settings for the VSPB.

For example, in the case where two VSPBs are simultaneously operating but only one VSPB is actually operating locally, if the QoS settings for the VSPB have not been switched, assume that the maximum performance of the VSPB is not switched either and estimate the maximum performance for the case where two VSPBs are simultaneously operating.

Performance of the VSPB required for a use case must satisfy both conditions (a) and (b) for the maximum performance of the VSPB described below. Note that register setting is required as described in (e) to derive the maximum VSPB performance for pixel rate.

(a) Maximum performance of the VSPB for pixel rate

(i) When one VSPB is in use

The description on the maximum performance of the VSPB for pixel rate is the same as that for version 1.1 of the R-Car M3-W. Refer to (a) in (1) Version 1.1 of the R-Car M3-W in this section.

(ii) When two VSPBs are in use

• When none of conditions 1 to 3 shown in Figure 5-8 are met:
  — 500 Mpixs/s (equivalent to Full HD at 240 fps)
• When condition 1 shown in Figure 5-8 is met:
  — 250 Mpixs/s (equivalent to Full HD at 120 fps)
• When either condition 2 or condition 3 shown in Figure 5-8 is met:
  — 375 Mpixs/s (equivalent to Full HD at 180 fps)

When two VSPBs are in use, the maximum pixel rates per VSPB are as follows.

• When none of conditions 1 to 3 shown in Figure 5-8 are met:
  — 375 Mpixs/s (equivalent to Full HD at 180 fps)
• When any of conditions 1 to 3 shown in Figure 5-8 is met:
  — 250 Mpixs/s (equivalent to Full HD at 120 fps)

If a display table is used for dynamically changing the CLU, LUT, or OSD-CLUT table, subtract the following value from the maximum pixel rates.

— CLU: 170 (kpixels) × frame rate (fps)
  (Example: For a frame rate of 60 fps, 10.2 Mpixs/s)
— LUT: 4.5 (kpixels) × frame rate (fps)
  (Example: For a frame rate of 60 fps, 270 kpixels/s)
— OSD-CLUT (per RPF): 4.5 (kpixels) × frame rate (fps)
  (Example: For a frame rate of 60 fps, 270 kpixels/s)
(b) Maximum performance of the VSPB for frame rate

(i) When one VSPB is in use

The description on the maximum performance for frame rate is the same as that for version 1.1 of the R-Car M3-W. Refer to (b) in (1) Version 1.1 of the R-Car M3-W in this section.

(ii) When two VSPBs are in use

The maximum frame rates per VSPB interface is 180 fps.

The total frame rate for all sequences that a single VSPB interface processes through time division must be no greater than 180 fps.
(c) Procedure for deriving the maximum performance for pixel rate

(i) When one VSPB is in use

The procedure for deriving the maximum performance for pixel rate is the same as that for version 1.1 of the R-Car M3-W. Refer to (c) in (1) Version 1.1 of the R-Car M3-W in this section.

(ii) When two VSPBs are in use

Figure 5-8 shows the procedure for deriving the maximum performance of the VSPB for pixel rate. For details of the conditions, refer to description in (d).

![Procedure for Deriving Maximum Performance of VSPB for Pixel Rate](image-url)

**Figure 5-8  Procedure for Deriving Maximum Performance of VSPB for Pixel Rate**
(d) Detailed conditions for determining the maximum performance for pixel rate

(i) When one VSPB is in use

The detailed conditions for determining the maximum performance for pixel rate are the same as those for version 1.1 of the R-Car M3-W. Refer to (d) in (1) Version 1.1 of the R-Car M3-W in this section.

(ii) When two VSPBs are in use

Details of conditions 1 to 3 described in Figure 5-8 are given below.

Condition 1: A specified condition is satisfied in the use of at least one RPF. This is the case where data are input in a specified format with a separate alpha plane for at least one RPF in the VSPB.

- \( \text{YCbCr}:4:4 \) semi-planar + alpha plane
- \( \text{YCbCr}:2:2 \) semi-planar + alpha plane
- 32-bpp ARGB + alpha plane
- YCbCr planar + alpha plane

Condition 2: The sum of BPP values of input formats handled by all RPFs in the VSPB is greater than 16. The following shows a case of input formats for RPF0 to RPF4 where the sum of BPP values of all RPFs\(^a\) is 17.

- RPF0 = \( \text{YCbCr}:4:2:2 \) semi-planar (2 bytes/pixel)
- RPF1 = \( \text{YCbCr}:4:2:2 \) semi-planar + alpha plane (3 bytes/pixel)
- RPF2 = 32-bpp ARGB (4 bytes/pixel)
- RPF3 = 32-bpp ARGB (4 bytes/pixel)
- RPF4 = 32-bpp ARGB (4 bytes/pixel)

Condition 3: A specified condition is satisfied for a combination of RPFs. This is the case where a combination of the RPFs in the VSPB satisfies one of the following conditions.

- Input format for two or more RPFs is YCbCr planar\(^a\).
- Input format for one RPF is YCbCr planar\(^a\) and the total number of RPFs\(^a\) is five planes.
- Input format for four or more RPFs is any of the following:
  - 24-bpp RGB + alpha plane
  - YCbCr:4:4 interleaved + alpha plane
  - YCbCr:4:2:0 interleaved + alpha plane
  - Input format for five RPFs is any of the following:
    - 24-bpp RGB\(^a\)
    - YCbCr:4:4 interleaved\(^a\)
    - YCbCr:4:2:0 interleaved\(^a\)
    - Input format for five RPFs is any of the following:
      - 8-bpp RGB + alpha plane
      - CLUT + alpha plane
      - YCbCr:2:0 semi-planar + alpha plane
      - YCbCr:2:2 semi-planar

Notes: 1. The plane where virtual RPF is used is excluded.
2. Both cases with and without an alpha plane are included.

(e) Register setting required for the maximum performance for pixel rate

To achieve the maximum performance for pixel rate per VSPB interface, set 256-pixel transfer or 512 pixel-transfer with the VI6_RPFn_BAC register by following the guidelines in the hardware manual.
(3) **Version 1.x of the R-Car M3-N**

Performance of the VSPB required for a use case must satisfy both conditions (a) and (b) for the maximum performance of the VSPB described below.

(a) **Maximum performance of the VSPB for pixel rate**

The maximum performance per VSPB interface for pixel rate is given below.

- When none of conditions 1 to 4 shown in Figure 5-9 are met:
  - 500 Mpixels/s (equivalent to Full HD at 240 fps)
- When condition 1 shown in Figure 5-9 is met:
  - 125 Mpixels/s (less than or equal to the equivalent of Full HD at 90 fps)
- When either condition 2 or condition 3 shown in Figure 5-9 is met:
  - 250 Mpixels/s (equivalent to Full HD at 120 fps)
- When condition 4 shown in Figure 5-9 is met:
  - 375 Mpixels/s (equivalent to Full HD at 180 fps)

If a display table is used for dynamically changing the CLU, LUT, or OSD-CLUT table, subtract the following value from the maximum pixel rates.

- CLU: 170 kpixels × frame rate (fps)
  
  (Example: For a frame rate of 60 fps, 10.2 Mpixels/s)

- LUT: 4.5 kpixels × frame rate (fps)
  
  (Example: For a frame rate of 60 fps, 270 kpixels/s)

- OSD-CLUT (per RPF): 4.5 kpixels × frame rate (fps)
  
  (Example: For a frame rate of 60 fps, 270 kpixels/s)

(b) **Maximum performance of the VSPB for frame rate**

- The maximum performance for frame rate per VSPB interface is 480 fps.
- The total frame rate for all sequences that a single VSPB interface processes through time division must be no greater than 480 fps.
Procedure for deriving the maximum performance for pixel rate

Figure 5-9 shows the procedure for deriving the maximum performance of the VSPB for pixel rate. For details of the conditions, refer to description in (d).

![Diagram of procedure for deriving maximum performance for pixel rate]

- **Condition 1**: When 8 < the total number of addresses, less than 125 Mpxs/s (less than the equivalent of Full HD at 60 fps)
- **Condition 2**: When 6 < the total number of addresses ≤ 8, 125 Mpxs/s (equivalent to Full HD at 60 fps)
- **Condition 3**: When 4 < the total number of addresses ≤ 6, 187.5 Mpxs/s (equivalent to Full HD at 90 fps)
- **Condition 4**: 500 Mpxs/s (equivalent to Full HD at 240 fps)

**Figure 5-9  Procedure for Deriving Maximum Performance of VSPB for Pixel Rate**
(d) Detailed conditions for determining the maximum performance for pixel rate

Details of conditions 1 to 4 described in Figure 5-9 are given below.

Condition 1: The total number of addresses of the input formats handled by RPFs is greater than 4.
   The following shows a case of color formats for RPF0 to RPF4 where the total number of input addresses
   for all RPFs* is 4.
   — RPF0 = YCbCr4:2:2 semi-planar (2 inputs addresses)
   — RPF1 = YCbCr4:2:2 interleave (1 input address)
   — RPF2 = 32-bpp ARGB (1 input address)
   — RPF3 is not in use.
   — RPF4 is not in use.

Condition 2: Data are input in the specified format (format 1) with a separate alpha plane.
   This is the case where at least one RPF in the VSPB is handling either of the following input formats.
   — 32-bpp ARGB + alpha plane
   — YCbCr planar + alpha plane

Condition 3: The sum of BPP values of input and output formats handled by all RPFs and WPF in the VSPB is greater
   than 12 (the BPP values for the WPF must also be taken into consideration because of the narrow
   bandwidth of the R-Car M3-N).
   The following shows a case of input and output formats for RPF0 to RPF4 and WPF0 where the sum of
   BPP values for all RPFs* and WPF is 12.
   — RPF0 = YCbCr4:2:2 interleave (2 bytes/pixel)
   — RPF1 = YCbCr4:2:2 interleave (2 bytes/pixel)
   — RPF2 = YCbCr4:2:2 interleave (2 bytes/pixel)
   — RPF3 = YCbCr4:2:2 interleave (2 bytes/pixel)
   — RPF4 is not in use.
   — WPF0 = 32-bpp ARGB (4 bytes/pixel)

Condition 4: Data are input in the specified format (format 2) with a separate alpha plane.
   This is the case where at least one RPF in the VSPB is handling either of the following input formats.
   — YCbCr4:4:4 semi-planar + alpha plane
   — YCbCr4:2:2 semi-planar + alpha plane

Note: * The plane where virtual RPF is used is excluded.
(4) Version 1. X of the R-Car E3

Performance of the VSPB required for a use case must satisfy both conditions (a) and (b) for the maximum performance of the VSPB described below.

(a) Maximum performance of the VSPB for pixel rate

The maximum performance per VSPB interface for pixel rate is given below.

- When none of conditions 1 to 4 shown in Figure 5-10 are met:
  - 125 Mpixels/s (equivalent to Full HD at 60 fps)
- When condition 1 shown in Figure 5-10 is met:
  - 62.5 Mpixels/s (equivalent to Full HD at 30 fps)
- When any of conditions 2 to 4 shown in Figure 5-10 is met:
  - 93.75 Mpixels/s (equivalent to Full HD at 45 fps)

If a display list is used for dynamically changing the CLU, LUT, or OSD-CLUT table, subtract the following value from the maximum performance for pixel rate.

- CLU: 170 (kpixels) × frame rate (fps)
  (Example: For a frame rate of 60 fps, 10.2 Mpixels/s)
- LUT: 4.5 (kpixels) × frame rate (fps)
  (Example: For a frame rate of 60 fps, 270 kpixels/s)
- OSD-CLUT (per RPF): 4.5 (kpixels) × frame rate (fps)
  (Example: For a frame rate of 60 fps, 270 kpixels/s)

(b) Maximum performance of the VSPB for frame rate

- The maximum performance for frame rate per VSPB interface is 120 fps.
- The total frame rate for all sequences that a single VSPB interface processes through time division must be no greater than 120 fps.
(c) Procedure for deriving the maximum performance for pixel rate

Figure 5-10 shows the procedure for deriving the maximum performance of the VSPB for pixel rate. For details of the conditions, refer to description in (d).

![Flowchart](image-url)

**Figure 5-10  Procedure for Deriving Maximum Performance of VSPB for Pixel Rate**
(d) Detailed conditions for determining the maximum performance for pixel rate

Details of conditions 1 to 4 described in Figure 5-10 are given below.

- **Condition 1:** Data are input in the specified format (format 1) with a separate alpha plane. This is the case where at least one RPF in the VSPB is handling either of the following input formats.
  - 32-bpp ARGB + alpha plane
  - YCbCr planar + alpha plane

- **Condition 2:** Data are input in the specified format (format 2) with a separate alpha plane. This is the case where at least one RPF in the VSPB is handling either of the following input formats.
  - YCbCr4:4:4 semi-planar + alpha plane
  - YCbCr4:2:2 semi-planar + alpha plane

- **Condition 3:** The sum of BPP values of input formats handled by all RPFs in the VSPB is greater than 16. The following shows a case of input formats for RPF0 to RPF4 where the sum of BPP values of all RPFs* is 17.
  - RPF0 = YCbCr4:2:2 semi-planar (2 bytes/pixel)
  - RPF1 = YCbCr4:2:2 semi-planar + alpha plane (3 bytes/pixel)
  - RPF2 = 32-bpp ARGB (4 bytes/pixel)
  - RPF3 = 32-bpp ARGB (4 bytes/pixel)
  - RPF4 = 32-bpp ARGB (4 bytes/pixel)

- **Condition 4:** A specified condition is satisfied for YCbCr planar input. This is the case where the RPFs in the VSPB satisfy either of the following conditions.
  - Two or more RPFs are in the YCbCr planar format.
  - One RPF is in the YCbCr planar format and the total number of RPFs* is five planes.

Note: * The plane where virtual RPF is used is excluded.
(5) **Version 1. X of the R-Car D3**

Performance of the VSPBS required for a use case must satisfy both conditions (a) and (b) for the maximum performance of the VSPBS described below.

(a) **Maximum performance of the VSPBS for pixel rate**

The maximum performance per VSPBS interface for pixel rate is given below.

- When none of conditions 1 to 3 shown in Figure 5-11 are met:
  - 125 Mpixels/s (equivalent to Full HD at 60 fps)
- When condition 1 shown in Figure 5-11 is met:
  - 62.5 Mpixels/s (equivalent to Full HD at 30 fps)
- When either condition 2 or condition 3 shown in Figure 5-11 is met:
  - 93.75 Mpixels/s (equivalent to Full HD at 45 fps)

If a display table is used for dynamically changing the CLU, LUT, or OSD-CLUT table, subtract the following value from the maximum pixel rates.

- CLU: 170 kpixels × frame rate (fps)
  (Example: For a frame rate of 60 fps, 10.2 Mpixels/s)
- LUT: 4.5 kpixels × frame rate (fps)
  (Example: For a frame rate of 60 fps, 270 kpixels/s)
- OSD-CLUT (per RPF): 4.5 kpixels × frame rate (fps)
  (Example: For a frame rate of 60 fps, 270 kpixels/s)

(b) **Maximum performance of the VSPBS for frame rate**

- The maximum performance for frame rate per VSPBS interface is 120 fps.
- The total frame rate for all sequences that a single VSPBS interface processes through time division must be no greater than 120 fps.
(c) Procedure for deriving the maximum performance for pixel rate

Figure 5-11 shows the procedure for deriving the maximum performance of the VSPBS for pixel rate. For details of the conditions, refer to description in (d).

![Flowchart](image_url)

**Figure 5-11  Procedure for Deriving Maximum Performance of VSPBS for Pixel Rate**
(d) Detailed conditions for determining the maximum performance for pixel rate

Details of conditions 1 to 3 described in Figure 5-11 are given below.

Condition 1: Data are input in the specified format (format 1) with a separate alpha plane. 
This is the case where at least one RPF in the VSPBS is handling either of the following input formats.
  — 32-bpp ARGB + alpha plane
  — YCbCr planar + alpha plane

Condition 2: Data are input in the specified format (format 2) with a separate alpha plane. 
This is the case where at least one RPF in the VSPBS is handling either of the following input formats.
  — YCbCr4:4:4 semi-planar + alpha plane
  — YCbCr4:2:2 semi-planar + alpha plane

Condition 3: A specified condition is satisfied for YCbCr planar input. 
This is the case where the RPFs in the VSPBS satisfy the following condition.
  — Two RPFs are in the YCbCr planar format.
5.4.2 B) Concepts of Deriving Performance

(1) Concepts of Deriving Required Performance

The performance required of the VSPB and VSPBS is estimated from the display size on the output side. In blending, the size and allocation of input images must be selected such that all pixels are allocated within the output images.

The maximum number of planes of input images is 5 for the VSPB and 2 for the VSPBS.
(2) Estimating Required Performance for Pixel Rate

When the VSPB and VSPBS process several sequences, the VSPB and VSPBS switch between the sequences in frame units in a time division manner. In such cases, the following performance for pixel rate is required.

\[
\text{Required performance [pixel/s]} = \left( \sum_{i=0}^{i=N} \text{FrameSize}[i] \times \text{FrameRate}[i] \right)
\]

FrameSize[i]: Number of pixels per frame in the i-th sequence (number of pixels horizontally × number of lines)

FrameRate[i]: Frame rate (fps) for the output of images by the VSPB or VSPBS in the i-th sequence

N: Number of sequences to be processed by the VSPB or VSPBS

The required performance for pixel rate obtained from the above expression must not be greater than the maximum performance for pixel rate of the VSPB or VSPBS.


5.4.3 C) Concepts of Deriving Bandwidth

The times for processing by the VSPB and VSPBS IP modules depend on the required bandwidth value specified for a QoS parameter (refer to section 3.2, QoS Settings and IP Processing Time).

The required bandwidth can be calculated in three ways. The following shows the characteristics of each calculation method.

Table 5-13 Bandwidth Calculation Methods and Characteristics for the VSPB and VSPBS

<table>
<thead>
<tr>
<th>Required Bandwidth Calculation Method</th>
<th>Advantages and Disadvantages in Terms of Characteristics</th>
</tr>
</thead>
<tbody>
<tr>
<td>Case 1</td>
<td>Advantage: The VSPB and VSPBS IP modules operate at the maximum performance. Disadvantage: As the bandwidth required for the VSPB and VSPBS becomes large, the bandwidths that can be assigned to other IP modules are reduced.</td>
</tr>
<tr>
<td>Case 2 (recommended)</td>
<td>Recommended: Use this calculation to complete processing of the sequence having the highest frame rate within the period for one frame. Compared to case 1, the processing time becomes longer but larger bandwidths can be assigned to other IP modules. Note: If the calculated value is greater than that in case 1, the processing cannot be done while keeping the cycles at the maximum frame rate. In this case, use the value calculated in case 1.</td>
</tr>
<tr>
<td>Case 3</td>
<td>Disadvantage: The minimum bandwidth required to satisfy the frame rate defined for each sequence is assigned. Although the defined frame rate can be satisfied, processing for some sequences may not be completed within the period for one frame. Advantage: Compared to case 2, larger bandwidths can be assigned to other IP modules.</td>
</tr>
</tbody>
</table>
Figure 5-13 describes the terms and symbols used in the descriptions and expressions on the following pages.

### Terms and Symbols Used in Bandwidth Calculation Expressions for the VSPB and VSPBS

**Input plane**
- \( J_{\text{max}} \): Maximum number of input planes. 2 for the R-Car D3, 5 for the other LSI chips other than the R-Car D3.
- \( j \): Input plane number. Select one from among 0 to \( J_{\text{max}} - 1 \).
- \( \text{HORI}[j] \): Number of pixels horizontally in input plane \( j \)
- \( \text{VERT}[j] \): Number of lines in input plane \( j \)
- \( \text{BPP}[j] \): Color depth in input plane \( j \) (byte/pixel)

\[ \text{HORI}[j] \times \text{VERT}[j] \]: Number of pixels in input plane \( j \)

\[ \sum_{j=0}^{J_{\text{max}}-1} \text{BPP}[j] \]: Sum of input color depths

**Output plane**
- \( \text{HOzRout} \): Number of pixels horizontally in the output plane
- \( \text{VERTout} \): Number of lines in the output plane
- \( \text{BPPout} \): Color depth in the output plane (byte/pixel)

\[ \text{HOzRout} \times \text{VERTout} \]: Image size of output plane

### Equations

\[ \text{FrameRate} = \frac{\text{FrameRate}}{N} \]

\[ \text{MAX}_i = 0 \text{ to } N-1 : \text{Maximum value in the sequences} \]

\[ i: \text{Number for a sequence to be processed through time division} \]

\[ N: \text{Total number of sequences to be processed through time division} \]
The required bandwidth can be calculated in three ways as shown in Table 5-14. Select one from among cases 1 to 3 in the table.


### Table 5-14 Bandwidth Calculation Expressions for the VSPB and VSPBS

<table>
<thead>
<tr>
<th>Required Bandwidth Calculation Method</th>
<th>Read/Write</th>
<th>Description and Expression</th>
</tr>
</thead>
</table>
| Case 1                                | Read       | Description: \( \text{Maximum performance [Mpixel/s]} \times \text{(maximum of the sums of input color depths [byte/pixel])} \)  
Expression: \( (500 \text{ or } 125) \text{ [Mpixels/s]} \times \text{MAX} \text{ (\( \sum \text{BPPin[j]} \) [byte/pixel])} \)  
Write | Description: \( \text{Maximum performance [Mpixel/s]} \times \text{(maximum of the output color depths [byte/pixel])} \)  
Expression: \( (500 \text{ or } 125) \text{ [Mpixels/s]} \times \text{MAX} \text{ (BPPout) [byte/pixel]} \) |
| Case 2                                | Read       | Description: \( \text{\( \sum \) (number of pixels in output plane } \times \text{ sum of input color depths [byte/frame]) } \times \text{(maximum of the frame rates [fps])} \)  
Expression: \( \text{\( \sum \) (HORIout } \times \text{ VERTout } \times \text{\( \sum \text{BPPin[j]} \) [byte/frame]} \) } \times \text{MAX} \text{ (FrameRate) [fps]} \)  
Write | Description: \( \text{\( \sum \) (number of pixels in output plane } \times \text{ output color depth [byte/frame]) } \times \text{(maximum of the frame rates [fps])} \)  
Expression: \( \text{\( \sum \) (HORIout } \times \text{ VERTout } \times \text{BPPout) [byte/frame]} \) } \times \text{MAX} \text{ (FrameRate) [fps]} \) |
| Case 3                                | Read       | Description: \( \text{\( \sum \) (number of pixels in output plane [pixel/frame]} \) } \times \text{(sum of input color depths [byte/pixel]} \times \text{(frame rate [fps])} \)  
Expression: \( \text{\( \sum \) (\( \text{\( \sum \text{HORIout } \times \text{ VERTout} \times \text{\( \sum \text{BPPin[j]} \) [byte/pixel]} \) } \times \text{(FrameRate [fps])})} \)  
Write | Description: \( \text{\( \sum \) (number of pixels in output plane [pixel/frame]} \) } \times \text{(output color depth [byte/pixel]} \times \text{(frame rate [fps])} \)  
Expression: \( \text{\( \sum \) (\( \text{\( \sum \text{HORIout } \times \text{ VERTout} \times \text{BPPout} [byte/pixel]} \) } \times \text{(FrameRate [fps])})} \) |

Note: In case 2 or 3, if the calculated value is greater than the value calculated in case 1, the required frame rate cannot be satisfied. In this case, use case 1.
5.4.4 D) Examples of Bandwidth Calculation

(1) Version 1.1 of the R-Car M3-W

The following shows the calculation of required bandwidth in each case using an example where two sequences operate simultaneously at different frame rates.

Sequence 0: Blending two input planes and outputting Full HD at 60p
Sequence 1: Blending two input planes and outputting Full HD at 15p

Figure 5-14 Overview of Bandwidth Calculation Examples for VSPB
Case 1: To operate the IP module at the maximum performance

### Table 5-15 Examples of Bandwidth Calculation for VSPB (Case 1)

<table>
<thead>
<tr>
<th>Required Bandwidth Calculation Method</th>
<th>Read/Write</th>
<th>Description and Expression</th>
</tr>
</thead>
<tbody>
<tr>
<td>To operate the IP module at the maximum performance</td>
<td>Read</td>
<td>Description: {Maximum performance [Mpixel/s]} × (maximum of the sums of input color depths [byte/pixel]) &lt;br&gt;Expression: 500 [Mpixels/s] × (MAX_i (Σ BPPin[j]) [byte/pixel])&lt;br&gt;Example: 500 [Mpixels/s] × MAX ((4 + 2), (4 + 2)) [bytes/pixel] = 500 × (4 + 2) = 3000 [Mbytes/s]</td>
</tr>
</tbody>
</table>

When the required bandwidth calculated is specified for a QoS parameter, the IP module operates as shown in Figure 5-15.

![Figure 5-15 VSPB Operation with Sample QoS Setting (Case 1)](image-url)
- Case 2: To complete processing within the period for one frame

**Table 5-16  Examples of Bandwidth Calculation for VSPB (Case 2)**

<table>
<thead>
<tr>
<th>Required Bandwidth Calculation Method</th>
<th>Read/Write</th>
<th>Description and Expression</th>
</tr>
</thead>
<tbody>
<tr>
<td>Case 2 To complete processing within the period for one frame</td>
<td>Read</td>
<td>Description</td>
</tr>
<tr>
<td></td>
<td>Expression</td>
<td>$\sum (\text{HORIout} \times \text{VERTout} \times \sum \text{BPPin[j]}) [\text{byte/frame}] \times {\text{MAX (FrameRate) [fps]}}$</td>
</tr>
<tr>
<td></td>
<td>Example</td>
<td>${1920 \times 1080 \times (4 + 2) + 1920 \times 1080 \times (4 + 2) [\text{bytes/frame}]} \times 60 = 1500 [\text{Mbytes/s}]$</td>
</tr>
<tr>
<td></td>
<td>Write</td>
<td>Description</td>
</tr>
<tr>
<td></td>
<td>Expression</td>
<td>$\sum (\text{HORIout} \times \text{VERTout} \times \text{BPPout}) [\text{byte/frame}] \times {\text{MAX (FrameRate) [fps]}}$</td>
</tr>
<tr>
<td></td>
<td>Example</td>
<td>${1920 \times 1080 \times 4 + 1920 \times 1080 \times 4 [\text{bytes/frame}]} \times 60 [\text{fps}] = 1000 [\text{Mbytes/s}]$</td>
</tr>
</tbody>
</table>

When the required bandwidth calculated is specified for a QoS parameter, the IP module operates as shown in Figure 5-16.

**Figure 5-16  VSPB Operation with Sample QoS Setting (Case 2)**
• Case 3: To only satisfy the frame rate

### Table 5-17 Examples of Bandwidth Calculation for VSPB (Case 3)

<table>
<thead>
<tr>
<th>Required Bandwidth Calculation Method</th>
<th>Read/Write</th>
<th>Description and Expression</th>
</tr>
</thead>
<tbody>
<tr>
<td>Case 3: To only satisfy the frame rate</td>
<td>Read</td>
<td>Description: ( \sum ) {number of pixels in output plane [pixel/frame] \times {sum of input color depths [byte/pixel]} \times {frame rate [fps]})</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Expression: ( \sum {\text{HORIout} \times \text{VERTout}} \times {\sum \text{BPPin}[j] \times {\text{FrameRate [fps]}}} )</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Example: ((1920 \times 1080) \times 6 \times 60 \times \text{FrameRate [fps]} \times {\text{HORIout} \times \text{VERTout}})</td>
</tr>
<tr>
<td></td>
<td>Write</td>
<td>Description: ( \sum {\text{number of pixels in output plane [pixel/frame]} \times {\text{output color depth [byte/pixel]} \times {\text{frame rate [fps]}}} )</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Expression: ( \sum {\text{HORIout} \times \text{VERTout}} \times {\text{BPPout [byte/pixel]} \times {\text{FrameRate [fps]}}} )</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Example: ((1920 \times 1080) \times 4 \times 60 \times \text{FrameRate [fps]} \times {\text{HORIout} \times \text{VERTout}})</td>
</tr>
</tbody>
</table>

When the required bandwidth calculated is specified for a QoS parameter, the IP module operates as shown in Figure 5-17.

![Figure 5-17 VSPB Operation with Sample QoS Setting (Case 3)](image-url)
(2) **Version 2.0 and 3.0 of the R-Car H3**

The description on the examples of the bandwidth calculation is the same as that for version 1.1 of the R-Car M3-W. Refer to (1) Version 1.1 of the R-Car M3-W in this section.

(3) **Version 1.x of the R-Car M3-N**

The description on the examples of the bandwidth calculation is the same as that for version 1.1 of the R-Car M3-W. Refer to (1) Version 1.1 of the R-Car M3-W in this section.
(4) **Version 1.x of the R-Car E3**

The following shows the calculation of required bandwidth in each case using an example where two sequences operate simultaneously at different frame rates.

Sequence 0: Blending two input planes and outputting Full HD at 20p
Sequence 1: Blending two input planes and outputting Full HD at 10p

![Diagram]

**Figure 5-18  Overview of Bandwidth Calculation Examples for VSPB**
Case 1: To operate the IP module at the maximum performance

Table 5-18  Examples of Bandwidth Calculation for VSPB (Case 1)

<table>
<thead>
<tr>
<th>Required Bandwidth Calculation Method</th>
<th>Read/Write</th>
<th>Description and Expression</th>
</tr>
</thead>
</table>
| Case 1 To operate the IP module at the maximum performance | Read | Description: {Maximum performance [Mpixel/s]} \( \times \) \{maximum of the sums of input color depths [byte/pixel]\}  
Expression: \( 125 \; [\text{Mpixels/s}] \times \{\text{MAX}_i (\sum_j \text{BPPin}[j]) \; [\text{byte/pixel}]\} \)  
Example: \( 125 \; [\text{Mpixels/s}] \times \text{MAX}((4 + 2), (4 + 2)) \; [\text{bytes/pixel}] = 125 \times (4 + 2) = 750 \; [\text{Mbytes/s}] \) |
| | Write | Description: {Maximum performance [Mpixel/s]} \( \times \) \{maximum of the output color depths [byte/pixel]\}  
Expression: \( 125 \; [\text{Mpixels/s}] \times \{\text{MAX}_i (\text{BPPout}) \; [\text{byte/pixel}]\} \)  
Example: \( 125 \; [\text{Mpixels/s}] \times 4 \; [\text{bytes/pixel}] = 500 \; [\text{Mbytes/s}] \) |

When the required bandwidth calculated is specified for a QoS parameter, the IP module operates as shown in Figure 5-19.
• Case 2: To complete processing within the period for one frame

### Table 5-19 Examples of Bandwidth Calculation for VSPB (Case 2)

<table>
<thead>
<tr>
<th>Required Bandwidth Calculation Method</th>
<th>Read/Write</th>
<th>Description and Expression</th>
</tr>
</thead>
</table>
| Case 2                                | Read       | Description \[\sum_i \text{(number of pixels in output plane } \times \text{ sum of input color depths)} \text{[byte/frame]} \times \{\text{maximum of the frame rates [fps]}\}\
|                                       |            | Expression \[\sum_i \text{(HORI}_{\text{out}} \times \text{VERT}_{\text{out}} \times \sum_j \text{BPP}_{\text{in}}[j]) \text{[byte/frame]} \times \{\text{MAX}_i \text{(FrameRate) [fps]}\}\
|                                       | Example    | 1920 \times 1080 \times (4 + 2) + 1920 \times 1080 \times (4 + 2) \text{[bytes/frame]} \times 20 = 500 \text{[Mbytes/s]} |
|                                       | Write      | Description \[\sum_i \text{(number of pixels in output plane } \times \text{ output color depth)} \text{[byte/frame]} \times \{\text{maximum of the frame rates [fps]}\}\
|                                       |            | Expression \[\sum_i \text{(HORI}_{\text{out}} \times \text{VERT}_{\text{out}} \times \text{BPP}_{\text{out}}) \text{[byte/frame]} \times \{\text{MAX}_i \text{(FrameRate) [fps]}\}\
|                                       | Example    | 1920 \times 1080 \times 4 + 1920 \times 1080 \times 4 \text{[bytes/frame]} \times 20 \text{[fps]} = 333 \text{[Mbytes/s]} |

When the required bandwidth calculated is specified for a QoS parameter, the IP module operates as shown in Figure 5-20.

---

**Figure 5-20** VSPB Operation with Sample QoS Setting (Case 2)
Table 5-20  Examples of Bandwidth Calculation for VSPB (Case 3)

<table>
<thead>
<tr>
<th>Required Bandwidth Calculation Method</th>
<th>Read/Write</th>
<th>Description and Expression</th>
</tr>
</thead>
<tbody>
<tr>
<td>Case 3</td>
<td>Read</td>
<td>Description: ( \sum_i \left( \frac{\text{number of pixels in output plane}}{\text{pixel/frame}} \times { \text{sum of input color depths} \ [\text{byte/pixel}] \times \text{frame rate} \ [\text{fps}] } \right) )</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Expression: ( \sum_i \left( \frac{\text{HORiout} \times \text{VERTiout}}{\text{pixel/frame}} \times \left( \sum_j \text{BPPi}[j] \ [\text{byte/pixel}] \times \text{FrameRate} \ [\text{fps}] \right) \right) )</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Example: ( (1920 \times 1080) \ [\text{pixels/frame}] \times 6 \ [\text{bytes/pixel}] \times 20 \ [\text{fps}] + (1920 \times 1080) \times 6 \times 10 = 375 \ [\text{Mbytes/s}] )</td>
</tr>
<tr>
<td></td>
<td>Write</td>
<td>Description: ( \sum_i \left( \frac{\text{number of pixels in output plane}}{\text{pixel/frame}} \times { \text{output color depth} \ [\text{byte/pixel}] \times \text{frame rate} \ [\text{fps}] } \right) )</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Expression: ( \sum_i \left( \frac{\text{HORiout} \times \text{VERTiout}}{\text{pixel/frame}} \times \text{BPPout} \ [\text{byte/pixel}] \times \text{FrameRate} \ [\text{fps}] \right) )</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Example: ( (1920 \times 1080) \ [\text{pixels/frame}] \times 4 \ [\text{bytes/pixel}] \times 20 \ [\text{fps}] + (1920 \times 1080) \times 4 \times 10 = 250 \ [\text{Mbytes/s}] )</td>
</tr>
</tbody>
</table>

When the required bandwidth calculated is specified for a QoS parameter, the IP module operates as shown in Figure 5-21.
(5) **Version 1.x of the R-Car D3**

The description on the examples of the bandwidth calculation is the same as that for version 1.x of the R-Car E3. Refer to (4) **Version 1.x of the R-Car E3** in this section. Read references to “VSPB” as “VSPBS” in the case of these devices.
5.5 VSPI

Version 1.x R-Car D3 devices do not have the VSPI module. This section is not applicable to version 1.x R-Car D3 devices.

5.5.1 A) Maximum Performance

(1) Version 1.1 of the R-Car M3-W

Performance of the VSPI required for a use case must satisfy both conditions (a) and (b) for the maximum performance of the VSPI described below.

(a) Maximum performance of the VSPI for pixel rate

The maximum performance per VSPI interface for pixel rate is given below.

- When none of conditions 1 to 3 shown in Figure 5-22 are met:
  - 500 Mpixels/s (equivalent to Full HD at 240 fps)
- When any of conditions 1 to 3 shown in Figure 5-22 is met:
  - 375 Mpixels/s (equivalent to Full HD at 180 fps)

(b) Maximum performance of the VSPI for frame rate

- The maximum performance for frame rate per VSPI interface is 480 fps.
- The total frame rate for all sequences that a single VSPI interface processes through time division must be no greater than 480 fps.
(c) Procedure for deriving the maximum performance for pixel rate

Figure 5-22 shows the procedure for deriving the maximum performance of the VSPI for pixel rate. For details of the conditions, refer to description in (d).

![Diagram](image)

**Figure 5-22 Procedure for Deriving Maximum Performance of VSPI for Pixel Rate**
(d) Detailed conditions for determining the maximum performance for pixel rate

Details of conditions 1 to 3 described in Figure 5-22 are given below.

- **Condition 1:** A specified condition is satisfied for input in a format with a separate alpha plane.
  This is the case where the VSPI is handling any of the following input formats.
  - YCbCr 4:4:4 semi-planar + alpha plane
  - 32-bpp ARGB + alpha plane
  - YCbCr planar + alpha plane

- **Condition 2:** Rotation or flipping is in use.
  This is the case where the VSPI is proceeding with 90- or 270-degree rotation (VI6_WPF0_OUTFMT.ROT* > 3).

- **Condition 3:** The up-down scaler (UDS) is in use with the super resolution unit (SRU) with no scaling and the horizontal scaling rate is greater than 4.
  This is the case where the UDS and SRU in the VSPI are used together and the following conditions are both satisfied.
  - The horizontal scaling rate is set to a value greater than 4 in the UDS.
  - The super resolution mode is set to super resolution without scaling in the SRU.

Note: * A register in the VSPI. For details, refer to section 32, Video Signal Processor (VSP2), in the hardware manual.

(2) **Version 2.0 and 3.0 of the R-Car H3**

The description on the maximum performance of the VSPI is the same as that for version 1.1 of the R-Car M3-W. Refer to (1) Version 1.1 of the R-Car M3-W in this section.

(3) **Version 1.x of the R-Car M3-N**

The description on the maximum performance of the VSPI is the same as that for version 1.1 of the R-Car M3-W. Refer to (1) Version 1.1 of the R-Car M3-W in this section.

(4) **Version 1.x of the R-Car E3**

Performance of the VSPI required for a use case must satisfy both conditions (a) and (b) for the maximum performance of the VSPI described below.

(a) **Maximum performance of the VSPI for pixel rate**

The maximum performance per VSPI interface for pixel rate is given below.

- When none of conditions 1 to 3 shown in Figure 5-23 are met:
  - 125 Mpixels/s (equivalent to Full HD at 60 fps)
- When any of conditions 1 to 3 shown in Figure 5-23 is met:
  - 93.75 Mpixels/s (equivalent to Full HD at 45 fps)

(b) **Maximum performance of the VSPI for frame rate**

- The maximum performance for frame rate per VSPI interface is 120 fps.
- The total frame rate for all sequences that a single VSPI interface processes through time division must be no greater than 120 fps.
Procedure for deriving the maximum performance for pixel rate

Figure 5-23 shows the procedure for deriving the maximum performance of the VSPI for pixel rate. For details of the conditions, refer to description in (d).

![Procedure for Deriving Maximum Performance of VSPI for Pixel Rate](image)

Figure 5-23 Procedure for Deriving Maximum Performance of VSPI for Pixel Rate
(d) Detailed conditions for determining the maximum performance for pixel rate

Details of conditions 1 to 3 described in Figure 5-23 are given below.

- **Condition 1:** A specified condition is satisfied for input in a format with a separate alpha plane.  
  This is the case where the VSPI is handling any of the following input formats.
  - YCbCr4:4:4 semi-planar + alpha plane
  - 32-bpp ARGB + alpha plane
  - YCbCr planar + alpha plane

- **Condition 2:** Rotation or flipping is in use.  
  This is the case where the VSPI is proceeding with 90- or 270-degree rotation (VI6_WPF0_OUTFMT.ROT* > 3).

- **Condition 3:** The up-down scaler (UDS) is in use with the super resolution unit (SRU) with no scaling and the horizontal scaling rate is greater than 4.  
  This is the case where the UDS and SRU in the VSPI are used together and the following conditions are both satisfied.
  - The horizontal scaling rate is set to a value greater than 4 in the UDS.
  - The super resolution mode is set to super resolution without scaling in the SRU.

Note: * A register in the VSPI. For details, refer to section 32, Video Signal Processor (VSP2), in the hardware manual.
### 5.5.2 B) Concepts of Deriving Performance

#### (1) Concepts of Deriving Required Performance

To estimate the performance in processing by the VSPI, use the combination of the greater values of the horizontal and vertical sizes from among those of the input, intermediate, and output images. This is because some processing such as scaling images may lead to differences among the sizes of the input, intermediate, and output images as shown in Figure 5-24. When the sizes of the input, intermediate, and output images are the same, base the estimate on the size of the output image. Note that the size of the intermediate image should only be used in estimation only when SRU with scaling-up by 2 is in use.

- **(a)** When the horizontal and vertical sizes of the output image are used in estimation:

- **(b)** When the horizontal size of the input image and the vertical size of the output image are used in estimation:

- **(c)** When the horizontal size of the output image and the vertical size of the intermediate image are used in estimation:

> Figure 5-24 Estimation of VSPI Performance
(2) Estimating Required Performance for Pixel Rate

When the VSPI processes several sequences, the VSPI switches between the sequences in frame units in a time division manner. In such cases, the following performance for pixel rate is required.

\[
\text{Required performance [pixel/s]} = \left( \sum_{i=0}^{i<N} (\text{FrameSize}[i] \times \text{FrameRate}[i]) \right)
\]

- \(\text{FrameSize}[i]\): Greater horizontal size \(\times\) greater vertical size (pixels per frame) of the images input to and output from the VSPI in the \(i\)-th sequence
- \(\text{FrameRate}[i]\): Frame rate (fps) for output images from the VSPI in the \(i\)-th sequence
- \(N\): Number of sequences to be processed by the VSPI

The required performance for pixel rate obtained from the above expression must not be greater than the maximum performance for pixel rate of the VSPI.
5.5.3 C) Concepts of Deriving Bandwidth

The times for processing by the VSPI IP module depend on the required bandwidth value specified for a QoS parameter (refer to section 3.2, QoS Settings and IP Processing Time). The required bandwidth can be calculated in three ways. The following shows the characteristics of each calculation method.

Table 5-21 VSPI Bandwidth Calculation Methods and Characteristics

<table>
<thead>
<tr>
<th>Required Bandwidth Calculation Method</th>
<th>Advantages and Disadvantages in Terms of Characteristics</th>
</tr>
</thead>
</table>
| **Case 1** To operate the IP module at the maximum performance | **Advantage:** The VSPI IP module operates at the maximum performance.  
**Disadvantage:** As the bandwidth required for the VSPI becomes large, the bandwidths that can be assigned to other IP modules are reduced. |
| **Case 2 (recommended)** To complete processing within the period for one frame | **Recommended:** Use this calculation to complete processing of the sequence having the highest frame rate within the period for one frame.  
Compared to case 1, the processing time becomes longer but larger bandwidths can be assigned to other IP modules.  
**Note:** If the calculated value is greater than that in case 1, the processing cannot be done while keeping the cycles at the maximum frame rate. In this case, use the value calculated in case 1. |
| **Case 3** To only satisfy the frame rate | **Disadvantage:** The minimum bandwidth required to satisfy the frame rate defined for each sequence is assigned. Although the defined frame rate can be satisfied, processing for some sequences may not be completed within the period for one frame.  
**Advantage:** Compared to case 2, larger bandwidths can be assigned to other IP modules. |
Figure 5-25 describes the terms and symbols used in the descriptions and expressions on the following pages. When a frame is divided into areas, the bandwidth varies with the content being processed and therefore cannot be defined accurately with the expressions given. Only use the expressions for rough calculation of the bandwidth, and use the attached video and display bandwidth calculation sheet for the precise calculation.

![Figure 5-25 Terms and Symbols Used in VSPI Bandwidth Calculation](image)

**Input plane**
- HORI<sub>in</sub>: Number of pixels horizontally in the input plane
- VERT<sub>in</sub>: Number of lines in the input plane
- BPP<sub>in</sub>: Color depth in the input plane (byte/pixel)
- HORIDIV<sub>in</sub>: Number of pixels horizontally in the input plane (when divided into areas)
  \[= \text{HORI}_{in} \times 1.1 \]  
- Image size of input plane (when divided into areas):
  \[= \text{HORI}_{IDIV} \times \text{VERT}_{in} \]

**Output plane**
- HORI<sub>out</sub>: Number of pixels horizontally in the output plane
- VERT<sub>out</sub>: Number of lines in the output plane
- BPP<sub>out</sub>: Color depth in the output plane (byte/pixel)

Notes:
1. When scaling, super-resolution processing, or 90-degree rotation is enabled, the VSPI divides each frame vertically into areas and handles the frame in area units. In this case, the input images of the divided areas overlap with each other, which leads to the bandwidth being greater than that for processing without division. The number of areas into which a frame is divided and the size of the overlaps in the input images vary with the processing.
2. The value 1.1 is a coefficient for rough calculation: it may differ from the actual value, which varies with the content being processed.
The required bandwidth can be calculated in three ways. Select one from among cases 1 to 3.


### Table 5-22 VSPI Bandwidth Calculation Expressions

<table>
<thead>
<tr>
<th>Required Bandwidth Calculation Method</th>
<th>Read/Write</th>
<th>Description and Expression</th>
</tr>
</thead>
</table>
| **Case 1** To operate the IP module at the maximum performance | Read | Description: \( \{ \text{Maximum performance} \ [\text{Mpixel/s}] \} \times \{ \text{maximum of the input color depths} \ [\text{byte/pixel}] \} \)
Expression: \((500 \text{ or } 125) \ [\text{Mpixels/s}] \times (\text{MAX}_i (\text{BPPin}) \ [\text{byte/pixel}]) \)
| Write | Description: \( \{ \text{Maximum performance} \ [\text{Mpixel/s}] \} \times \{ \text{maximum of the output color depths} \ [\text{byte/pixel}] \} \)
Expression: \((500 \text{ or } 125) \ [\text{Mpixels/s}] \times (\text{MAX}_i (\text{BPPout}) \ [\text{byte/pixel}]) \)
| **Case 2** To complete processing within the period for one frame | Read | Description: \( \{ \text{SUM}_i \ (\text{number of pixels in input plane} \times \text{input color depth} \ [\text{byte/frame}]) \times \{ \text{maximum of the frame rates} \ [\text{fps}] \} \)
Expression: \( \{ \text{SUM}_i \ (\text{HORIDIVin} \times \text{VERTin} \times \text{BPPin}) \ [\text{byte/frame}] \} \times (\text{MAX}_i (\text{FrameRate}) \ [\text{fps}] \)
| Write | Description: \( \{ \text{SUM}_i \ (\text{number of pixels in output plane} \times \text{output color depth} \ [\text{byte/frame}]) \times \{ \text{maximum of the frame rates} \ [\text{fps}] \} \)
Expression: \( \{ \text{SUM}_i \ (\text{HORIout} \times \text{VERTout} \times \text{BPPout}) \ [\text{byte/frame}] \} \times (\text{MAX}_i (\text{FrameRate}) \ [\text{fps}] \)
| **Case 3** To only satisfy the frame rate | Read | Description: \( \{ \text{SUM}_i \ (\text{number of pixels in input plane} \times \text{input color depth} \ [\text{byte/pixel}] \times \{ \text{frame rate} \ [\text{fps}] \} \)
Expression: \( \{ \text{SUM}_i \ ((\text{HORIDIVin} \times \text{VERTin}) \ [\text{pixel/frame}] \times \text{BPPin} \ [\text{byte/pixel}]) \times \{ \text{FrameRate} \ [\text{fps}] \} \)
| Write | Description: \( \{ \text{SUM}_i \ (\text{number of pixels in output plane} \times \text{output color depth} \ [\text{byte/pixel}] \times \{ \text{frame rate} \ [\text{fps}] \} \)
Expression: \( \{ \text{SUM}_i \ ((\text{HORIout} \times \text{VERTout}) \ [\text{pixel/frame}] \times \text{BPPout} \ [\text{byte/pixel}]) \times \{ \text{FrameRate} \ [\text{fps}] \} \)

**Note:** In case 2 or 3, if the calculated value is greater than the value calculated in case 1, the required frame rate cannot be satisfied. In this case, use case 1.
5.5.4 D) Example of Bandwidth Calculation

(1) Version 1.1 of the R-Car M3-W

The following shows the calculation of required bandwidth in each case using an example where two sequences operate simultaneously at different frame rates.

Sequence 0: Scaling an input image of $680 \times 480$ pixels and outputting Full HD at 60p
Sequence 1: Scaling an input image of Full HD and outputting $680 \times 480$ pixels at 15p

---

**Figure 5-26 Overview of Bandwidth Calculation Examples for VSPI**
- Case 1: To operate the IP module at the maximum performance

**Table 5-23  Examples of Bandwidth Calculation for VSPI (Case 1)**

<table>
<thead>
<tr>
<th>Required Bandwidth Calculation Method</th>
<th>Read/Write</th>
<th>Description and Expression</th>
</tr>
</thead>
<tbody>
<tr>
<td>Case 1</td>
<td>Read</td>
<td>(Maximum performance [Mpixel/s]) \times (maximum of the input color depths [byte/pixel])</td>
</tr>
<tr>
<td>To operate the IP module at the maximum performance</td>
<td>Expression</td>
<td>(500 \text{ [Mpixels/s]} \times \text{MAX}(\text{BPPin})\text{ [byte/pixel]})</td>
</tr>
<tr>
<td></td>
<td>Example</td>
<td>(500 \text{ [Mpixels/s]} \times \text{MAX}(4, 4)\text{ [bytes/pixel]} = 500 \times 4 = 2000\text{ [Mbytes/s]})</td>
</tr>
<tr>
<td></td>
<td>Write</td>
<td>(Maximum performance [Mpixel/s]) \times (maximum of the output color depths [byte/pixel])</td>
</tr>
<tr>
<td></td>
<td>Expression</td>
<td>(500 \text{ [Mpixels/s]} \times \text{MAX}(\text{BPPout})\text{ [byte/pixel]})</td>
</tr>
<tr>
<td></td>
<td>Example</td>
<td>(500 \text{ [Mpixels/s]} \times \text{MAX}(4, 4)\text{ [bytes/pixel]} = 500 \times 4 = 2000\text{ [Mbytes/s]})</td>
</tr>
</tbody>
</table>

When the required bandwidth calculated is specified for a QoS parameter, the IP module operates as shown in Figure 5-27.

![Figure 5-27  VSPI Operation with Sample QoS Setting (Case 1)](image-url)


- Case 2: To complete processing within the period for one frame

### Table 5-24 Examples of Bandwidth Calculation for VSPI (Case 2)

<table>
<thead>
<tr>
<th>Required Bandwidth Calculation Method</th>
<th>Read/Write</th>
<th>Description and Expression</th>
</tr>
</thead>
</table>
| Case 2: To complete processing within the period for one frame | Read       | Description: \[\sum_{i} (\text{number of pixels in input plane (divided into areas)} \times \text{input color depth}) \times \text{maximum of the frame rates [fps]}\]  
Expression: \[\sum_{i} (\text{HORIDIVin} \times \text{VERTin} \times \text{BPPin}) \times \text{MAXi (FrameRate) [fps]}\]  
Example: \(640 \times 1.1 \times 480 \times 4 + 1920 \times 1.1 \times 1080 \times 4 \text{ [bytes/frame]} \times 60 \approx 629 \text{ [Mbytes/s]}\] |
|                                      | Write      | Description: \[\sum_{i} (\text{number of pixels in output plane} \times \text{output color depth}) \times \text{maximum of the frame rates [fps]}\]  
Expression: \[\sum_{i} (\text{HORIout} \times \text{VERTout} \times \text{BPPout}) \times \text{MAXi (FrameRate) [fps]}\]  
Example: \(1920 \times 1080 \times 4 + 640 \times 480 \times 4 \text{ [bytes/frame]} \times 60 \approx 571 \text{ [Mbytes/s]}\) |

When the required bandwidth calculated is specified for a QoS parameter, the IP module operates as shown in Figure 5-28.
Case 3: To only satisfy the frame rate

### Table 5-25  Examples of Bandwidth Calculation for VSPI (Case 3)

<table>
<thead>
<tr>
<th>Required Bandwidth Calculation Method</th>
<th>Read/Write</th>
<th>Description and Expression</th>
</tr>
</thead>
</table>
| Case 3  
To only satisfy the frame rate      | Read       | Description: \( \sum \{(\text{number of pixels in input plane (divided into areas)} \times \text{input color depth}) \times \text{frame rate}\} \)  

Expression: \( \sum \{((\text{HORIDIVin} \times \text{VERTin}) \times \text{BPPin}) \times \text{frame rate}\} \)

**Example**  
\((640 \times 1.1 \times 480) \times 4 \times 60 + (1920 \times 1.1 \times 1080) \times 4 \times 15 \approx 218 \text{ [Mbyte/s]}\)

|                         | Write      | Description: \( \sum \{(\text{number of pixels in output plane}) \times \text{output color depth}) \times \text{frame rate}\} \)  

Expression: \( \sum \{((\text{HORIout} \times \text{VERTout}) \times \text{BPPout}) \times \text{frame rate}\} \)

**Example**  
\((1920 \times 1080) \times 4 \times 60 + (640 \times 480) \times 4 \times 15 \approx 516 \text{ [Mbyte/s]}\)

When the required bandwidth calculated is specified for a QoS parameter, the IP module operates as shown in Figure 5-29.

![Figure 5-29  VSPI Operation with Sample QoS Setting (Case 3)](image-url)
(2) **Version 2.0 and 3.0 of the R-Car H3**

The description on the examples of the bandwidth calculation is the same as that for version 1.1 of the R-Car M3-W. Refer to (1) Version 1.1 of the R-Car M3-W in this section.

(3) **Version 1.x of the R-Car M3-N**

The description on the examples of the bandwidth calculation is the same as that for version 1.1 of the R-Car M3-W. Refer to (1) Version 1.1 of the R-Car M3-W in this section.
(4) Version 1.x of the R-Car E3

The following shows the calculation of required bandwidth in each case using an example where two sequences operate simultaneously at different frame rates.

Sequence 0: Scaling an input image of 680 \times 480 \text{ pixels} and outputting Full HD at 30p

Sequence 1: Scaling an input image of Full HD and outputting 680 \times 480 \text{ pixels} at 10p

\begin{figure}
\centering
\includegraphics[width=\textwidth]{image}
\caption{Overview of Bandwidth Calculation Examples for VSPI}
\end{figure}
Case 1: To operate the IP module at the maximum performance

### Table 5-26  Examples of Bandwidth Calculation for VSPI (Case 1)

<table>
<thead>
<tr>
<th>Required Bandwidth Calculation Method</th>
<th>Read/Write</th>
<th>Description and Expression</th>
<th>Example</th>
</tr>
</thead>
<tbody>
<tr>
<td>Case 1</td>
<td>Read</td>
<td>Description {Maximum performance [Mpixel/s]} × {maximum of the input color depths [byte/pixel]}</td>
<td>125 [Mpixels/s] × MAXi (BPPin) [byte/pixel] = 125 × 4 = 500 [Mbytes/s]</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Expression 125 [Mpixels/s] × MAXi (BPPin) [byte/pixel]</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Write</td>
<td>Description {Maximum performance [Mpixel/s]} × {maximum of the output color depths [byte/pixel]}</td>
<td>125 [Mpixels/s] × MAXi (BPPout) [byte/pixel] = 125 × 4 = 500 [Mbytes/s]</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Expression 125 [Mpixels/s] × MAXi (BPPout) [byte/pixel]</td>
<td></td>
</tr>
</tbody>
</table>

When the required bandwidth calculated is specified for a QoS parameter, the IP module operates as shown in Figure 5-31.

![Figure 5-31  VSPI Operation with Sample QoS Setting (Case 1)](image-url)
Case 2: To complete processing within the period for one frame

Table 5-27 Examples of Bandwidth Calculation for VSPI (Case 2)

<table>
<thead>
<tr>
<th>Required Bandwidth Calculation Method</th>
<th>Read/Write</th>
<th>Description and Expression</th>
</tr>
</thead>
<tbody>
<tr>
<td>Case 2</td>
<td>Read</td>
<td>Description: ( \sum_i (\text{number of pixels in input plane (divided into areas) } \times \text{input color depth}) \text{ [byte/frame]} \times {\text{maximum of the frame rates [fps]}} )</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Expression: ( \sum_i (\text{HORIDIVin } \times \text{VERTin } \times \text{BPPin}) \text{ [byte/frame]} \times {\text{MAXi (FrameRate) [fps]}} )</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Example: ( 640 \times 1.1 \times 480 \times 4 + 1920 \times 1.1 \times 1080 \times 4 \text{ [bytes/frame]} \times 30 \approx 315 \text{ [Mbytes/s]} )</td>
</tr>
<tr>
<td></td>
<td>Write</td>
<td>Description: ( \sum_i (\text{number of pixels in output plane } \times \text{output color depth}) \text{ [byte/frame]} \times {\text{maximum of the frame rates [fps]}} )</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Expression: ( \sum_i (\text{HORIout } \times \text{VERTout } \times \text{BPPout}) \text{ [byte/frame]} \times {\text{MAXi (FrameRate) [fps]}} )</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Example: ( 1920 \times 1080 \times 4 + 640 \times 480 \times 4 \text{ [bytes/frame]} \times 30 \approx 286 \text{ [Mbytes/s]} )</td>
</tr>
</tbody>
</table>

When the required bandwidth calculated is specified for a QoS parameter, the IP module operates as shown in Figure 5-32.

![Figure 5-32 VSPI Operation with Sample QoS Setting (Case 2)]
- Case 3: To only satisfy the frame rate

### Table 5-28   Examples of Bandwidth Calculation for VSPI (Case 3)

<table>
<thead>
<tr>
<th>Required Bandwidth Calculation Method</th>
<th>Read/Write</th>
<th>Description and Expression</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Case 3</strong></td>
<td>Read</td>
<td>Description: ( \sum_i \left( \text{number of pixels in input plane (divided into areas)} \times \text{input color depth} \times \text{frame rate} \right) )</td>
</tr>
<tr>
<td><strong>To only satisfy the frame rate</strong></td>
<td>Read</td>
<td>Expression: ( \sum_i \left( \text{(HORIDIVin \times VERTin)} \times \text{BPPin} \times \text{FrameRate} \right) )</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Example: ( (640 \times 1.1 \times 480) \times 4 \times 30 \approx 132 ) [Mbytes/s]</td>
</tr>
<tr>
<td></td>
<td>Write</td>
<td>Description: ( \sum_i \left( \text{number of pixels in output plane} \times \text{output color depth} \times \text{frame rate} \right) )</td>
</tr>
<tr>
<td></td>
<td>Write</td>
<td>Expression: ( \sum_i \left( \text{(HORIout \times VERTout)} \times \text{BPPout} \times \text{FrameRate} \right) )</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Example: ( (1920 \times 1080) \times 4 \times 30 \approx 261 ) [Mbytes/s]</td>
</tr>
</tbody>
</table>

When the required bandwidth calculated is specified for a QoS parameter, the IP module operates as shown in Figure 5-33.

![Figure 5-33  VSPI Operation with Sample QoS Setting (Case 3)](image-url)
5.6  VCP4 and iVDP1C

Version 1.x R-Car D3 devices do not have the VCP4 and iVDP1C modules. This section is not applicable to version 1.x R-Car D3 devices.

5.6.1  A) Maximum Performance

Performance of the VCP4 and iVDP1C required for a use case must satisfy both conditions (1) and (2) for the maximum performance of the VCP4 and iVDP1C described below.

(1)  **Maximum Performance for Pixel Rate**

Refer to (3) Maximum Performance for Pixel Rate of the VCP4 and (4) Maximum Performance for Pixel Rate of the iVDP1C.

(2)  **Maximum Performance for Frame Rate**

- The maximum performance for frame rate per VCP4 or iVDP1C interface is 240 fps.
- The total frame rate for all sequences that a single VCP4 or iVDP1C interface processes through time division must be no greater than 240 fps.
- Even if parallel operation of the VCPLF and VDPB is enabled in the VCP4, the maximum performance for frame rate is 240 fps.

Definition of a term used in this section:

- **Another codec**: A codec supported by the VCP4 but other than the H.264, H.265, VP9, and RealVideo codecs
(3) Maximum Performance for Pixel Rate of the VCP4

(a) Version 2.0 and 3.0 of the R-Car H3, version 1.1 of the R-Car M3-W, version 1.x of the R-Car M3-N (other than when in use with a VP9 codec)

**When iVDP1C is in use**

The maximum performance values for pixel rate of the VCP4 when the iVDP1C is in use are given in Table 5-29.

The maximum performance values depend on the combinations of codecs. There are four possible combinations in terms of the maximum performance values as listed in Table 5-29. For cases 3 and 4, the combination of the codecs is the same, but the difference is that the higher processing performance is assigned to another codec in case 3, and to an H.264 or H.265 codec in case 4. The combination of a RealVideo codec and another codec cannot be used.

### Table 5-29 Maximum Performance Values for Pixel Rate of VCP4 (When iVDP1C is in Use)

<table>
<thead>
<tr>
<th>Case</th>
<th>Maximum Performance of an H.264 or H.265 Codec (Mpixel/s)</th>
<th>Maximum Performance of a RealVideo Codec (Mpixel/s)</th>
<th>Maximum Performance of Another Codec (Mpixel/s)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Case 1</td>
<td>250.7 (1920 × 1088 at 120 fps)</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>Case 2</td>
<td>62.67 (1920 × 1088 at 30 fps)</td>
<td>62.67 (1920 × 1088 at 30 fps)</td>
<td>0</td>
</tr>
<tr>
<td>Case 3</td>
<td>62.67 (1920 × 1088 at 30 fps)</td>
<td>0</td>
<td>125.3 (1920 × 1088 at 60 fps)</td>
</tr>
<tr>
<td>Case 4</td>
<td>125.3 (1920 × 1088 at 60 fps)</td>
<td>0</td>
<td>62.67 (1920 × 1088 at 30 fps)</td>
</tr>
</tbody>
</table>

**Notes:**
1. An image is compressed or decompressed in units of 16 × 16 blocks based on image compression standard. Accordingly, the image size should be rounded up to the nearest multiple of 16 when calculating the maximum performance value.
2. Even when only a RealVideo codec is in use, the maximum performance is 62.67 Mpixels/s.
3. Even when only another codec is in use, the maximum performance is 125.3 Mpixel/s.
When iVDP1C is not in use

The maximum performance values for pixel rate of the VCP4 when the iVDP1C is not in use are given in Table 5-30. The maximum performance values depend on the combinations of codecs. There are four possible combinations in terms of the maximum performance values as listed in Table 5-30. For case 3 and case 4, the combination of the codecs is the same, but the difference is that the higher processing performance is assigned to another codec in case 3, and to an H.264 or H.265 codec in case 4. The combination of a RealVideo codec and another codec cannot be used.

Table 5-30  Maximum Performance Values for Pixel Rate of VCP4 (When iVDP1C is Not in Use)

<table>
<thead>
<tr>
<th>Case</th>
<th>Maximum Performance of an H.264 Codec (Mpixel/s)</th>
<th>Maximum Performance of a RealVideo Codec (Mpixel/s)</th>
<th>Maximum Performance of Another Codec (Mpixel/s)</th>
<th>Maximum Performance of an H.265 Codec (Mpixel/s)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Case 1</td>
<td>250.7 (1920 × 1088 at 120 fps)</td>
<td>0</td>
<td>0</td>
<td>250.7 (1920 × 1088 at 120 fps)</td>
</tr>
<tr>
<td>Case 2</td>
<td>62.67 (1920 × 1088 at 30 fps)</td>
<td>62.67 (1920 × 1088 at 30 fps)</td>
<td>0</td>
<td>250.7 (1920 × 1088 at 120 fps)</td>
</tr>
<tr>
<td>Case 3</td>
<td>62.67 (1920 × 1088 at 30 fps)</td>
<td>0</td>
<td>125.3 (1920 × 1088 at 60 fps)</td>
<td>250.7 (1920 × 1088 at 120 fps)</td>
</tr>
<tr>
<td>Case 4</td>
<td>125.3 (1920 × 1088 at 60 fps)</td>
<td>0</td>
<td>62.67 (1920 × 1088 at 30 fps)</td>
<td>250.7 (1920 × 1088 at 120 fps)</td>
</tr>
</tbody>
</table>

Notes:
1. An image is compressed or decompressed in units of 16 × 16 blocks based on image compression standard. Accordingly, the image size should be rounded up to the nearest multiple of 16 when calculating the maximum performance value.
2. When only a RealVideo codec is in use, the maximum performance is 125.3 Mpixe/s.
3. Even when only another codec is in use, the maximum performance is 125.3 Mpixe/s.

Figure 5-35  Maximum Performance Values for Pixel Rate of VCP4 (When iVDP1C is Not in Use)
(b) Version 1.x of the R-Car M3-N (when in use with a VP9 codec)

When iVDP1C is in use

The maximum performance values for pixel rate of the VCP4 when in use with a VP9 codec and the iVDP1C is in use are given in Table 5-31.

The maximum performance values depend on the combinations of codecs. There are three possible combinations in terms of the maximum performance values as listed in Table 5-31.

Table 5-31  Maximum Performance Values for Pixel Rate of VCP4 (When in Use with a VP9 Codec and the iVDP1C is in Use)

<table>
<thead>
<tr>
<th>Case</th>
<th>Maximum Performance of an H.264 Codec (Mpixel/s)</th>
<th>Maximum Performance of a VP9 Codec (Mpixel/s)</th>
<th>Maximum Performance of Another Codec (Mpixel/s)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Case 1</td>
<td>0</td>
<td>125.3 (1920 × 1088 at 60 fps)*</td>
<td>0</td>
</tr>
<tr>
<td>Case 2</td>
<td>125.3 (1920 × 1088 at 60 fps)</td>
<td>62.67 (1920 × 1088 at 30 fps)</td>
<td>0</td>
</tr>
<tr>
<td>Case 3</td>
<td>0</td>
<td>62.67 (1920 × 1088 at 30 fps)</td>
<td>62.67 (1920 × 1088 at 30 fps)</td>
</tr>
</tbody>
</table>

Note: * An image is compressed or decompressed in units of 16 × 16 blocks based on image compression standard. Accordingly, the image size should be rounded up to the nearest multiple of 16 when calculating the maximum performance value.

Figure 5-36  Maximum Performance Values for Pixel Rate of VCP4 (When in Use with a VP9 Codec and the iVDP1C is in Use)
When iVDP1C is not in use

The maximum performance values for pixel rate of the VCP4 when in use with a VP9 codec and the iVDP1C is not in use are given in Table 5-32. The maximum performance values depend on the combinations of codecs. There are eight possible combinations in terms of the maximum performance values as listed in Table 5-32. For case 3 and case 4, the combination of the codecs is the same, but the difference is that the higher processing performance is assigned to another codec in case 3, and to an H.264 or H.265 codec in case 4. This also applies to cases 7 and 8. The combination of a RealVideo codec and another codec cannot be used.

Table 5-32 Maximum Performance Values for Pixel Rate of VCP4 (When in Use with a VP9 Codec and the iVDP1C is Not in Use)

<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Case 1</td>
<td>250.7 (1920 × 1088 at 120 fps)</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>125.3 (1920 × 1088 at 60 fps)</td>
</tr>
<tr>
<td>Case 2</td>
<td>62.67 (1920 × 1088 at 30 fps)</td>
<td>62.67 (1920 × 1088 at 30 fps)</td>
<td>0</td>
<td>0</td>
<td>125.3 (1920 × 1088 at 60 fps)</td>
</tr>
<tr>
<td>Case 3</td>
<td>125.3 (1920 × 1088 at 60 fps)</td>
<td>0</td>
<td>62.67 (1920 × 1088 at 30 fps)</td>
<td>0</td>
<td>125.3 (1920 × 1088 at 60 fps)</td>
</tr>
<tr>
<td>Case 4</td>
<td>62.67 (1920 × 1088 at 30 fps)</td>
<td>0</td>
<td>125.3 (1920 × 1088 at 60 fps)</td>
<td>0</td>
<td>125.3 (1920 × 1088 at 60 fps)</td>
</tr>
<tr>
<td>Case 5</td>
<td>250.7 (1920 × 1088 at 120 fps)</td>
<td>0</td>
<td>0</td>
<td>125.3 (1920 × 1088 at 60 fps)</td>
<td>62.67 (1920 × 1088 at 30 fps)</td>
</tr>
<tr>
<td>Case 6</td>
<td>62.67 (1920 × 1088 at 30 fps)</td>
<td>62.67 (1920 × 1088 at 30 fps)</td>
<td>0</td>
<td>125.3 (1920 × 1088 at 60 fps)</td>
<td>62.67 (1920 × 1088 at 30 fps)</td>
</tr>
<tr>
<td>Case 7</td>
<td>125.3 (1920 × 1088 at 60 fps)</td>
<td>0</td>
<td>62.67 (1920 × 1088 at 30 fps)</td>
<td>125.3 (1920 × 1088 at 60 fps)</td>
<td>62.67 (1920 × 1088 at 30 fps)</td>
</tr>
<tr>
<td>Case 8</td>
<td>62.67 (1920 × 1088 at 30 fps)</td>
<td>0</td>
<td>125.3 (1920 × 1088 at 60 fps)</td>
<td>125.3 (1920 × 1088 at 60 fps)</td>
<td>62.67 (1920 × 1088 at 30 fps)</td>
</tr>
</tbody>
</table>

Note: * An image is compressed or decompressed in units of 16 × 16 blocks based on image compression standard. Accordingly, the image size should be rounded up to the nearest multiple of 16 when calculating the maximum performance value.
Figure 5-37  Maximum Performance Values for Pixel Rate of VCP4 (When in use with a VP9 codec and the iVDP1C is Not in Use)
**When iVDP1C is in use**

The maximum performance values for pixel rate of the VCP4 when the iVDP1C is in use are given in Table 5-33.

The maximum performance values depend on the combinations of codecs. There are three possible combinations in terms of the maximum performance values as listed in Table 5-33.

<table>
<thead>
<tr>
<th>Case</th>
<th>Maximum Performance of an H.264, H.265, or Another Codec (Mpixel/s)</th>
<th>Maximum Performance of a VP9 Codec (Mpixel/s)</th>
<th>Maximum Performance of a RealVideo Codec (Mpixel/s)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Case 1</td>
<td>62.67 (1920 × 1088 at 30 fps)*</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>Case 2</td>
<td>0</td>
<td>27.6 (1280 × 720 at 30 fps)</td>
<td>0</td>
</tr>
<tr>
<td>Case 3</td>
<td>0</td>
<td>0</td>
<td>27.6 (1280 × 720 at 30 fps)</td>
</tr>
</tbody>
</table>

Note: * An image is compressed or decompressed in units of 16 × 16 blocks based on image compression standard. Accordingly, the image size should be rounded up to the nearest multiple of 16 when calculating the maximum performance value.

**Figure 5-38 Maximum Performance Values for Pixel Rate of VCP4 (When iVDP1C is in Use)**
When iVDP1C is not in use

The maximum performance values for pixel rate of the VCP4 when the iVDP1C is not in use are given in Table 5-34. The maximum performance values depend on the combinations of codecs. There are three possible combinations in terms of the maximum performance values as listed in Table 5-34.

Table 5-34  Maximum Performance Values for Pixel Rate of VCP4 (When iVDP1C is Not in Use)

<table>
<thead>
<tr>
<th>Case</th>
<th>Maximum Performance of an H.264, H.265, or Another Codec (Mpixel/s)</th>
<th>Maximum Performance of a VP9 Codec (Mpixel/s)</th>
<th>Maximum Performance of a RealVideo Codec (Mpixel/s)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Case 1</td>
<td>125.3 (1920 × 1088 at 60 fps)*</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>Case 2</td>
<td>0</td>
<td>62.67 (1920 × 1088 at 30 fps)</td>
<td>0</td>
</tr>
<tr>
<td>Case 3</td>
<td>0</td>
<td>0</td>
<td>62.67 (1920 × 1088 at 30 fps)</td>
</tr>
</tbody>
</table>

Note:  * An image is compressed or decompressed in units of 16 × 16 blocks based on image compression standard. Accordingly, the image size should be rounded up to the nearest multiple of 16 when calculating the maximum performance value.

Figure 5-39  Maximum Performance Values for Pixel Rate of VCP4 (When iVDP1C is Not in Use)
(4) Maximum Performance for Pixel Rate of the iVDP1C

(a) Version 2.0 and 3.0 of the R-Car H3, version 1.1 of the R-Car M3-W, version 1.x of the R-Car M3-N

The maximum performance value for pixel rate of the iVDP1C is given in Table 5-35.

Table 5-35  Maximum Performance Value for Pixel Rate of iVDP1C

<table>
<thead>
<tr>
<th>Case</th>
<th>Maximum Performance Value of an H.264 or a JPEG Codec (Mpixel/s)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Case 1</td>
<td>147.5 (1280 × 960 at 120 fps)</td>
</tr>
</tbody>
</table>

![Figure 5-40  Maximum Performance Value for Pixel Rate of iVDP1C](image)
(b) Version 1.x of the R-Car E3

**When VCP4 is in use**

The maximum performance value for pixel rate of the iVDP1C when the VCP4 is in use is given in Table 5-36.

**Table 5-36 Maximum Performance Value for Pixel Rate of iVDP1C (When VCP4 is in Use)**

<table>
<thead>
<tr>
<th>Case</th>
<th>Maximum Performance Value of an H.264 or a JPEG Codec (Mpixel/s)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Case 1</td>
<td>36.9 ((1280 \times 960 \text{ at } 30 \text{ fps}))</td>
</tr>
</tbody>
</table>

![Figure 5-41 Maximum Performance Value for Pixel Rate of iVDP1C (When VCP4 is in Use)](image)

**When VCP4 is not in use**

The maximum performance value for pixel rate of the iVDP1C when the VCP4 is not in use is given in Table 5-37.

**Table 5-37 Maximum Performance Value for Pixel Rate of iVDP1C (When VCP4 is Not in Use)**

<table>
<thead>
<tr>
<th>Case</th>
<th>Maximum Performance Value of an H.264 or a JPEG Codec (Mpixel/s)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Case 1</td>
<td>73.7 ((1280 \times 960 \text{ at } 60 \text{ fps}))</td>
</tr>
</tbody>
</table>

![Figure 5-42 Maximum Performance Value for Pixel Rate of iVDP1C (When VCP4 is Not in Use)](image)
5.6.2  B) Concepts of Deriving Performance

(1) Procedure for Checking the Performance for Pixel Rate of the VCP4

The following describes the procedure for checking that the performance for the pixel rate which a use case requires of the VCP4 is not greater than its maximum performance.

- Procedure 1: Obtaining the required performance for pixel rate
  Performance required of an H.264 codec
  Performance required of an H.265 codec
  Performance required of a VP9 codec
  Performance required of a RealVideo codec
  Performance required of another codec

- Procedure 2: Comparing the required performance for pixel rate with the maximum performance of the VCP4

Detailed descriptions of procedures 1 and 2 are given in (a) to (f) on the following pages.
(a) Calculating the performance required of an H.264 codec

The performance for pixel rate required of the VCP4 in handling several H.264 sequences can be obtained from the expression below.

Performance required of H. 264 codec [pixel/s]

\[
\frac{1}{\sum_{i=0}^{N-1} \text{Roundup}(\text{Hsize}[i], 16) \times \text{Roundup}(\text{Vsize}[i], 16) \times \text{FrameRate}[i])}
\]

Hsize[i]: Number of pixels horizontally for use in the i-th H.264 sequence
Vsize[i]: Number of lines for use in the i-th H.264 sequence
FrameRate[i]: Frame rate for use in the i-th H.264 sequence (frame/s)*
Roundup(x, y): Round x up to the nearest integer multiple of y.
Sum from i = 0 to i = N – 1: Calculate the sum of the results for several H.264 sequences.

Note: * In interlaced mode, the frame rate (frame/s) is half the field rate (field/s). The frame rate for 60i, for example, is 30 frames/s.
(b) Calculating the performance required of an H.265 codec

The performance for pixel rate required of the VCP4 in handling several H.265 sequences can be obtained from the expression below.

Performance required of H. 265 codec [pixel/s]

\[
= \sum_{i=0}^{i<N} \text{Roundup}(\text{Hsize}[i], 64) \times \text{Roundup}(\text{Vsize}[i], 64) \times \text{FrameRate}[i])
\]

Hsize[i]: Number of pixels horizontally for use in the i-th H.265 sequence

Vsize[i]: Number of lines for use in the i-th H.265 sequence

FrameRate[i]: Frame rate for use in the i-th H.265 sequence (frame/s)

Roundup(x, y): Round x up to the nearest integer multiple of y.

Sum from i = 0 to i = N – 1: Calculate the sum of the results for several H.265 sequences.
(c) Calculating the performance required of a VP9 codec

The performance for pixel rate required of the VCP4 in handling several VP9 sequences can be obtained from the expression below.

Performance required of VP9 codec [pixel/s]

\[
\text{Performance required of VP9 codec [pixel/s] } = \sum_{i=0}^{i=N} (\text{Roundup}(\text{Hsize}[i], 64) \times \text{Roundup}(\text{Vsize}[i], 64) \times \text{FrameRate}[i])
\]

Hsize[i]: Number of pixels horizontally for use in the i-th VP9 sequence

Vsize[i]: Number of lines for use in the i-th VP9 sequence

FrameRate[i]: Frame rate for use in the i-th VP9 sequence (frame/s)

Roundup(x, y): Round x up to the nearest integer multiple of y.

Sum from i = 0 to i = N – 1: Calculate the sum of the results for several VP9 sequences.
(d) Calculating the performance required of a RealVideo codec

The performance for pixel rate required of the VCP4 in handling several RealVideo sequences can be obtained from the expression below.

Performance required of RealVideo codec [pixel/s]

\[
\text{Performance} = \left( \sum_{i=0}^{N-1} \text{Roundup}(\text{Hsize}[i], 16) \times \text{Roundup}(\text{Vsize}[i], 16) \times \text{FrameRate}[i] \right)
\]

Hsize[i]: Number of pixels horizontally for use in the i-th RealVideo sequence

Vsize[i]: Number of lines for use in the i-th RealVideo sequence

FrameRate[i]: Frame rate for use in the i-th RealVideo sequence (frame/s)

Roundup(x, y): Round x up to the nearest integer multiple of y.

Sum from i = 0 to i = N – 1: Calculate the sum of the results for several RealVideo sequences.
Calculating the performance required of another codec

The performance for pixel rate required of the VCP4 in handling several sequences with another codec can be obtained from the expression below.

\[
\text{Performance required of another codec [pixel/s]} = \sum_{i=0}^{i=N-1} (\text{Roundup}(\text{Hsize}[i], 16) \times \text{Roundup}(\text{Vsize}[i], 16) \times \text{FrameRate}[i])
\]

Hsize[i]: Number of pixels horizontally for use in the i-th sequence with another codec

Vsize[i]: Number of lines for use in the i-th sequence with another codec

FrameRate[i]: Frame rate for use in the i-th sequence with another codec (frame/s)*

Roundup(x, y): Round x up to the nearest integer multiple of y.

Sum from i = 0 to i = N – 1: Calculate the sum of the results for several sequences with another codec.

Note: * In interlaced mode, the frame rate (frame/s) is half the field rate (field/s). The frame rate for 60i, for example, is 30 frames/s.
Comparing the required performance with the maximum performance of the VCP4

Use the method described below to check whether the required performance for pixel rate calculated in procedure 1 satisfies the conditions for maximum performance of the VCP4.

Version 2.0 and 3.0 of the R-Car H3, version 1.1 of the R-Car M3-W, and version 1.x of the R-Car M3-N (other than when in use with a VP9 codec)

- When the iVDP1C is in use: Check whether the various maximum performance values for pixel rate of the VCP4 (cases 1 to 4) when the iVDP1C is in use satisfy all conditions listed below.
  
  Performance required of H.264 + performance required of H.265 (pixel/s) ≤ maximum performance of H.264 or H.265 codec of VCP4 (pixel/s)
  
  Performance required of RealVideo (pixel/s) ≤ maximum performance of RealVideo codec of VCP4 (pixel/s)
  
  Performance required of another codec (pixel/s) ≤ maximum performance of another codec of VCP4 (pixel/s)

- When the iVDP1C is not in use: Check whether the various maximum performance values for pixel rate of the VCP4 (cases 1 to 3) when the iVDP1C is not in use satisfy all conditions listed below.

  Performance required of H.264 (pixel/s) ≤ maximum performance of H.264 codec of VCP4 (pixel/s)
  
  Performance required of H.265 (pixel/s) ≤ maximum performance of H.265 codec of VCP4 (pixel/s)
  
  Performance required of RealVideo (pixel/s) ≤ maximum performance of RealVideo codec of VCP4 (pixel/s)
  
  Performance required of another codec (pixel/s) ≤ maximum performance of another codec of VCP4 (pixel/s)

Version 1.x of the R-Car M3-N (when in use with a VP9 codec)

- When the iVDP1C is in use: Check whether the various maximum performance values for pixel rate of the VCP4 (cases 1 to 3) when the iVDP1C is in use satisfy all conditions listed below.

  Performance required of H.264 (pixel/s) ≤ maximum performance of H.264 codec of VCP4 (pixel/s)
  
  Performance required of VP9 (pixel/s) ≤ maximum performance of VP9 codec of VCP4 (pixel/s)
  
  Performance required of another codec (pixel/s) ≤ maximum performance of another codec of VCP4 (pixel/s)

- When the iVDP1C is not in use: Check whether the various maximum performance values for pixel rate of the VCP4 (cases 1 to 8) when the iVDP1C is not in use satisfy all conditions listed below.

  Performance required of H.264 (pixel/s) ≤ maximum performance of H.264 codec of VCP4 (pixel/s)
  
  Performance required of H.265 (pixel/s) ≤ maximum performance of H.265 codec of VCP4 (pixel/s)
  
  Performance required of VP9 (pixel/s) ≤ maximum performance of VP9 codec of VCP4 (pixel/s)
  
  Performance required of RealVideo (pixel/s) ≤ maximum performance of RealVideo codec of VCP4 (pixel/s)
  
  Performance required of another codec (pixel/s) ≤ maximum performance of another codec of VCP4 (pixel/s)

Version 1.x of the R-Car E3

- Check whether the various maximum performance values for pixel rate of the VCP4 (cases 1 to 3) when the iVDP1C is in use or not in use satisfy all conditions listed below.

  Performance required of H.264 + performance required of H.265 + performance required of another codec (pixel/s) ≤ maximum performance of H.264, H.265, or another codec of VCP4 (pixel/s)
  
  Performance required of VP9 (pixel/s) ≤ maximum performance of VP9 codec of VCP4 (pixel/s)
  
  Performance required of RealVideo (pixel/s) ≤ maximum performance of RealVideo codec of VCP4 (pixel/s)
(2) Procedure for Checking the Performance for Pixel Rate of the iVDP1C

The following describes the procedure for checking that the performance for the pixel rate which a use case requires of the iVDP1C is not greater than its maximum performance.

- Procedure 1: Obtaining the required performance for pixel rate
  - Performance required of an H.264 codec
  - Performance required of a JPEG codec

- Procedure 2: Comparing the required performance for pixel rate with the maximum performance of the iVDP1C

Detailed descriptions of procedures 1 and 2 are given in (a) to (c) on the following pages.
(a) Calculating the performance required of an H.264 codec

The performance for pixel rate required of the iVDP1C in handling several H.264 sequences can be obtained from the expression below. Note that the performance does not depend on the color difference format (4:2:0 or 4:2:2) or the bit depth (8, 10, or 12 bits).

Performance required of H.264 codec [pixel/s]

\[
\frac{1}{\sum_{i=0}^{i=N-1} (\text{Roundup}(\text{Hsize}[i], 16) \times \text{Roundup}(\text{Vsize}[i], 16) \times \text{FrameRate}[i])}
\]

Hsize[i]: Number of pixels horizontally for use in the i-th H.264 sequence
Vsize[i]: Number of lines for use in the i-th H.264 sequence
FrameRate[i]: Frame rate for use in the i-th H.264 sequence (frame/s)*
Roundup(x, y): Round x up to the nearest integer multiple of y.
Sum from i = 0 to i = N – 1: Calculate the sum of the results for several H.264 sequences.

Note: * In interlaced mode, the frame rate (frame/s) is half the field rate (field/s). The frame rate for 60i, for example, is 30 frames/s.
(b) Calculating the performance required of a JPEG codec

The performance for pixel rate required of the iVDP1C in handling several JPEG sequences can be obtained from the expression below. Note that the performance does not depend on the color difference format (4:2:0 or 4:2:2) or the bit depth (8, 10, or 12 bits).

\[
\text{Performance required of JPEG codec [pixel/s]} = \sum_{i=0}^{i=N} (\text{Roundup}(\text{Hsize}[i], 16) \times \text{Roundup}(\text{Vsize}[i], 16) \times \text{FrameRate}[i])
\]

Hsize[i]: Number of pixels horizontally for use in the i-th JPEG sequence

Vsize[i]: Number of lines for use in the i-th JPEG sequence

FrameRate[i]: Frame rate for use in the i-th JPEG sequence (frame/s)

Roundup(x, y): Round x up to the nearest integer multiple of y.

Sum from i = 0 to i = N − 1: Calculate the sum of the results for several JPEG sequences.
(c) Comparing the required performance with the maximum performance

Use the method described below to check whether the required performance for pixel rate calculated in procedure 1 satisfies the conditions for maximum performance of the iVDP1C.

- Check whether the maximum performance of the iVDP1C satisfies the following condition.
  
  Performance required of H.264 + performance required of JPEG (pixel/s) 
  ≤ maximum performance of H.264 or JPEG codec of iVDP1C (pixel/s)
5.6.3 C) Concepts of Deriving Bandwidth

(a) Concepts of deriving bandwidth (1)

The VCP4 and iVDP1C write or read data such as image data or bit streams to or from external memory during encoding or decoding of moving pictures.

The bandwidths for the VCP4 and iVDP1C depend on the input bit stream and input images with regard to the factors described in the examples below.

Example 1: The amount of reference image data to be read depends on the bit stream.

Example 2: The rate of hits in access to the cache by the frame compression processor for codec (FCPC) depends on the bit stream.

Example 3: The rate of lossless data compression by the FCPC depends on the input images. For example, the application of lossless data compression by the FCPC becomes more difficult with more finely textured images.

The bandwidths for the VCP4 and iVDP1C also depend on the items listed below.

- Type of video coding scheme (e.g., H.264, H.265, or MPEG-2)
- Encoding or decoding?

![Diagram of Concepts of Deriving Bandwidths for the VCP4 and iVDP1C](image-url)
(b) Concepts of deriving bandwidth (2)

Use the attached video and display bandwidth calculation sheet to derive the bandwidth for the VCP4 or iVDP1C.

The required bandwidth for the VCP4 and iVDP1C is calculated based on the following information entered into the calculation sheet.

- Size of the input images
- Frame rate
- Image format
- Type of video coding scheme
- Encoding or decoding?

In addition, the three cases shown in Table 5-38 are selectable in decoding.

**Table 5-38 Cases for Calculation of VCP4 or iVDP1C Bandwidth**

<table>
<thead>
<tr>
<th>Case</th>
<th>Definition of Case</th>
<th>For Reference: Assumed Bit Stream</th>
</tr>
</thead>
<tbody>
<tr>
<td>Typical case</td>
<td>The amount of reference image data to be read is 50% of that in the worst case.</td>
<td>Stream that requires a normal bandwidth</td>
</tr>
<tr>
<td>Typical worst case</td>
<td>The amount of reference image data to be read is 75% of that in the worst case.</td>
<td>Stream that requires a high bandwidth</td>
</tr>
<tr>
<td>Worst case</td>
<td>The amount of reference image data to be read is the theoretical maximum.</td>
<td>Stream for testing, which is created to require a high bandwidth</td>
</tr>
</tbody>
</table>
(c) Note

- Use of the iVDP1C
  - The iVDP1C can only be used for low-delay decoding of video data from cameras.
5.7 CSI2 and VIN

5.7.1 A) Maximum Performance

(1) Version 1.1 of the R-Car M3-W

The VIN module in the R-Car M3-W provides two types of input interface: the MIPI CSI-2 interface (camera serial interface 2) ((a) in Figure 5-44) and a digital interface ((b) in Figure 5-44). Up to four virtual channels of data can be output from each of CSI40 and CSI20, and these are input to the VIN module ((d) in Figure 5-44) through the channel selector (c) in Figure 5-44).

Although the VIN module (d) has eight channels, data cannot be input beyond the maximum performance of the MIPI CSI-2 interface (a) or the digital interface (b). This is because the VIN module is connected with either the MIPI CSI-2 interface (a) or the digital interface (b). On these bases, this section explains the maximum performances of (a), (b), (c) and (d). The connection relationship among (a), (b), (c) and (d) is shown in Figure 5-44.

Figure 5-44 CSI2-VIN Module Configuration (Version 1.1 of the R-Car M3-W)
(a) Data rate limits for MIPI CSI-2 interface

The MIPI CSI-2 interface has multiple channels. Table 5-39 shows the channel names and number of lanes of the MIPI CSI-2 interface. The maximum rate of data transfer per lane is 1.5 Gbits/s, and video data cannot be input at a higher rate than the maximum rate for each MIPI CSI-2 channel.

Table 5-39 Maximum Performance Specifications of CSI2 (Version 1.1 of the R-Car M3-W)

<table>
<thead>
<tr>
<th>MIPI CSI-2 Interface Channel Name</th>
<th>Number of Lanes</th>
<th>Maximum Specifications of Video Input Data Rate (Mbyte/s)</th>
<th>Maximum-Size Video Format and Data Type</th>
</tr>
</thead>
<tbody>
<tr>
<td>CSI40</td>
<td>4</td>
<td>668.25 (= 148.5 \times 1.5 \times 3)</td>
<td>2880 \times 1080p60 RGB-888</td>
</tr>
<tr>
<td>CSI20</td>
<td>2</td>
<td>334.125 (= 74.25 \times 1.5 \times 3)</td>
<td>2880 \times 1080p30 RGB-888</td>
</tr>
</tbody>
</table>

(b) Video clock frequency limits for digital interface

The digital interface has two channels and the maximum video clock frequency is 100 MHz.

(c) Recommended setting for channel selector

Possible combinations of VIN channel and input interface through the channel selector are limited. For details, refer to the tables of “Video Channels and Supported Interfaces” in section 26.3, Operation, in the hardware manual. The combinations of the VIN channels and the input interfaces must satisfy the following conditions.

- Send image data with the highest data rate through VC0 of the CSI40 and CSI20 interfaces.
- The output from CSI40 must be connected to VIN0 to VIN3. Note that VC0 of CSI40 must be connected to VIN0.
- The output from CSI20 must be connected to VIN4 to VIN7. Note that VC0 of CSI20 must be connected to VIN4.

The above connections are based on the assumption that VIN0 and VIN4 are used to capture high transfer-rate images. For details, refer to section 5.7.2 (4), Allocation of VIN Channel for Writing Image at High Transfer Rate.

(d) Data rate limits for VIN

The maximum video clock frequency per VIN channel is 222.75 (= 148.5 \times 1.5) MHz. The data rate limits are as follows.

Table 5-40 Maximum Performance Specifications of VIN (Version 1.1 of the R-Car M3-W)

<table>
<thead>
<tr>
<th>Condition</th>
<th>Maximum Specifications of Video Input and Data Rate (Mbyte/s)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>If any of the VIN channels connected with CSI40 has an input data rate higher than 148.5 \times 3 Mbytes/s, use only VIN0: VIN1 to VIN3 must not be used.</td>
</tr>
<tr>
<td>2</td>
<td>The digital interface or the CSI20 channel with the highest input data rate must be connected to VIN4.</td>
</tr>
<tr>
<td>3</td>
<td>The output data rate (video clock frequency \times scaling factor \times output color depth) per VIN channel must not exceed 891 (= 148.5 \times 1.5 \times 4) Mbytes/s.</td>
</tr>
<tr>
<td>4</td>
<td>The sum of the output data rates for the 8 VIN channels must not exceed 1336.5 (= 148.5 \times 1.5 \times 4 + 74.25 \times 1.5 \times 4) Mbytes/s.</td>
</tr>
</tbody>
</table>
(2) Version 2.0 and 3.0 of the R-Car H3

The VIN module in the R-Car H3 provides two types of input interface: the MIPI CSI-2 interface (camera serial interface 2) ((a) in Figure 5-45) and a digital interface (b) in Figure 5-45). Up to four virtual channels of data can be output from each of CSI40, CSI41, and CSI20, and these are input to the VIN module ((d) in Figure 5-45) through the channel selector ((c) in Figure 5-45).

Although the VIN module (d) has eight channels, data cannot be input beyond the maximum performance of the MIPI CSI-2 interface (a) or the digital interface (b). This is because the VIN module is connected with either the MIPI CSI-2 interface (a) or the digital interface (b). On these bases, this section explains the maximum performances of (a), (b), (c) and (d). The connection relationship among (a), (b), (c) and (d) is shown in Figure 5-45.

![CSI2-VIN Module Configuration (Version 2.0 and 3.0 of the R-Car H3)](image-url)
(a) Data rate limits for MIPI CSI-2 interface

The MIPI CSI-2 interface has multiple channels. Table 5-41 shows the channel names and number of lanes of the MIPI CSI-2 interface. The maximum rate of data transfer per lane is 1.5 Gbits/s, and video data cannot be input at a higher rate than the maximum rate for each MIPI CSI-2 channel.

<table>
<thead>
<tr>
<th>MIPI CSI-2 Interface Channel Name</th>
<th>Number of Lanes</th>
<th>Maximum Specifications of Video Input</th>
</tr>
</thead>
<tbody>
<tr>
<td>CSI40</td>
<td>4</td>
<td>Data Rate (Mbyte/s) 668.25 (= 148.5 × 1.5 × 3)</td>
</tr>
<tr>
<td>CSI41</td>
<td>4</td>
<td>Data Rate (Mbyte/s) 668.25 (= 148.5 × 1.5 × 3)</td>
</tr>
<tr>
<td>CSI20</td>
<td>2</td>
<td>Data Rate (Mbyte/s) 334.125 (= 74.25 × 1.5 × 3)</td>
</tr>
</tbody>
</table>

(b) Video clock frequency limits for digital interface

The digital interface has two channels and the maximum video clock frequency is 100 MHz.

(c) Recommended setting for channel selector

Possible combinations of VIN channel and input interface through the channel selector are limited. For details, refer to the tables of "Video Channels and Supported Interfaces" in section 26.3, Operation, in the hardware manual. The combinations of the VIN channels and the input interfaces must satisfy the following conditions.

Send image data with the highest data rate through VC0 of the CSI40, CSI41, and CSI20 interfaces.

- The output from CSI40 must be connected to VIN0 to VIN3. Note that VC0 of CSI40 must be connected to VIN0.
- The output from CSI41 must be connected to VIN4 to VIN7. Note that VC0 of CSI41 must be connected to VIN4.
- The output from VC0 of CSI20 must be connected must be connected to VIN0 or VIN4.

The above connections are based on the assumption that VIN0 and VIN4 are used to capture high transfer-rate images. For details, refer to section 5.7.2 (4), Allocation of VIN Channel for Writing Image at High Transfer Rate.

(d) Data rate limits for VIN

The maximum video clock frequency per one VIN channel is 222.75 MHz. The data rate limits are as follows.

<table>
<thead>
<tr>
<th>Condition</th>
<th>Maximum Specifications of Video Input and Data Rate (Mbyte/s)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>If any of the VIN channels connected with CSI40 has an input data rate higher than 148.5 × 3 (Mbytes/s), use only VIN0: VIN1 to VIN3 must not be used.</td>
</tr>
<tr>
<td>2</td>
<td>If any of the VIN channels connected with CSI41 has an input data rate higher than 148.5 × 3 (Mbytes/s), use only VIN4: VIN5 to VIN7 must not be used.</td>
</tr>
<tr>
<td>3</td>
<td>When the digital interface is to be used, connect the CSI20 interface to VIN0 to VIN3. When it is not to be used, the CSI41 or CSI20 channel with the highest input data rate must be connected to VIN4.</td>
</tr>
<tr>
<td>4</td>
<td>The output data rate (= video clock frequency × scaling factor × output color depth) per one VIN channel must not exceed 891 (= 148.5 × 1.5 × 4) Mbytes/s.</td>
</tr>
<tr>
<td>5</td>
<td>The sum of the output data rates for the 8 VIN channels must not exceed 2227.5 (= 891 × 2 + 445.5) Mbytes/s.</td>
</tr>
</tbody>
</table>
(3) **Version 1.x of the R-Car M3-N**

The VIN module in the R-Car M3-N provides two types of input interface: the MIPI CSI-2 interface (camera serial interface 2) ((a) in Figure 5-46) and a digital interface ((b) in Figure 5-46). Up to four virtual channels of data can be output from each of CSI40 and CSI20, and these are input to the VIN module ((d) in Figure 5-46) through the channel selector ((c) in Figure 5-46).

Although the VIN module (d) has eight channels, data cannot be input beyond the maximum performance of the MIPI CSI-2 interface (a) or the digital interface (b). This is because the VIN module is connected with either the MIPI CSI-2 interface (a) or the digital interface (b). On these bases, this section explains the maximum performances of (a), (b), (c) and (d). The connection relationship among (a), (b), (c) and (d) is shown in Figure 5-46.

![CSI2-VIN Module Configuration (Version 1.x of the R-Car M3-N)](image-url)
The MIPI CSI-2 interface has multiple channels. Table 5-43 shows the channel names and number of lanes of the MIPI CSI-2 interface. The maximum rate of data transfer per lane is 1.5 Gbits/s, and video data cannot be input at a higher rate than the maximum rate for each MIPI CSI-2 channel.

### Table 5-43 Maximum Performance Specifications of CSI2 (Version 1.x of the R-Car M3-N)

<table>
<thead>
<tr>
<th>MIPI CSI-2 Interface Channel Name</th>
<th>Number of Lanes</th>
<th>Data Rate (Mbyte/s)</th>
<th>Maximum-Sized Video Format and Data Type</th>
</tr>
</thead>
<tbody>
<tr>
<td>CSI40</td>
<td>4</td>
<td>445.5 (= 148.5 × 3)</td>
<td>1920 × 1080p60 RGB-888</td>
</tr>
<tr>
<td>CSI20</td>
<td>2</td>
<td>222.75 (= 74.25 × 3)</td>
<td>1920 × 1080p30 RGB-888</td>
</tr>
</tbody>
</table>

The digital interface has two channels and the maximum video clock frequency is 100 MHz.

Possible combinations of VIN channel and input interface through the channel selector are limited. For details, refer to the tables of "Video Channels and Supported Interfaces" in section 26.3, Operation, in the hardware manual. The combinations of the VIN channels and the input interfaces must satisfy the following conditions:

Send image data with the highest data rate through VC0 of the CSI40 and CSI20 interfaces.

The output from CSI40 must be connected to VIN0 to VIN3. Note that VC0 of CSI40 must be connected to VIN0.

The output from CSI20 must be connected to VIN4 to VIN7. Note that VC0 of CSI20 must be connected to VIN4.

The above connections are based on the assumption that VIN0 and VIN4 are used to capture high transfer-rate images. For details, refer to section 5.7.2 (4), Allocation of VIN Channel for Writing Image at High Transfer Rate.

The maximum video clock frequency per one VIN channel is 148.5 MHz. The data rate limits are as follows.

### Table 5-44 Maximum Performance Specifications of VIN (Version 1.x of the R-Car M3-N)

<table>
<thead>
<tr>
<th>Condition</th>
<th>Maximum Specifications of Video Input and Data Rate (Mbyte/s)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>The digital interface or the CSI20 channel with the highest input data rate must be connected to VIN4.</td>
</tr>
<tr>
<td>2</td>
<td>The output data rate (= video clock frequency × scaling factor × output color depth) per one VIN channel must not exceed 594 (= 148.5 × 4) Mbytes/s.</td>
</tr>
<tr>
<td>3</td>
<td>The sum of the output data rates for the 8 VIN channels must not exceed 891 (= 148.5 × 4 + 74.25 × 4) Mbytes/s.</td>
</tr>
</tbody>
</table>
(4) Version 1.x of the R-Car E3

The VIN module in the R-Car E3 provides two types of input interface: the MIPI CSI-2 interface (camera serial interface 2) ((a) in Figure 5-47) and a digital interface ((b) in Figure 5-47). The CSI2 module incorporated in the R-Car E3 is a single CSI40 (CSI4LNK0) which is capable of handling four lanes. Note, however, that only two of these lanes are usable in the R-Car E3. Accordingly, up to four virtual channels of data can be output from CSI40, and these are input to the VIN module ((d) in Figure 5-47) through the channel selector ((c) in Figure 5-47).

Although the VIN module (d) has two channels, data cannot be input beyond the maximum performance of the MIPI CSI-2 interface (a) or the digital interface (b). This is because the VIN module is connected with either the MIPI CSI-2 interface (a) or the digital interface (b). On these bases, this section explains the maximum performances of (a), (b), (c) and (d). The connection relationship among (a), (b), (c) and (d) is shown in Figure 5-47.

Figure 5-47  CSI2-VIN Module Configuration (Version 1.x of the R-Car E3)
(a) Data rate limits for MIPI CSI-2 interface

The MIPI CSI-2 interface has multiple channels. Table 5-45 shows the channel names and number of lanes of the MIPI CSI-2 interface. The maximum rate of data transfer per lane is 1.5 Gbits/s, and video data cannot be input at a higher rate than the maximum rate for each MIPI CSI-2 channel.

**Table 5-45 Maximum Performance Specifications of CSI2 (Version 1.x of the R-Car E3)**

<table>
<thead>
<tr>
<th>MIPI CSI-2 Interface Channel Name</th>
<th>Number of Lanes</th>
<th>Maximum Specifications of Video Input</th>
<th>Maximum-SIZE Video Format and Data Type</th>
</tr>
</thead>
<tbody>
<tr>
<td>CSI40</td>
<td>2</td>
<td>222.75 ( = 74.25 \times 3 )</td>
<td>1920 \times 1080p30 RGB-888</td>
</tr>
</tbody>
</table>

(b) Video clock frequency limits for digital interface

The digital interface has two channels and the maximum video clock frequency is 100 MHz.

(c) Recommended setting for channel selector

Possible combinations of VIN channel and input interface through the channel selector are limited. For details, refer to the tables of "Video Channels and Supported Interfaces" in section 26.3, Operation, in the hardware manual. The combinations of the VIN channels and the input interfaces must satisfy the following conditions.

- Send image data with the highest data rate through VC0 of the CSI40 interface.
- The output from CSI40 must be connected to VIN4 and VIN5. Note that VC0 of CSI40 must be connected to VIN4.

The above connections are based on the assumption that VIN4 is used to capture high transfer-rate images. For details, refer to section 5.7.2 (4), Allocation of VIN Channel for Writing Image at High Transfer Rate.

(d) Data rate limits for VIN

The maximum video clock frequency per one VIN channel is 74.25 MHz. The data rate limits are as follows.

**Table 5-46 Maximum Performance Specifications of VIN (Version 1.x of the R-Car E3)**

<table>
<thead>
<tr>
<th>Condition</th>
<th>Maximum Specifications of Video Input and Data Rate (Mbyte/s)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>The digital interface or the CSI40 channel with the highest input data rate must be connected to VIN4.</td>
</tr>
<tr>
<td>2</td>
<td>The output data rate (= video clock frequency \times scaling factor \times output color depth) per VIN channel must not exceed 297 (=74.25 \times 4) Mbytes/s.</td>
</tr>
<tr>
<td>3</td>
<td>The sum of the output data rates for the 2 VIN channels must not exceed 445.5 (= 74.25 \times 4 + 74.25 \times 2) Mbytes/s.</td>
</tr>
</tbody>
</table>
(5) **Version 1.x of the R-Car D3**

The VIN module in the R-Car D3 can provide a digital interface ((b) in Figure 5-48) as an input interface. Data are input to the VIN module ((d) in Figure 5-48) through the digital interface ((b) in Figure 5-48). A MIPI CSI2 and channel selector are not provided.

Although the VIN module (d) has one channel, data cannot be input beyond the maximum performance of the digital interface (b). This is because the VIN module is connected with the digital interface (b). On these bases, this section explains the maximum performances of (b) and (d). The connection relationship between (b) and (d) is shown in Figure 5-48.

![Figure 5-48 VIN Module Configuration (Version 1.x of the R-Car D3)](image-url)
(a) Data rate limits for MIPI CSI-2 interface
Not applicable to the R-Car D3.

(b) Video clock frequency limits for digital interface
The digital interface has one channel and the maximum video clock frequency is 100374.25 MHz.

(c) Recommended setting for channel selector
Not applicable to the R-Car D3.

(d) Data rate limits for VIN
The maximum video clock frequency per one VIN channel is 74.25 MHz. The data rate limits are as follows.

<table>
<thead>
<tr>
<th>Condition</th>
<th>Maximum Performance Specifications of VIN (Version 1.x of the R-Car D3)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>The output data rate (=\text{video clock frequency} \times \text{scaling factor} \times \text{output color depth}) per one VIN channel must not exceed 148.5 (=74.25 \times 2) Mbytes/s.</td>
</tr>
</tbody>
</table>
5.7.2 B) Concepts of Deriving Performance

(1) Concepts of Deriving Required Performance

The video clock frequency can be obtained from the following expression by using the total number of pixels horizontally, total number of lines, and frame rate.

\[
\text{Video clock frequency} = \text{total number of pixels horizontally} \times \text{total number of lines} \times \text{frame rate}
\]

The "total number of pixels horizontally" and "total number of lines" represent the sizes including the blanking periods, which are not included in the number of valid pixels horizontally and number of valid lines. The following shows examples in standard video formats such as those prescribed in SMPTE and VESA.

Table 5-48 Examples in Standard Video Formats

<table>
<thead>
<tr>
<th>Video Format</th>
<th>Number of Valid Pixels Horizontally</th>
<th>Number of Valid Lines</th>
<th>Total Number of Pixels Horizontally</th>
<th>Total Number of Lines</th>
<th>Frame Rate (Hz)</th>
<th>Video Clock Frequency (MHz)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1280 × 720p60</td>
<td>1280</td>
<td>720</td>
<td>1650</td>
<td>750</td>
<td>60</td>
<td>74.25</td>
</tr>
<tr>
<td>1920 × 1080i60</td>
<td>1920</td>
<td>1080</td>
<td>2200</td>
<td>1125</td>
<td>30</td>
<td>74.25</td>
</tr>
<tr>
<td>1920 × 1080p60</td>
<td>1920</td>
<td>1080</td>
<td>2200</td>
<td>1125</td>
<td>60</td>
<td>148.5</td>
</tr>
</tbody>
</table>

In development of the target board, the actual video clock frequency is determined by the specifications of the external device on the other end, such as a camera, from which video is input. Consult with those who manage the related requirements to determine the video clock frequency.
(2) Deriving the Transfer Rate per Lane in the CSI2

For the CSI2 interfaces, the maximum transfer rate per lane is 1.5 Gbits/s. Video data cannot be input at a higher rate than this. For the maximum transfer rate for the CSI2, refer to section 5.7.1, A) Maximum Performance.

The data transfer rate for each CSI2 lane can be obtained from the following expression by using the video clock frequency, number of bits per pixel, and number of lanes.

\[
\text{Data transfer rate per lane [Gbit/s]} = \frac{\text{video clock frequency [MHz]} \div 1000 \times \text{number of bits per pixel}}{\text{number of lanes}}
\]

The number of bits per pixel depends on the data type.

- RGB-888: 24 bits
- 10-bit YCbCr-422: 20 bits
- 8-bit YCbCr-422: 16 bits
- RAW8: 8 bits
(3) Roughly Estimating whether Data Can be Input to the CSI2

Table 5-49 shows examples indicating whether data can be input under various conditions in terms of the video format, data type, and number of lanes.

Table 5-49  Examples Indicating whether Data Can be Input to the CSI2

<table>
<thead>
<tr>
<th>Video Format</th>
<th>Data Type</th>
<th>CSI2 Interface</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>4 Lanes</td>
</tr>
<tr>
<td>1920 × 1080p60</td>
<td>RGB-888</td>
<td>OK</td>
</tr>
<tr>
<td></td>
<td>10-bit YCbCr-422</td>
<td>OK</td>
</tr>
<tr>
<td></td>
<td>8-bit YCbCr-422</td>
<td>OK</td>
</tr>
<tr>
<td>1280 × 720p60</td>
<td>RGB-888</td>
<td>OK</td>
</tr>
<tr>
<td></td>
<td>10-bit YCbCr-422</td>
<td>OK</td>
</tr>
<tr>
<td></td>
<td>8-bit YCbCr-422</td>
<td>OK</td>
</tr>
<tr>
<td>1920 × 1080i60</td>
<td>RGB-888</td>
<td>OK</td>
</tr>
<tr>
<td></td>
<td>10-bit YCbCr-422</td>
<td>OK</td>
</tr>
<tr>
<td></td>
<td>8-bit YCbCr-422</td>
<td>OK</td>
</tr>
</tbody>
</table>

OK: Can be input
NG: Cannot be input.
(4) Allocation of VIN Channel for Writing Image at High Transfer Rate

To write images to external memory at a high transfer rate, such as RGB Full HD at 60 fps, we recommend the allocation of video channel 0 (VIN0) or channel 4 (VIN4) in the VIN. VIN0 and VIN4 have larger data buffers than the other channels, which reduce overflows at a high transfer rate.

Additionally, high transfer-rate images are assumed to be input to VC0 of the CSI4x and CSI20 interfaces, so we recommend that VC0 of the CSI4x and CSI20 be connected to VIN0 and VIN4.

Video channels 4 and 5 (VIN4 and VIN5) of the VIN are allocated for input from the digital interface. We recommend that connections be made in the modes shown in the following table by using the mode setting register in the channel selector, and taking into account the imbalances between VIN0 to VIN3 and VIN4 to VIN7 in terms of the amounts of data to be transferred. For details on the mode setting register, refer to Table 26.14, CSI2 Channel Select Setting in section 26.2.8, Video n CSI2 Interface Mode Register (VnCSI_IFMD) in the hardware manual.

### Table 5-50  List of Possible Combinations of CSI2 and VIN Channels [Version 1.1 of the R-Car M3-W]

<table>
<thead>
<tr>
<th>VIN Ch</th>
<th>Mode Setting Register</th>
<th>Channels and Virtual Channels of the CSI2 to be Input to the VIN in each Mode</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>V0CSI_IFMD</td>
<td>CSI40/VC0</td>
</tr>
<tr>
<td>1</td>
<td>---</td>
<td>CSI20/VC0</td>
</tr>
<tr>
<td>2</td>
<td>---</td>
<td>CSI40/VC1</td>
</tr>
<tr>
<td>3</td>
<td>---</td>
<td>CSI40/VC3</td>
</tr>
<tr>
<td>4</td>
<td>V4CSI_IFMD</td>
<td>---</td>
</tr>
<tr>
<td>5</td>
<td>---</td>
<td>---</td>
</tr>
<tr>
<td>6</td>
<td>---</td>
<td>CSI40/VC0</td>
</tr>
<tr>
<td>7</td>
<td>---</td>
<td>CSI20/VC1</td>
</tr>
</tbody>
</table>

Note: VC0 to VC3 in the table indicate the virtual channel ports of the CSI2.

### Table 5-51  List of Possible Combinations of CSI2 and VIN Channels [Version 2.0 and 3.0 of the R-Car H3]

<table>
<thead>
<tr>
<th>VIN Ch</th>
<th>Mode Setting Register</th>
<th>Channels and Virtual Channels of the CSI2 to be Input to the VIN in each Mode</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>V0CSI_IFMD</td>
<td>CSI40/VC0</td>
</tr>
<tr>
<td>1</td>
<td>---</td>
<td>CSI20/VC0</td>
</tr>
<tr>
<td>2</td>
<td>---</td>
<td>CSI20/VC1</td>
</tr>
<tr>
<td>3</td>
<td>---</td>
<td>CSI40/VC1</td>
</tr>
<tr>
<td>4</td>
<td>V4CSI_IFMD</td>
<td>CSI41/VC0</td>
</tr>
<tr>
<td>5</td>
<td>---</td>
<td>CSI20/VC0</td>
</tr>
<tr>
<td>6</td>
<td>---</td>
<td>CSI20/VC1</td>
</tr>
<tr>
<td>7</td>
<td>---</td>
<td>CSI20/VC1</td>
</tr>
</tbody>
</table>

Note: VC0 to VC3 in the table indicate the virtual channel ports of the CSI2.

### Table 5-52  List of Possible Combinations of CSI2 and VIN Channels [Version 1.x of the R-Car M3-N]

<table>
<thead>
<tr>
<th>VIN Ch</th>
<th>Mode Setting Register</th>
<th>Channels and Virtual Channels of the CSI2 to be Input to the VIN in each Mode</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>V0CSI_IFMD</td>
<td>CSI40/VC0</td>
</tr>
<tr>
<td>1</td>
<td>---</td>
<td>CSI20/VC0</td>
</tr>
<tr>
<td>2</td>
<td>---</td>
<td>CSI20/VC1</td>
</tr>
<tr>
<td>3</td>
<td>---</td>
<td>CSI40/VC1</td>
</tr>
<tr>
<td>4</td>
<td>V4CSI_IFMD</td>
<td>---</td>
</tr>
<tr>
<td>5</td>
<td>---</td>
<td>---</td>
</tr>
<tr>
<td>6</td>
<td>---</td>
<td>CSI40/VC0</td>
</tr>
<tr>
<td>7</td>
<td>---</td>
<td>CSI20/VC1</td>
</tr>
</tbody>
</table>

Note: VC0 to VC3 in the table indicate the virtual channel ports of the CSI2.
Table 5-53  List of Possible Combinations of CSI2 and VIN Channels [Version 1.x of the R-Car E3]

<table>
<thead>
<tr>
<th>VIN Ch</th>
<th>Mode Setting Register</th>
<th>Channels and Virtual Channels of the CSI2 to be Input to the VIN in each Mode</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>Mode 0</td>
</tr>
<tr>
<td>4</td>
<td>V4CSI_IFMD</td>
<td>CSI40/VC0</td>
</tr>
<tr>
<td>5</td>
<td></td>
<td>—</td>
</tr>
</tbody>
</table>

Note: VC0 and VC1 in the table indicate the virtual channel ports of the CSI2.

(5) Usage Notes for VIN Scaling

When the VIN scales input images up and writes the scaled-up images to external memory, the scaling factors must be no more than 2 horizontally and 3 vertically. For details, refer to section 26.1.1 (8), Vertical and Horizontal Scaling in the hardware manual.

In addition, when scaling up, the value of (video clock frequency × factor for scaling up) must not be greater than the upper limit of the video clock frequency (= 148.5 × 1.5 [MHz]).

For the VIN, the calculation of the bandwidth depends on whether the vertical scaling mode is no scaling or scaling-down, or is scaling-up. For details, refer to section 5.7.3, C) Concepts of Deriving Bandwidth.
5.7.3 C) Concepts of Deriving Bandwidth

The VIN writes image data input from an external pin or the CSI2 to external memory. To prevent overflows, the maximum bandwidth (referred to as the peak bandwidth) instead of the average bandwidth within the period until a frame of data has been input is required.

The VIN writes bundles of images input through up to four channels to external memory. Specifically, images through VIN video channels 0 to 3 are bundled and those through channels 4 to 7 are bundled for output to external memory. Accordingly, the bandwidths should be separately derived for these two bundles, the bundle of video channels 0 to 3 of the VIN and the bundle of video channels 4 to 7 of the VIN. The peak bandwidth per bundle of images input through four VIN channels is the sum of the peak bandwidths for the input images in the bundle.

(1) Version 1.1 of the R-Car M3-W

Peak bandwidth per bundle of four VIN channels is calculated as follows.

(a) For scaling up vertically in the UDS

\[
\text{Peak bandwidth per bundle of four VIN channels (Mbyte/s) } = (\sum_{n} 400[\text{Mpix/s}] \times \text{BPPout}[n])
\]

\[
\text{BPPout}[n]: \text{ Number of bytes per pixel in input image } n \text{ being written to external memory}
\]

\[
n: \text{ Video channels 0 to 3 or video channels 4 to 7}
\]

(b) For no scaling vertically or scaling down vertically in the UDS

\[
\text{Peak bandwidth per bundle of four VIN channels (Mbyte/s)} = (\sum_{n} \text{PXL CLOCK}[n] \times \text{BPPout}[n] \times h_{scale}[n] \times \text{max}(v_{scale}[n], 1))
\]

\[
\text{PXL CLOCK}[n]: \text{ Video clock frequency for input image } n \text{ (MHz)}
\]

\[
\text{BPPout}[n]: \text{ Number of bytes per pixel in input image } n \text{ being written to external memory}
\]

\[
h_{scale}[n]: \text{ Horizontal scaling factor for input image } n
\]

\[
v_{scale}[n]: \text{ Vertical scaling factor for input image } n
\]

The term \(\text{max}(v_{scale}[n], 1)\) is greater than 1 in case of vertical scaling up and it is 1 for no vertical scaling or scaling down, with reference to the scaling factor of input image \(n\).

\[
n: \text{ Video channels 0 to 3 or video channels 4 to 7}
\]

Horizontal and vertical scaling factors can be set in the scaling factor registers (VnUDS_SCALE) of the UDS. For details, refer to the hardware manual.

For convenience of explanation, the following expressions are used for calculation in section 5.7.4, D) Example of Bandwidth Calculation.

\[
h_{scale} = \text{HORIout}/\text{HORIin}
\]

\[
v_{scale} = \text{VERTout}/\text{VERTin}
\]

\[
\text{HORIin}: \text{ Number of pixels horizontally in the input plane (CSI2 or digital interface)}
\]

\[
\text{VERTin}: \text{ Number of lines in the input plane (CSI2 or digital interface)}
\]

\[
\text{HORIout}: \text{ Number of pixels horizontally in the output plane}
\]

\[
\text{VERTout}: \text{ Number of lines in the output plane}
\]
The peak bandwidth of the VIN is calculated separately for each of the operation categories as shown below.

### Table 5-54 Operation Categories for Peak Bandwidth Calculation [Version 2.0 of the R-Car H3]

<table>
<thead>
<tr>
<th>Operation Categories for Peak Bandwidth</th>
<th>Condition</th>
</tr>
</thead>
<tbody>
<tr>
<td>Processing at 400 Mpix/s</td>
<td>When either of the conditions below is satisfied. Scaling up vertically in the UDS and output in the YCbCr format. Scaling up vertically in the UDS and conditions shown in Table 5-55, Conditions for Width are satisfied.</td>
</tr>
<tr>
<td>Processing at video clock rate</td>
<td>Other than the above</td>
</tr>
</tbody>
</table>

### Table 5-55 Conditions for Width

<table>
<thead>
<tr>
<th>VIN Channel</th>
<th>ARGB-8888</th>
<th>RGB-565</th>
<th>ARGB-1555</th>
<th>RGB-888</th>
</tr>
</thead>
<tbody>
<tr>
<td>0, 4</td>
<td>1022 pixels or less</td>
<td>2046 pixels or less</td>
<td>2046 pixels or less</td>
<td>1022 pixels or less</td>
</tr>
<tr>
<td>1, 2, 3, 5, 6, 7</td>
<td>510 pixels or less</td>
<td>1022 pixels or less</td>
<td>1022 pixels or less</td>
<td>510 pixels or less</td>
</tr>
</tbody>
</table>

Peak bandwidth per bundle of images for four VIN channels is calculated as follows.

(a) In processing at 400 Mpix/s

Peak bandwidth per bundle of four VIN channels (Mbyte/s) = \( \frac{\sum_{n} 400 \text{Mpix/s} \times BPP_{out}[n]}{n} \)

BPPout[n]: Number of bytes per pixel in input image n being written to external memory

n: Video channels 0 to 3 or video channels 4 to 7

(b) In processing at video clock rate

Peak bandwidth per bundle of four VIN channels (Mbyte/s)

\[
= \left( \sum_{n} \text{PXL}_{\text{CLOCK}}[n] \times BPP_{out}[n] \times h_{\text{scale}}[n] \times \text{max}(v_{\text{scale}}[n], 1) \right)
\]

PXL\(_{\text{CLOCK}}\)[n]: Video clock frequency for input image n (MHz)

BPPout[n]: Number of bytes per pixel in input image n being written to external memory

h_{\text{scale}}[n]: Horizontal scaling factor for input image n

v_{\text{scale}}[n]: Vertical scaling factor for input image n

The term max(v_{\text{scale}}[n], 1) is greater than 1 in case of vertical scaling up and it is 1 for no vertical scaling or scaling down, with reference to the scaling factor of input image n.

n: Video channels 0 to 3 or video channels 4 to 7

Horizontal and vertical scaling factors can be set in the scaling factor registers (VnUDS\_SCALE) of the UDS. For details, refer to the hardware manual.

For convenience of explanation, the following expressions are used for calculation in section 5.7.4, D) Example of Bandwidth Calculation.

\[ h_{\text{scale}} = \frac{\text{HORI}_{\text{out}}}{\text{HORI}_{\text{in}}} \]

\[ v_{\text{scale}} = \frac{\text{VERT}_{\text{out}}}{\text{VERT}_{\text{in}}} \]

\[ \text{HORI}_{\text{in}}: \text{Number of pixels horizontally in the input plane (CSI2 or digital interface)} \]

\[ \text{VERT}_{\text{in}}: \text{Number of lines in the input plane (CSI2 or digital interface)} \]

\[ \text{HORI}_{\text{out}}: \text{Number of horizontal pixels in the output plane} \]

\[ \text{VERT}_{\text{out}}: \text{Number of lines in the output plane} \]
(3) **Version 3.0 of the R-Car H3, version 1.x of the R-Car M3-N, version 1.x of the R-Car E3, and version 1.x of the R-Car D3**

Peak bandwidth per bundle of four VIN channels is calculated as follows.

\[
\text{Peak bandwidth per bundle of four VIN channels (Mbyte/s)} = \left( \sum_\text{n} \text{PXL} \_\text{CLOCK}[n] \times \text{BPPout}[n] \times \text{h} \_\text{scale}[n] \times \text{max} (\text{v} \_\text{scale}[n], 1) \right)
\]

- PXL\_CLOCK[n]: Video clock frequency for input image n (MHz)
- BPPOut[n]: Number of bytes per pixel in input image n being written to external memory
- h\_scale[n]: Horizontal scaling factor for input image n
- v\_scale[n]: Vertical scaling factor for input image n
  - The term max(v\_scale[n],1) is greater than 1 in case of vertical scaling up and it is 1 for no vertical scaling or scaling down, with reference to the scaling factor of input image n.
- n: Video channels 0 to 3 or video channels 4 to 7

Horizontal and vertical scaling factors can be set in the scaling factor registers (VnUDS\_SCALE) of the UDS. For details, refer to the hardware manual.

For convenience of explanation, the following expressions are used for calculation in section 5.7.4, D) Example of Bandwidth Calculation.

\[
\text{h} \_\text{scale} = \frac{\text{HORIout}}{\text{HORIin}} \\
\text{v} \_\text{scale} = \frac{\text{VERTout}}{\text{VERTin}}
\]

- HORIin: Number of pixels horizontally in the input plane (CSI2 or digital interface)
- VERTin: Number of lines in the input plane (CSI2 or digital interface)
- HORIout: Number of pixels horizontally in the output plane
- VERTout: Number of lines in the output plane
5.7.4 D) Example of Bandwidth Calculation

The bandwidth required for VIN operation is the peak bandwidth for images input to the VIN. The following shows an example of calculation.

Example: To use two video channels VIN0 and VIN4

VIN0: Video clock frequency = 148.5 MHz, frame rate = 60 fps, image size = Full HD, color depth = 4 bytes/pixel, and UDS is not used.
VIN4: Video clock frequency = 37.125 MHz, frame rate = 60 fps, image size = 960 × 540, color depth = 4 bytes/pixel, and UDS is used for scaling up to 1920 × 1080 pixels.

Bandwidth required of four VIN channels (VIN0 to VIN3) = \( \sum_{VIN0}^{VIN3} \) input video clock frequency \( \times \) factor of scaling up \( \times \) output color depth
= 148.5 (MHz) \( \times \) 1 \( \times \) 4 (bytes/pixel) = 594 \( \approx \) 600 (Mbytes/s)

Bandwidth required of four VIN channels (VIN4 to VIN7) = \( \sum_{VIN4}^{VIN7} \) input video clock frequency \( \times \) factor of scaling up \( \times \) output color depth
= 37.125 (MHz) \( \times \) (2 \( \times \) 3) \( \times \) 4 (bytes/pixel) = 891 \( \approx \) 900 (Mbytes/s)

When the required bandwidth calculated is specified for a QoS parameter, the IP module operates as shown in Figure 5-49.

![Figure 5-49 CSI2 and VIN Operation with Sample QoS Setting](image)
5.8 FDP

Version 1.x R-Car D3 devices do not have the FDP module. This section is not applicable to version 1.x R-Car D3 devices.

5.8.1 A) Maximum Performance

(1) Version 1.1 of the R-Car M3-W

Performance of the FDP required for a use case must satisfy both conditions (a) and (b) for the maximum performance of the FDP described below.

(a) Maximum performance of the FDP for pixel rate

- The maximum performance for pixel rate per FDP interface is 500 Mevids/s (equivalent to Full HD at 240 fps).

(b) Maximum performance of the FDP for frame rate

- The maximum performance for frame rate per FDP interface is 480 fps.
- The total frame rate for all sequences that a single FDP interface processes through time division must be no greater than 480 fps.

(2) Version 2.0 and 3.0 of the R-Car H3

The description on the maximum performance of the FDP is the same as that for version 1.1 of the R-Car M3-W. Refer to (1) Version 1.1 of the R-Car M3-W in this section.

(3) Version 1.x of the R-Car M3-N

The description on the maximum performance of the FDP is the same as that for version 1.1 of the R-Car M3-W. Refer to (1) Version 1.1 of the R-Car M3-W in this section.

(4) Version 1.x of the R-Car E3

Performance of the FDP required for a use case must satisfy both conditions (a) and (b) for the maximum performance of the FDP described below.

(a) Maximum performance of the FDP for pixel rate

- The maximum performance for pixel rate per FDP interface is 125 Mevids/s (equivalent to Full HD at 60 fps).

(b) Maximum performance of the FDP for frame rate

- The maximum performance for frame rate per FDP interface is 120 fps.
- The total frame rate for all sequences that a single FDP interface processes through time division must be no greater than 120 fps.
5.8.2 B) Concepts of Deriving Performance

(1) Concepts of Deriving Required Performance

The performance required of the FDP is estimated from the image size on the output side.

When interlaced-to-progressive conversion is enabled, the FDP converts a single field of data into one frame of data as shown in Figure 5-50. Accordingly, the output images are vertically twice as large as the input images.

![Figure 5-50 Estimation of FDP Performance (Interlaced-to-Progressive Conversion is Enabled)](image)

When interlaced-to-progressive conversion is disabled (progressive images pass through the FDP), the FDP outputs input images without changing their size as shown in Figure 5-51. Though either the size at the input or output can be used in estimating the processing performance of the FDP, use that on the output side in general to take account of cases where interlaced-to-progressive conversion is enabled.

![Figure 5-51 Estimation of FDP Performance (Interlaced-to-Progressive Conversion is Disabled)](image)
(2) Estimating Required Performance for Pixel Rate

When the FDP processes several sequences, the FDP switches between the sequences in frame units in a time division manner. In such cases, the following performance for pixel rate is required.

\[
\text{Required performance [pixel/s]} = \left( \sum_{i=0}^{i<8} (\text{FrameSize}[i] \times \text{FrameRate}[i]) \right)_{i=0}^{i<8}
\]

FrameSize[i]: Number of pixels per frame in the image data which the FDP outputs in the i-th sequence (number of pixels horizontally × number of lines)

FrameRate[i]: Frame rate (fps) for image data which the FDP outputs in the i-th sequence

The required performance for pixel rate obtained from the above expression must not be greater than the maximum performance for pixel rate of the FDP.
5.8.3 C) Concepts of Deriving Bandwidth

The times for processing by the FDP IP module depend on the required bandwidth value specified for a QoS parameter (refer to section 3.2, QoS Settings and IP Processing Time). The required bandwidth can be calculated in three ways. The following shows the characteristics of each calculation method. Use the attached video and display bandwidth calculation sheet to calculate the actual bandwidth.

Table 5-56  FDP Bandwidth Calculation Methods and Characteristics

<table>
<thead>
<tr>
<th>Required Bandwidth Calculation Method</th>
<th>Advantages and Disadvantages in Terms of Characteristics</th>
</tr>
</thead>
<tbody>
<tr>
<td>Case 1  To operate the IP module at the maximum performance</td>
<td>Advantage: The FDP IP module operates at the maximum performance.</td>
</tr>
<tr>
<td></td>
<td>Disadvantage: As the bandwidth required for the FDP becomes large, the bandwidths that can be assigned to other IP modules are reduced.</td>
</tr>
<tr>
<td>Case 2 (recommended)  To complete processing within the period for one frame</td>
<td>Recommended: Use this calculation to complete processing of the sequence having the highest frame rate within the period for one frame. Compared to case 1, the processing time becomes longer but larger bandwidths can be assigned to other IP modules. Note: If the calculated value is greater than that in case 1, the processing cannot be done while keeping the cycles at the maximum frame rate. In this case, use the value calculated in case 1.</td>
</tr>
<tr>
<td>Case 3  To only satisfy the frame rate</td>
<td>Disadvantage: The minimum bandwidth required to satisfy the frame rate defined for each sequence is assigned. Although the defined frame rate can be satisfied, processing for some sequences may not be completed within the period for one frame.</td>
</tr>
<tr>
<td></td>
<td>Advantage: Compared to case 2, larger bandwidths can be assigned to other IP modules.</td>
</tr>
</tbody>
</table>

When reading lossless compressed data, the bandwidth depends on the compression rate. Either of the two cases shown in Table 5-57 may apply.

Table 5-57  FDP Bandwidth Calculation Cases for Reading Lossless Compressed Data

<table>
<thead>
<tr>
<th>Compression Rate Case</th>
<th>Read Bandwidth</th>
<th>Reference: Compressed data assumed</th>
</tr>
</thead>
<tbody>
<tr>
<td>Typical case</td>
<td>Read bandwidth is 55% of the worst case.</td>
<td>Compressed data producing standard bandwidth</td>
</tr>
<tr>
<td>Worst case</td>
<td>Theoretically maximum bandwidth (same as the bandwidth without compression)</td>
<td>Compressed data for testing, intended to produce a high bandwidth</td>
</tr>
</tbody>
</table>
Figure 5-52 describes the terms and symbols used in the descriptions and expressions on the following pages.

**Input plane**
- **HORI_{in}**: Number of pixels horizontally in the input plane
- **VERT_{in}**: Number of lines in the input plane
- **BPP_{in}**: Color depth in the input plane (byte/pixel)
- **HORI_{in} \times VERT_{in} \times M**: Total number of pixels to be read in the input plane
- **M**: When 3D fixed IPC or 2D/3D adaptive IPC* is enabled, the value is determined by the format of images input to the FDP1 as follows.
  - YCbCr4:2:0 or YCbCr4:2:2: 2
  - YCbCr4:4:4: 5/3
  - Others: 1

**Output plane**
- **HORI_{out}**: Number of pixels horizontally in the output plane
- **VERT_{out}**: Number of lines in the output plane
- **BPP_{out}**: Color depth in the output plane (byte/pixel)

**Sequence**
- **Frame rate**: 
  - **FrameRate_{out}**: Frame rate for the output plane (fps)
  - **FrameRate_{i}**: Frame rate for the sequence

**Frame rate**
- **Sequence i = N – 1**: Image size of output plane
- **Sequence i = 0**: Image size of input plane
- **Input color depth**: BPP_{in}
- **Output color depth**: BPP_{out}

*Note: IPC is an abbreviation for the interlaced-to-progressive converter.*

For details, refer to section 33.1.1, Features, under the section on Fine Display Processor (FDP1) in the hardware manual, etc.
The required bandwidth can be calculated in three ways. Select one from among cases 1 to 3.


### Table 5-58  FDP Bandwidth Calculation Expressions

<table>
<thead>
<tr>
<th>Required Bandwidth Calculation Method</th>
<th>Read/Write</th>
<th>Description and Expression</th>
</tr>
</thead>
</table>
| Case 1 To operate the IP module at the maximum performance | Read | Description: \( \{ \text{Maximum performance [Mpixel/s]} \} \times \{ \text{maximum of the input color depths [byte/pixel]} \} \)  
Expression: \( (500 \text{ or } 125) \times \{ \text{MAXi}\times(BPPin) \} \)  
Write | Description: \( \{ \text{Maximum performance [Mpixel/s]} \} \times \{ \text{maximum of the output color depths [byte/pixel]} \} \)  
Expression: \( (500 \text{ or } 125) \times \{ \text{MAXi}\times(BPPout) \} \) |
| Case 2 To complete processing within the period for one frame | Read | Description: \( \sum \{ \text{total number of pixels to be read in input plane} \times \text{input color depth} \} \times \{ \text{maximum of the output frame rates [fps]} \} \)  
Expression: \( \sum \{ \text{HORIin} \times \text{VERTin} \times \text{M} \times BPPin \} \times \{ \text{MAXi}\times(\text{FrameRateout}) \} \)  
Write | Description: \( \sum \{ \text{number of pixels in output plane} \times \text{output color depth} \} \times \{ \text{maximum of the output frame rates [fps]} \} \)  
Expression: \( \sum \{ \text{HORIout} \times \text{VERTout} \times BPPout \} \times \{ \text{MAXi}\times(\text{FrameRateout}) \} \) |
| Case 3 To only satisfy the frame rate | Read | Description: \( \sum \{ \text{total number of pixels to be read in input plane} \times \text{input color depth} \} \times \{ \text{output frame rate [fps]} \} \)  
Expression: \( \sum \{ \text{HORIin} \times \text{VERTin} \times M \times BPPin \} \times \{ \text{FrameRateout[fps]} \} \)  
Write | Description: \( \sum \{ \text{number of pixels in output plane} \times \text{output color depth} \} \times \{ \text{output frame rate [fps]} \} \)  
Expression: \( \sum \{ \text{HORIout} \times \text{VERTout} \times BPPout \} \times \{ \text{FrameRateout[fps]} \} \) |

Note: In case 2 or 3, if the calculated value is greater than the value calculated in case 1, the required frame rate cannot be satisfied. In this case, use case 1.
5.8.4 D) Examples of Bandwidth Calculation

(1) Version 1.1 of the R-Car M3-W

The following shows the calculation of required bandwidth in each case using an example where two sequences operate simultaneously at different frame rates.

Sequence 0 (Full HD at 60p is input and IP conversion is disabled):

Calculate bandwidths for input = Full HD at 60p and output = Full HD at 60p.

Sequence 1 (Full HD at 15i is input and IP conversion is enabled):

Calculate bandwidths for input = Full HD at 15i and output = Full HD at 15p.

![Diagram showing bandwidth calculation examples for FDP](image)

**Figure 5-53 Overview of Bandwidth Calculation Examples for FDP**

Notes:
1. When the color format of the images input to the FDP is YCbCr4:2:0 semi-planar, the input color depth is 2 bytes/pixel. For details, refer to section 5.2, Relationships between Data Types and Color Depths.
2. When IP conversion is enabled, set the vertical size of the input plane to half the size of the output plane.
Case 1: To operate the IP module at the maximum performance

### Table 5-59 Examples of Bandwidth Calculation for FDP (Case 1)

<table>
<thead>
<tr>
<th>Required Bandwidth Calculation Method</th>
<th>Read/Write</th>
<th>Description and Expression</th>
</tr>
</thead>
<tbody>
<tr>
<td>To operate the IP module at the maximum performance</td>
<td>Read</td>
<td>Description: (Maximum performance [Mpixel/s]) ( \times ) (maximum of the input color depths [byte/pixel])&lt;br&gt;Expression: ( 500 \ [\text{Mpixels/s}] \times \text{MAX} (BPPin) [\text{byte/pixel}] )&lt;br&gt;Example: ( 500 \ [\text{Mpixels/s}] \times \text{MAX} (2, 2) [\text{byte/pixel}] = 500 \times 2 = 1000 [\text{Mbytes/s}] )</td>
</tr>
<tr>
<td></td>
<td>Write</td>
<td>Description: (Maximum performance [Mpixel/s]) ( \times ) (maximum of the output color depths [byte/pixel])&lt;br&gt;Expression: ( 500 \ [\text{Mpixels/s}] \times \text{MAX} (BPPout) [\text{byte/pixel}] )&lt;br&gt;Example: ( 500 \ [\text{Mpixels/s}] \times \text{MAX} (1.5, 2) [\text{byte/pixel}] = 500 \times 2 = 1000 [\text{Mbytes/s}] )</td>
</tr>
</tbody>
</table>

When the required bandwidth calculated is specified for a QoS parameter, the IP module operates as shown in Figure 5-54.

![Figure 5-54  FDP Operation with Sample QoS Setting (Case 1)](image-url)
• Case 2: To complete processing within the period for one frame

### Table 5-60  Examples of Bandwidth Calculation for FDP (Case 2)

<table>
<thead>
<tr>
<th>Required Bandwidth Calculation Method</th>
<th>Read/Write</th>
<th>Description and Expression</th>
</tr>
</thead>
<tbody>
<tr>
<td>Case 2 To complete processing within the period for one frame</td>
<td>Read</td>
<td>Description: ( \sum_i ) (total number of pixels to be read in input plane ( \times ) input color depth) [byte/frame] ( \times ) (maximum of the output frame rates [fps])</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Expression: ( \sum (\text{HORIn} \times \text{VERTin} \times M \times \text{BPPin}) ) [byte/frame] ( \times ) (MAX, (FrameRateout) [fps])</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Example: ( {1920 \times 1080 \times 1 \times 2 + 1920 \times 540 \times 2 \times 2 } \times 60 \approx 498 \text{ MBytes/s} )</td>
</tr>
<tr>
<td></td>
<td>Write</td>
<td>Description: ( \sum (\text{number of pixels in output plane} \times \text{output color depth}) ) [byte/frame] ( \times ) (maximum of the output frame rates [fps])</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Expression: ( \sum (\text{HOROut} \times \text{VERTout} \times \text{BPPout}) ) [byte/frame] ( \times ) (MAX, (FrameRateout) [fps])</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Example: ( {1920 \times 1080 \times 1.5 + 1920 \times 1080 \times 2 } \times 60 = 436 \text{ MBytes/s} )</td>
</tr>
</tbody>
</table>

When the required bandwidth calculated is specified for a QoS parameter, the IP module operates as shown in Figure 5-55.
Case 3: To only satisfy the frame rate

Table 5-61  Examples of Bandwidth Calculation for FDP (Case 3)

<table>
<thead>
<tr>
<th>Required Bandwidth Calculation Method</th>
<th>Read/Write</th>
<th>Description and Expression</th>
</tr>
</thead>
<tbody>
<tr>
<td>Case 3: To only satisfy the frame rate</td>
<td>Read</td>
<td><strong>Description</strong> ( \Sigma ) ({total number of pixels to be read in input plane [pixel/frame]} \times {input color depth [byte/pixel]} \times {output frame rate [fps]})</td>
</tr>
<tr>
<td></td>
<td></td>
<td><strong>Expression</strong> ( \Sigma ) ({HORI_{in} \times VERT_{in} \times M} [pixel/frame]) \times {BPP_{in} [byte/pixel]} \times {FrameRate_{out}[fps]})</td>
</tr>
<tr>
<td></td>
<td>Write</td>
<td><strong>Description</strong> ( \Sigma ) ({number of pixels in output plane [pixel/frame]} \times {output color depth [byte/pixel]} \times {output frame rate [fps]})</td>
</tr>
<tr>
<td></td>
<td></td>
<td><strong>Expression</strong> ( \Sigma ) ({HORI_{out} \times VERT_{out}} [pixel/frame]) \times {BPP_{out} [byte/pixel]} \times {FrameRate_{out}[fps]})</td>
</tr>
</tbody>
</table>

**Example**

Case 3: To only satisfy the frame rate

- **Read**
  \[
  \sum \left( \text{HORI}_{in} \times \text{VERT}_{in} \times M \right) \times \text{BPP}_{in} \times \text{FrameRate}_{out} = (1920 \times 1080 \times 1) \times 2 \times 60 + (1920 \times 540 \times 2) \times 2 \times 15 \approx 312 \text{ Mbyte/s}
  \]

- **Write**
  \[
  \sum \left( \text{HORI}_{out} \times \text{VERT}_{out} \right) \times \text{BPP}_{out} \times \text{FrameRate}_{out} = (1920 \times 1080) \times 1.5 \times 60 + (1920 \times 1080) \times 2 \times 15 \approx 249 \text{ Mbyte/s}
  \]

When the required bandwidth calculated is specified for a QoS parameter, the IP module operates as shown in Figure 5-56.
(2) Version 2.0 and 3.0 of the R-Car H3
The description on the examples of the bandwidth calculation is the same as that for version 1.1 of the R-Car M3-W. Refer to (1) Version 1.1 of the R-Car M3-W in this section.

(3) Version 1.x of the R-Car M3-N
The description on the examples of the bandwidth calculation is the same as that for version 1.1 of the R-Car M3-W. Refer to (1) Version 1.1 of the R-Car M3-W in this section.
(4) **Version 1.x of the R-Car E3**

The following shows the calculation of required bandwidth in each case using an example where two sequences operate simultaneously at different frame rates.

Sequence 0 (Full HD at 30p is input and IP conversion is disabled):
- Calculate bandwidths for input = Full HD at 30p and output = Full HD at 30p.

Sequence 1 (Full HD at 15i is input and IP conversion is enabled):
- Calculate bandwidths for input = Full HD at 15i and output = Full HD at 15p.

---

**Figure 5-57 Overview of Bandwidth Calculation Examples for FDP**

Notes:
1. When the color format of the images input to the FDP is YCbCr4:2:0 semi-planar, the input color depth is 2 bytes/pixel. For details, refer to section 5.2. Relationships between Data Types and Color Depths.
2. When IP conversion is enabled, set the vertical size of the input plane to half the size of the output plane.
Case 1: To operate the IP module at the maximum performance

Table 5-62  Examples of Bandwidth Calculation for FDP (Case 1)

<table>
<thead>
<tr>
<th>Required Bandwidth Calculation Method</th>
<th>Read/Write</th>
<th>Description and Expression</th>
</tr>
</thead>
<tbody>
<tr>
<td>Case 1</td>
<td>Read</td>
<td>Description: {Maximum performance [Mpixel/s]} (\times) {maximum of the input color depths [byte/pixel]}</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Expression: 125 [Mpixels/s] (\times) (\text{MAX}(\text{BPPin})) [byte/pixel]</td>
</tr>
<tr>
<td></td>
<td>Example</td>
<td>125 [Mpixels/s] (\times) MAX (2, 2) [bytes/pixel] = 125 \times 2 = 250 [Mbytes/s]</td>
</tr>
<tr>
<td>Case 1</td>
<td>Write</td>
<td>Description: {Maximum performance [Mpixel/s]} (\times) {maximum of the output color depths [byte/pixel]}</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Expression: 125 [Mpixels/s] (\times) (\text{MAX}(\text{BPPout})) [byte/pixel]</td>
</tr>
<tr>
<td></td>
<td>Example</td>
<td>125 [Mpixels/s] (\times) MAX (1.5, 2) [bytes/pixel] = 125 \times 2 = 250 [Mbytes/s]</td>
</tr>
</tbody>
</table>

When the required bandwidth calculated is specified for a QoS parameter, the IP module operates as shown in Figure 5-58.
Case 2: To complete processing within the period for one frame

Table 5-63 Examples of Bandwidth Calculation for FDP (Case 2)

<table>
<thead>
<tr>
<th>Required Bandwidth Calculation Method</th>
<th>Read/Write</th>
<th>Description and Expression</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Case 2</strong></td>
<td>Read</td>
<td>{( \sum ) (total number of pixels to be read in input plane \times input color depth) [byte/frame]} \times {maximum of the output frame rates [fps]}</td>
</tr>
<tr>
<td><strong>To complete processing within the period for one frame</strong></td>
<td>Expression</td>
<td>{( \sum ) (HORin \times VERTin \times M \times BPPin) [byte/frame]} \times {MAX. (FrameRateout) [fps]}</td>
</tr>
<tr>
<td><strong>Case 2</strong></td>
<td>Example</td>
<td>{1920 \times 1080 \times 1 \times 2 + 1920 \times 540 \times 2 \times 2 [bytes/frame]} \times 30 \approx 250 [Mbytes/s]</td>
</tr>
<tr>
<td>Write</td>
<td>Description</td>
<td>{( \sum ) (number of pixels in output plane \times output color depth) [byte/frame]} \times {maximum of the output frame rates [fps]}</td>
</tr>
<tr>
<td>Write</td>
<td>Expression</td>
<td>{( \sum ) (HORout \times VERTout \times BPPout) [byte/frame]} \times {MAX. (FrameRateout) [fps]}</td>
</tr>
<tr>
<td>Write</td>
<td>Example</td>
<td>{1920 \times 1080 \times 1.5 + 1920 \times 1080 \times 2 [bytes/frame]} \times 30 \approx 218 [Mbytes/s]</td>
</tr>
</tbody>
</table>

When the required bandwidth calculated is specified for a QoS parameter, the IP module operates as shown in Figure 5-59.

![Figure 5-59  FDP Operation with Sample QoS Setting (Case 2)](image-url)
- Case 3: To only satisfy the frame rate

### Table 5-64  Examples of Bandwidth Calculation for FDP (Case 3)

<table>
<thead>
<tr>
<th>Required Bandwidth Calculation Method</th>
<th>Read/Write</th>
<th>Description and Expression</th>
</tr>
</thead>
<tbody>
<tr>
<td>Case 3</td>
<td>Read</td>
<td>$\sum_i \left( \text{total number of pixels to be read in input plane [pixel/frame]} \times \text{input color depth [byte/pixel]} \times \text{output frame rate [fps]} \right)$</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$\sum_i \left( \text{(HORin} \times \text{VERTin} \times \text{M) [pixel/frame]} \times \text{BPPin [byte/pixel]} \times \text{FrameRateout[fps]} \right)$</td>
</tr>
<tr>
<td>To only satisfy the frame rate</td>
<td>Example</td>
<td>$(1920 \times 1080 \times 1) \times 2 \times 30 \approx 187 \text{ [Mbytes/s]}$</td>
</tr>
<tr>
<td></td>
<td>Write</td>
<td>$\sum_i \left( \text{number of pixels in output plane [pixel/frame]} \times \text{output color depth [byte/pixel]} \times \text{output frame rate [fps]} \right)$</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$\sum_i \left( \text{(HORout} \times \text{VERTout) [pixel/frame]} \times \text{BPPout [byte/pixel]} \times \text{FrameRateout[fps]} \right)$</td>
</tr>
<tr>
<td></td>
<td>Example</td>
<td>$(1920 \times 1080) \times 1.5 \times 30 \times 2 \times 15 \approx 156 \text{ [Mbytes/s]}$</td>
</tr>
</tbody>
</table>

When the required bandwidth calculated is specified for a QoS parameter, the IP module operates as shown in Figure 5-60.

**Figure 5-60  FDP Operation with Sample QoS Setting (Case 3)**
5.8.5 Usage Notes

Handling images decoded by the VCP4 and iVDP1C
Images decoded by the VCP4 and iVDP1C are not stored in external memory in the order of raster scanning but in tile units in a zig-zag order. In addition, when lossless data compression is enabled, the images stored in the memory are compressed. Accordingly, decompression and rearrangement in the order of raster scanning are required to display the images.

This processing is done in the read paths of the FDP. Therefore, even if interlaced-to-progressive conversion is not to proceed (or is unnecessary), the FDP module should be used for this processing.

Handling input images from the VIN
When images are input from the VIN in interlaced mode, the system in use must define whether the first field is the top or bottom field. When interlaced-to-progressive conversion is enabled, whether the image data input to the FDP is for the top or bottom field must be set correctly in the FDP register.
6. References

- R-Car Series, 3rd Generation User's Manual: Hardware Ver. 0.80
- Guide to Setting QoS Parameters
## Revision History

<table>
<thead>
<tr>
<th>Rev.</th>
<th>Date</th>
<th>Description</th>
<th>Page</th>
<th>Summary</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.05</td>
<td>September, 2017</td>
<td>—</td>
<td>1</td>
<td>First edition issued</td>
</tr>
<tr>
<td></td>
<td></td>
<td>16, 25, 36, 48, 51, 61, 87, 92, 94, 96, and 108</td>
<td>4</td>
<td>The description of “Version 1.x of the R-Car M3-N” added in</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Section 4.1(3), 5.3.1(3), 5.4.1(3), 5.4.4(3), 5.5.1(3), 5.5.4(3),</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>5.7.1(3), 5.7.2, 5.7.3, 5.8.1 and 5.8.4(3).</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>63</td>
<td>Section 5.6.1(3) “Maximum Performance for Pixel Rate of the VCP4” updated.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>69</td>
<td>The description of VP9 added in Section 5.6.2 and 5.6.3.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>36 to 38</td>
<td>The description of “Maximum performance of the VSPB” in Section 5.4.1(3) updated.</td>
</tr>
<tr>
<td></td>
<td>June, 2018</td>
<td>Target readers and target devices have been updated.</td>
<td>1</td>
<td>Version 1.x of the R-Car E3 has been added in section 1 “Target LSIs”.</td>
</tr>
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<td></td>
<td></td>
<td>18, 19</td>
<td>18, 19</td>
<td>Section 4.1(4) has been added.</td>
</tr>
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<td></td>
<td></td>
<td>28, 29</td>
<td>28, 29</td>
<td>Section 5.3.1(4) has been added.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>42 to 44</td>
<td>42 to 44</td>
<td>Section 5.4.1(4) has been added.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>54</td>
<td>54</td>
<td>Section 5.4.4(4) has been added.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>58 to 59</td>
<td>58 to 59</td>
<td>Section 5.5.1(4) has been added.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>70</td>
<td>70</td>
<td>Section 5.5.4(4) has been added.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>77, 78</td>
<td>77, 78</td>
<td>Section 5.6.1(3) (c) has been added.</td>
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<td>80</td>
<td>80</td>
<td>Section 5.6.1(4)(b) has been added.</td>
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<tr>
<td></td>
<td></td>
<td>87</td>
<td>87</td>
<td>Version 1.x of the R-Car E3 has been added in section 5.6.2 (1)(f).</td>
</tr>
<tr>
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<td></td>
<td>101, 102</td>
<td>101, 102</td>
<td>Section 5.7.1(4) has been added.</td>
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<td></td>
<td></td>
<td>107</td>
<td>107</td>
<td>Table 5-45 has been added.</td>
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<td></td>
<td></td>
<td>110</td>
<td>110</td>
<td>Description of version 1.x of the R-Car E3 has been added in section 5.7.3 (3).</td>
</tr>
<tr>
<td></td>
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<td>112</td>
<td>112</td>
<td>Section 5.8.1(4) has been added.</td>
</tr>
<tr>
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<td></td>
<td>122</td>
<td>122</td>
<td>Section 5.8.4(4) has been added.</td>
</tr>
<tr>
<td>1.08</td>
<td>August, 2018</td>
<td>Version 3.0 of the R-Car H3 has been added to target devices.</td>
<td>1</td>
<td>Version 3.0 of the R-Car H3 has been added in section 1 “Target LSIs”.</td>
</tr>
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<td></td>
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<td>14, 15</td>
<td>14, 15</td>
<td>Version 3.0 of the R-Car H3 has been added in section 4.1(2).</td>
</tr>
<tr>
<td></td>
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<td>26</td>
<td>26</td>
<td>Version 3.0 of the R-Car H3 has been added in section 5.3.1(2).</td>
</tr>
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<td>35</td>
<td>Version 3.0 of the R-Car H3 has been added in section 5.4.1(2).</td>
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<td></td>
<td></td>
<td>54</td>
<td>54</td>
<td>Version 3.0 of the R-Car H3 has been added in section 5.4.4(2).</td>
</tr>
<tr>
<td></td>
<td></td>
<td>57</td>
<td>57</td>
<td>Version 3.0 of the R-Car H3 has been added in section 5.5.1(2).</td>
</tr>
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<td></td>
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<td>70</td>
<td>Version 3.0 of the R-Car H3 has been added in section 5.5.4(2).</td>
</tr>
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<td></td>
<td></td>
<td>72</td>
<td>72</td>
<td>Version 3.0 of the R-Car H3 has been added in section 5.6.1(3)(a).</td>
</tr>
<tr>
<td></td>
<td></td>
<td>79</td>
<td>79</td>
<td>Version 3.0 of the R-Car H3 has been added in section 5.6.1(4)(a).</td>
</tr>
<tr>
<td></td>
<td></td>
<td>97, 98</td>
<td>97, 98</td>
<td>Version 3.0 of the R-Car H3 has been added in section 5.7.1(2).</td>
</tr>
<tr>
<td></td>
<td></td>
<td>106</td>
<td>106</td>
<td>Version 3.0 of the R-Car H3 has been added in section 5.7.2(4).</td>
</tr>
<tr>
<td></td>
<td></td>
<td>110</td>
<td>110</td>
<td>Version 3.0 of the R-Car H3 has been added in section 5.7.3(3).</td>
</tr>
<tr>
<td></td>
<td></td>
<td>112</td>
<td>112</td>
<td>Version 3.0 of the R-Car H3 has been added in section 5.8.1(2).</td>
</tr>
<tr>
<td></td>
<td></td>
<td>122</td>
<td>122</td>
<td>Version 3.0 of the R-Car H3 has been added in section 5.8.4(2).</td>
</tr>
<tr>
<td>Rev.</td>
<td>Date</td>
<td>Description</td>
<td>Page</td>
<td>Summary</td>
</tr>
<tr>
<td>------</td>
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<td>------</td>
<td>---------</td>
</tr>
<tr>
<td>1.10</td>
<td>August, 2018</td>
<td>R-Car D3 has been added in [Target Readers].</td>
<td>1</td>
<td>Version 3.0 of the R-Car D3 has been added to target devices.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Version 1.x of the R-Car D3 has been added in section 1 “Target LSIs”.</td>
<td>4</td>
<td></td>
</tr>
<tr>
<td>8, 9, 11</td>
<td></td>
<td>VSPBS has been added in table 3-1, table 3-2, and figure 3-2.</td>
<td>19</td>
<td>IMR1 has been deleted in table 4-10.</td>
</tr>
<tr>
<td>20, 21</td>
<td></td>
<td>Section 4.1 (5) has been added.</td>
<td>24</td>
<td>VSPBS has been added in table 5-3.</td>
</tr>
<tr>
<td>25</td>
<td></td>
<td>VSPBS has been added in table 5-4.</td>
<td>26</td>
<td>VSPBS has been added in table 5-5.</td>
</tr>
<tr>
<td>31, 32</td>
<td></td>
<td>Section 5.3.1 (5) has been added.</td>
<td>36</td>
<td>VSPBS has been added to the title of section 5.4.</td>
</tr>
<tr>
<td>49 to 51</td>
<td></td>
<td>Section 5.4.1 (5) has been added.</td>
<td>52, 53</td>
<td>VSPBS has been added in section 5.4.2.</td>
</tr>
<tr>
<td>54 to 56</td>
<td></td>
<td>VSPBS has been added in section 5.4.3.</td>
<td>55</td>
<td>Figure 5-13 has been updated.</td>
</tr>
<tr>
<td>56</td>
<td></td>
<td>Description for case 1 has been updated in table 5-14.</td>
<td>62 to 65</td>
<td>Section 5.4.4 (4) has been updated.</td>
</tr>
<tr>
<td>66</td>
<td></td>
<td>Section 5.4.4 (5) has been added.</td>
<td>82 to 85</td>
<td>Section 5.5.4 (4) has been updated.</td>
</tr>
<tr>
<td>118, 119</td>
<td></td>
<td>Section 5.7.1 (5) has been added.</td>
<td>127</td>
<td>Version 1.x of the R-Car D3 has been added to the title of section 5.7.3 (3).</td>
</tr>
<tr>
<td>134</td>
<td></td>
<td>Description for case 1 has been updated in table 5-58.</td>
<td>140 to 143</td>
<td>Section 5.8.4 (4) has been updated.</td>
</tr>
</tbody>
</table>
### General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

<table>
<thead>
<tr>
<th>1. Handling of Unused Pins</th>
</tr>
</thead>
<tbody>
<tr>
<td>Handle unused pins in accordance with the directions given under Handling of Unused Pins in the manual.</td>
</tr>
<tr>
<td>— The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>2. Processing at Power-on</th>
</tr>
</thead>
<tbody>
<tr>
<td>The state of the product is undefined at the moment when power is supplied.</td>
</tr>
<tr>
<td>— The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.</td>
</tr>
<tr>
<td>In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.</td>
</tr>
<tr>
<td>In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>3. Prohibition of Access to Reserved Addresses</th>
</tr>
</thead>
<tbody>
<tr>
<td>Access to reserved addresses is prohibited.</td>
</tr>
<tr>
<td>— The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>4. Clock Signals</th>
</tr>
</thead>
<tbody>
<tr>
<td>After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.</td>
</tr>
<tr>
<td>— When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>5. Differences between Products</th>
</tr>
</thead>
<tbody>
<tr>
<td>Before changing from one product to another, i.e. to a product with a different part number, confirm that the change will not lead to problems.</td>
</tr>
<tr>
<td>— The characteristics of Microprocessing unit or Microcontroller unit products in the same group but having a different part number may differ in terms of the internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.</td>
</tr>
</tbody>
</table>
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(Ren 4.0.1 November 2017)