Description

The ZSSC4151C is a member of Renesas's family of CMOS integrated circuits for highly accurate amplification and sensor-specific correction of differential bridge sensor signals. Featuring a maximum analog pre-amplification of 200, the ZSSC4151C is adjustable to nearly all resistive sensor bridges.

Digital compensation of offset, sensitivity, temperature drift, and nonlinearity is accomplished via a 16-bit RISC microcontroller. Calibration coefficients and configuration data are stored in the ZSSC4151C nonvolatile memory (NVM), which is reliable in automotive applications.

Measured values are provided via a ratiometric analog output signal at the AOUT pin. End-of-line calibration is also supported through this output pin via Renesas's ZACwire™ one-wire interface (OWI). Digital calibration helps keep assembly cost low as no trimming by external devices or lasers is needed.

The ZSSC4151C is optimized for automotive environments by over-voltage and reverse-polarity protection circuitry, excellent electromagnetic compatibility, and multiple diagnostic features.

Typical Applications

- Fluid brake pressure sensing (PV)
- Hydraulic pressure sensing
  (e.g., steering systems with hydraulic steering support)
- Pneumatic pressure sensing
  (e.g., air brake systems; pneumatic shock absorbers)

Available Support

- Evaluation Kit
- Application Notes
- Calculation Tools

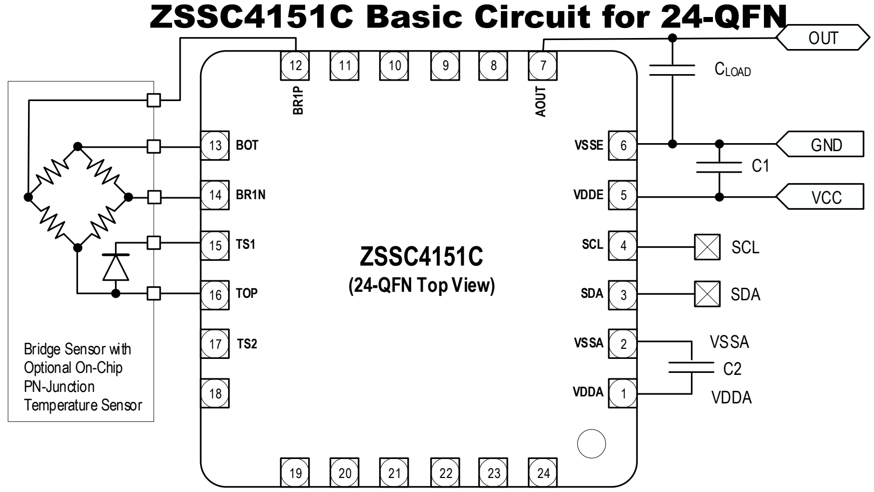
Features

- Differential bridge sensor input and on-chip or external temperature sensors, selectable for conditioning of sensor input signal
- Digital compensation for offset, gain, and higher-order nonlinearity as well as temperature coefficients of the measured bridge sensor input signal
- Operating temperature range: -40°C to 150°C
- Accuracy: ±1.0% FS at -40°C to 150°C
- Nonvolatile memory (NVM) for configuration, calibration data, and configurable measurement, and conditioning functionality
- Configurable for nearly all resistive bridge sensors
- One-pass, end-of-line calibration algorithm minimizes production costs
- No external trimming or components required
- Qualified according to the AEC-Q100 Grade 0 automotive standard

Physical Characteristics

- Supply voltage: 4.5V to 5.5V
- Continuous over-voltage and reverse-polarity protection – no duration limit: up to +/-40V
- Bridge sensor input span: 1 to 800 mV/V
- Bridge sensor signal ADC resolution: 12 to 18 bit
- Output resolution: 12-bit analog output; signed 16-bit readout for raw data acquisition
- Delivery options:
  - 24-QFN (4.0 × 4.0 mm; wettable flanks);
  - 16-TSSOP (5.0 × 4.4 mm exposed pad)
  - Tested die; tested wafer

ZSSC4151C Basic Circuit for 24-QFN



Contents

1. Pin Assignments....4
1.1 Pin Layout for 24-QFN Package....4
1.2 Pin Layout for 16-TSSOP Package....4
2. Pin Descriptions....5
3. Absolute Maximum Ratings....6
4. Operating Conditions....7
5. Electrical Characteristics....8
5.1 Supply Current and System Operation Conditions....8
5.2 Analog Front-End Characteristics....8
5.3 A2D Conversion....9
5.4 Temperature Measurement....9
5.5 Sensor Diagnostic Tasks....9
5.6 DAC and Analog Output (AOUT Pin)....9
5.7 System Response....10
5.8 Power Management....11
6. Interface Characteristics and Nonvolatile Memory....12
6.1 I2C Interface – only for production purposes....12
6.2 ZACwire™ One-Wire Interface (OWI at the AOUT pin) – only for production purposes....13
6.3 Nonvolatile Memory (NVM)....13
7. Circuit Description....14
7.1 Signal Path....15
7.2 Signal Measurement....16
7.2.1 Full Bridge Sensor Measurement....16
7.2.2 Temperature Measurements....16
7.2.3 Measurement Cycle....16
7.3 Analog Front-End....17
7.3.1 Overview....17
7.3.2 SCCM....17
7.3.3 Input Multiplexer....17
7.3.4 Programmable Gain Amplifier....17
7.3.5 Analog-to-Digital Converter....18
7.4 Signal Conditioning....18
7.4.1 Full Bridge Sensor Signal Conditioning....18
7.4.2 Conditioning Cycle....18
7.5 Output Stage....18
8. Fault-Safe Operation....19
8.1 Fault-Safe Operation Modes....19
8.1.1 Timing Definitions....20

8.2 Diagnostic Output 20
8.3 Over-Voltage, Reverse-Polarity, and Short-Circuit Protection 20
9. Application Circuit and External Components 22
10. ESD Protection and EMC Specification 23
10.1 ESD Protection 23
10.2 Latch-Up Immunity 23
10.3 Electromagnetic Emission 23
10.4 Conducted Susceptibility (DPI) 24
11. Reliability and RoHS Conformity 24
12. Package Outline Drawings 24
13. Marking Diagram 25
14. Ordering Information 26
15. Glossary 27
16. Revision History 28

List of Figures

Figure 1. 24-QFN Pin Assignments – Top View 4
Figure 2. 16-TSSOP Pin Assignments – Top View 4
Figure 3. ZSSC4151C Block Diagram 14
Figure 4. Main Signal Path 15
Figure 5. ZSSC4151C Principle Measurement Cycle 16
Figure 6. 24-QFN Application Circuit Example: Pressure and Temperature Sensor with Analog Output 22
Figure 7. 16-TSSOP Application Circuit Example: Pressure and Temperature Sensor with Analog Output 22

List of Tables

Table 1. ZSSC4151C Pin Descriptions 24-QFN Package 5
Table 2. Absolute Maximum Ratings 6
Table 3. Operating Conditions 7
Table 4. Electrical Parameters 8
Table 5. Interface Characteristics and Nonvolatile Memory 12
Table 6. Adjustable PGA Gains and Resulting Sensor Signal Spans and Common Mode Ranges 17
Table 7. Timing Parameters 20
Table 8 Protection Features 21
Table 9. Dimensioning of External Components for the Application Example 23
Table 10. Conducted Susceptibility (DPI) Tests 24

1. Pin Assignments

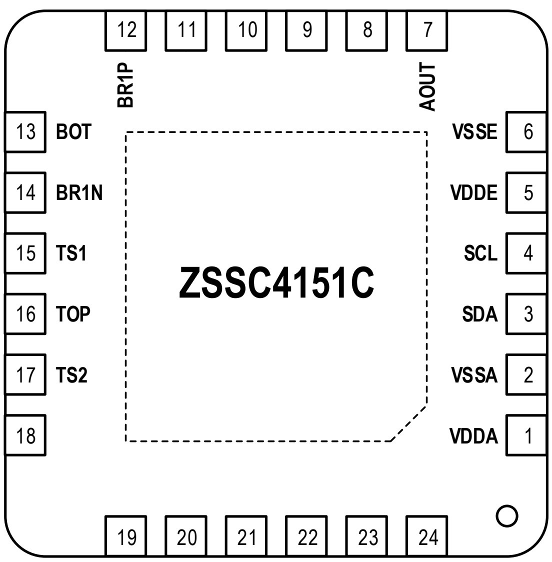
In addition to tested die and wafer, the ZSSC4151C is available in a 24-QFN RoHS-conformant package (4 × 4 mm; wettable flanks) and in a 16-TSSOP package (5.0 x 4.4 mm according to JEDEC MO-153) with an exposed pad. For details regarding die and wafers, refer to the *ZSSC4151C Technical Note – Die and Pad Dimensions,* which is available on request (see last page for contact information).

Recommendation: On the printed circuit board (PCB), the land pattern of the exposed pad should be shorted to the solder pad of the VSSA pin.

1.1 Pin Layout for 24-QFN Package

Note: The backside of the 24-QFN package (exposed pad; see section 12) is electrically connected to VSSA. A solder connection to the exposed pad of the 24-QFN package is not needed.

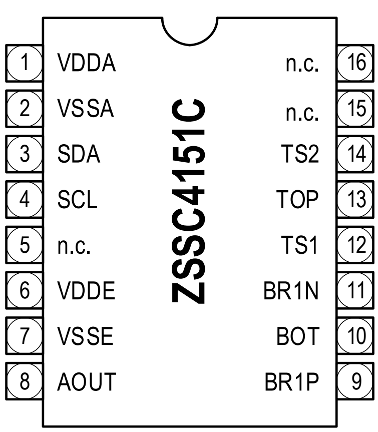
Figure 1. 24-QFN Pin Assignments – Top View



1.2 Pin Layout for 16-TSSOP Package

Note: The backside of the package 16-TSSOP (exposed pad; see section 12) is electrically connected to VSSA. A solder connection to the exposed pad of the 16-TSSOP package is not needed.

Figure 2. 16-TSSOP Pin Assignments – Top View



2. Pin Descriptions

Table 1. ZSSC4151C Pin Descriptions 24-QFN Package

Note: Pins designated as "n.c." (no connection) are not internally connected. VSSA can be routed using these pins.

24-QFN Pin	16-TSSOP Pin	Pin Name	Type	Description
1	1	VDDA	Supply	Internal supply
2	2	VSSA	Ground	Internal ground
3	3	SDA [a], [b]	Analog I/O	I2C data input/output (optional communication interface)
4	4	SCL [a], [b]	Analog Input	I2C clock (optional communication interface)
–	5	–	–	n.c. [b]
5	6	VDDE	Supply	External supply
6	7	VSSE	Analog	External ground
7	8	AOUT	Analog	Analog output and ZACwire™ one-wire interface (OWI) input/output
8 to 11	–	–	–	n.c. [b] for 24-QFN package.
12	9	BR1P	Analog	Positive bridge sensor input
13	10	BOT	Analog	Negative bridge supply voltage
14	11	BR1N	Analog	Negative bridge sensor input
15	12	TS1	Analog	External temperature sensor input 1. Note: Either TS1 or TS2 can be used for the external temperature sensor input, but not both at the same time.
16	13	TOP	Analog	Positive bridge supply voltage
17	14	TS2	Analog	External temperature sensor input 2. Note: Either TS1 or TS2 can be used for the external temperature sensor input, but not both at the same time.
18 to 24	15 to 16	–	–	n.c. [b]
–		EPAD [c]	Ground	Internal ground; connected to VSSA

[a] Internal pull-up.

[b] No connection required. Pins marked as "n.c." are not internally connected and have no physical connection to the silicon.

[c] External ground pad on the bottom of the package. Recommendation: Connect the EPAD externally to VSSA (pin 2). Note: The EPAD has a high-ohmic connection to the internal ground VSSA.

3. Absolute Maximum Ratings

The absolute maximum ratings are stress ratings only. Stresses greater than those listed below can cause permanent damage to the device. Functional operation of the ZSSC4151C at absolute maximum ratings is not implied. Exposure to absolute maximum rating conditions might affect device reliability.

Table 2. Absolute Maximum Ratings

Requirement	Parameter	Symbol	Conditions	Min	Max	Unit
DS_001	Supply voltage	V_{DDE_ABS}		-40	40	VDC
DS_002	Voltage at AOUT pin	V_{AOUT_ABS}		-40	40	VDC
DS_003	Pin voltage difference	V_{DIFF_ABS}	Voltage between any two of these pins: VDDE, AOUT and VSSE	-40	40	V
DS_004	Analog supply voltage	V_{DDA_ABS}	On-chip controlled voltage; do not supply externally	-0.3	6.5	VDC
DS_005	Voltage at all other pins	V_{PIN_ABS}	Maximum voltage is V_{DDA} + 0.3V	-0.3	6	V
DS_006	Junction temperature [a]	T_{J_ABS}		-50	160 [a]	°C
DS_007	Storage temperature	T_{STOR_ABS}		-55	155	°C

[a] The specified junction temperature range T_J is required for both normal operation and all protection cases. In the event of an over-voltage, the device might have increased power dissipation. Depending on the sensor elements and the output load, this could lead to a violation of the maximum junction temperature.

4. Operating Conditions

Important note: The operating conditions given this section set the conditions over which Renesas specifies device operation. These are the device conditions that the application circuit must not exceed for it to function as intended. Unless otherwise noted, the limits for parameters that appear in the operating conditions section are used as the test conditions for the limits given in this section, section 5 (Electrical Characteristics), and section 6 (Interface Characteristics and Nonvolatile Memory).

All voltages in this section are relative to VSSA unless otherwise noted.

Table 3. Operating Conditions

Requirement	Parameter	Symbol	Conditions	Min	Typical	Max	Unit
DS_050	Supply voltage	V_{DDE}	VDDE to VSSE	4.5	5	5.5	V
DS_051	Operating supply voltage [a]	V_{DDE_OP}	VDDE to VSSE; specified accuracy is not guaranteed in this range. Note for a supply voltage greater than 5.5V: Above the over-voltage limitation threshold, the output potential is clipped at this threshold.	V_{PWR_ON}		6	V
DS_052	Ambient temperature	T_{TQE}	Extended Temperature Range (TQE)	-40		150	°C
		T_{TQA}	Advanced-Performance Temperature Range (TQA)	-40		125	°C
Informational [b]	Thermal resistance 24-QFN [a]	$R_{th\_JA\_QFN\ 24}$	According to JESD 51		32		K/W
Informational [b]	Thermal resistance 16-TSSOP [a] with EPAD	$R_{th\_JA\_TSSOP16}$	According to JESD 51		38		K/W
DS_053	Bridge resistance [a], [c]	R_{BR}	Output range 4% to 96%	2		15	kΩ
		$R_{BR\_10\text{-}90}$	Output range 10% to 90%	1		15	kΩ

[a] No measurement in mass production; parameter is guaranteed by design and/or quality observation.

[b] Package-related parameter.

[c] R_{BR} greater than the maximum limit can result in higher noise.

5. Electrical Characteristics

All parameter values in this section are valid under the operating conditions specified in section 4 (unless otherwise stated). All voltages are referenced to VSSA pin.

Note: All parameters are measured/validated for r_{ADC} = 14-bit; segmentation of 1st and 2nd ADC stage = 8/6; f_{OSC} = 8.0MHz; analog gain = ~100; and T_{TQE} (see specification DS_052). Changing the AD conversion settings influences all timing parameters.

Table 4. Electrical Parameters

Note: See important table notes at the end of the table.

Requirement	Parameter	Symbol	Conditions	Min	Typ	Max	Unit
5.1 Supply Current and System Operation Conditions							
DS_100	Supply current	I_S	Excluding the sensor supply current and excluding output current at AOUT pin; oscillator adjusted.		5.5	7	mA
DS_101	Over-voltage power consumption [a]	P_{OV}	5.5V < V_{DDE} < 40V; excluding sensor and output load.			250	mW
DS_102	Sensor bridge supply voltage	V_{SENS}	$V_{SENS} = V_{TOP} - V_{BOT}$ where V_{TOP} is the voltage at the TOP pin and V_{BOT} is the voltage at BOT pin.	0.9		1	V_{DDA}
DS_103	Oscillator frequency	f_{OSC}	Adjusted.	7.2	8.0	8.8	MHz
DS_104	Analog supply voltage	V_{DDA}	V_{DDA} is limited if V_{DDE} exceeds the threshold $V_{OV\_LIM\_TH}$; see DS_226. V_{DDA} must not be supplied externally.	0.9		1	V_{DDE}
5.2 Analog Front-End Characteristics							
DS_120	Input span	V_{IN_SPAN}		±1		±800	mV/V
DS_121	Input voltage range	V_{IN_RNG1}	Analog gain = 1 Corresponds to V_{ADC_IN}.	0.05		0.95	V_{SENS}
DS_122		V_{IN_RNG2}	Analog gain = 2 to 200	0.3		0.65	V_{SENS}
DS_123	External capacitance at input[a]	C_{IN_EXT}	Capacitance at BR1P and BR1N to VSSA pins, see DS_124.	0		10 +20%	nF
DS_124	Time constant at input pins [a]	$6 \times C_{IN} \times R_{BR}$	Capacitance either at BRP, BRN to VSSA or between BRP and BRN pins. Calculation: $C_{IN} \leq 30\mu s / (6 * R_{BR})$ Time constant can be extended by configuration.	0	30		µs
DS_125	Input leakage current [a]	I_{IN_leak}		-15		15	nA

Requirement	Parameter	Symbol	Conditions	Min	Typ	Max	Unit
5.3 A2D Conversion							
DS_130	ADC resolution [a]	r_{ADC}		12		18	Bit
DS_131	DNL[a]	DNL_{ADC}	Best fit; overall AFE; V_{ADC_IN} according to DS_134.			0.95	LSB
DS_132	INL in TQA temperature range [a]	INL_{ADC_TQA}	Best fit.			4	LSB
DS_133	INL in TQE temperature range	INL_{ADC_TQE}	Best fit.			8	LSB
DS_134	ADC input range	V_{ADC_IN}		0.05		0.95	V_{SENS}
5.4 Temperature Measurement							
Informational [a]	Internal PTAT temperature sensor measurement range [a]	OPR_{TS}	Important: This range exceeds operating conditions for T_{J_ABS}.	-60		200	°C
DS_140	Internal PTAT temperature sensitivity	ST_{TSI}	Raw values, without conditioning calculation. Analog gain = 12.6	20			LSB/K
DS_141	External temperature diode channel gain	A_{TSE_D}		3			LSB/mV
DS_142	External temperature diode bias current	I_{TSE_D}		10	20	40	µA
DS_143	External temperature diode input range [a]	V_{TSE_D}	Relative to V_{TOP}.	-1		-0.2	V
DS_144	External bridge TC channel gain	A_{TSE_BRTC}		3			LSB/mV
DS_145	External bridge TC input voltage range [a]	V_{TSE_BRTC}	Relative to VDDA.	-1		-0.2	V
DS_146	External RTD channel gain	A_{TSE_RTD}		10			LSB/mV
DS_147	External RTD input range [a]	V_{TSE_RTD}	Relative to VDDA.	-2		-0.2	V
5.5 Sensor Diagnostic Tasks							
DS_151	Sensor connection loss threshold [b]	R_{SCC}		20		240	kΩ
DS_152	Sensor short threshold	R_{SSC}		50		1000	Ω
5.6 DAC and Analog Output (AOUT Pin)							
DS_161	DAC resolution [a]	r_{DAC}	Analog output.		12		Bit
DS_162	Output current sink/source	$\lvert I_{OUT\_SRC/SINK} \rvert$	V_{AOUT}: 5% to 95%, $R_{LOAD} \geq 2k\Omega$			2.65	mA
DS_163			V_{AOUT}: 10% to 90%, $R_{LOAD} \geq 1k\Omega$			5	mA
DS_164	Output current driving capability[g]	I_{OUT}	Adjusted.	-6		6	mA

Requirement	Parameter	Symbol	Conditions	Min	Typ	Max	Unit
DS_165	Short-circuit current (AOUT to VSSE or VDDE)[h]	I_{OUT_max}	Short to VSSE or VDDE; adjusted.	-25		25	mA
DS_166	Addressable output range [a]	V_{R_OUT}		0.04		0.96	V_{DDE}
DS_167		V_{R_OUT90}	$R_{LOAD} \geq 2k\Omega$	0.05		0.95	V_{DDE}
DS_168		V_{R_OUT80}	$R_{LOAD} \geq 1k\Omega$	0.10		0.90	V_{DDE}
DS_169	Load capacitance[a]	C_{LOAD}	Defined for best EMC performance.	4	47	100 +20%	nF
DS_170	Output slew rate[a]	SR_{OUT}	C_{LOAD} < 50nF	0.1			V/µs
DS_171	Clipping levels	LowLim	Configurable 8-bit value stored in NVM.	0.1		25	$\%V_{DDE}$
		UppLim	Configurable 8-bit value stored in NVM.	75		99.9	$\%V_{DDE}$
DS_179	Clipping adjustment step [a]	$Step_{CLIP}$				0.1	$\%V_{DDE}$
DS_180	Output resistance in Diagnostic Mode [a]	R_{OUT_DIA}	Diagnostic Range: 4% to 96%, $R_{LOAD} \geq 2k\Omega$ 8% to 92%, $R_{LOAD} \geq 1k\Omega$			80	Ω
DS_172	DNL	DNL_{OUT}	r_{DAC} =12 bit	-0.99		0.99	LSB
DS_173	INL in TQA temperature range [a]	INL_{OUT}	Best fit, r_{DAC} =12-bit	-5		5	LSB
DS_174	INL in TQE temperature range	INL_{OUT}	Best fit, r_{DAC} =12-bit	-8		8	LSB
DS_175	Output to ground leakage current in TQA [a]	$I_{LEAK\_OUT\_GND\_TQA}$	At ground loss, R_{LOAD} → ground.	-12		0.1	µA
DS_176	Output to power leakage current in TQA [a]	$I_{LEAK\_OUT\_PWR\_TQA}$	At power loss, R_{LOAD} → power.	-0.1		12	µA
DS_177	Output to ground leakage current in TQE	$I_{LEAK\_OUT\_GND\_TQE}$	At ground loss, R_{LOAD} → ground.	-20		0.1	µA
DS_178	Output to power leakage current in TQE	$I_{LEAK\_OUT\_PWR\_TQA}$	At power loss, R_{LOAD} → power	-0.1		20	µA
5.7 System Response							
DS_200	Startup time [a], [c] (time to first valid output after power-on)	$t_{STARTUP}$				7	ms
DS_201	Output update rate [a]	OUR	Output update rate; depends on the configuration used.			0.5	ms
DS_202	Output response time [a] [c] [d]	ORT	100% input step; depends on the configuration used.			1.0	ms
DS_203	Diagnostic testing interval [a]	DTI	Depends on configuration used.			10	ms

Requirement	Parameter	Symbol	Conditions	Min	Typ	Max	Unit
DS_204	Failure reaction time [a]	FRT	Time between failure detection and reaction by the ZSSC4151C; depends on configuration used.			20	ms
DS_205	Failure messaging time [a]	FMT	Time between occurrence of a failure event and reporting on the analog output (assuming one single failure confirmation); depends on the configuration used.			20	ms
DS_206	Analog output noise peak-to-peak [a]	$V_{NOISE,PP}$	DAC and output buffer only. Bandwidth ≤ 10kHz			10	mV
DS_207	Analog output noise RMS [a]	$V_{NOISE,RMS}$	DAC and output buffer only. Bandwidth ≤ 10kHz			3	mV
DS_208	Ratiometricity error [a]	RE_{OUT_5}	Maximum error: V_{DDE} range = 4.5V to 5.5V	-1900		1900	ppm
DS_209	Overall failure for bridge sensor measurement. Deviation from ideal line including INL, gain, offset, and temperature impacts; excluding sensor-caused effects [a], [e]	F_{ALL}	TQA temperature range.			0.5	% FSO
			TQE temperature range.			1.0	% FSO
5.8 Power Management							
DS_220	Power-on threshold [f]	V_{PWR_ON}		3.5		4.2	V
DS_221	Power-off threshold [f]	V_{PWR_OFF}		3.0		3.9	V
DS_222	POC hysteresis [a]	V_{POC_HYST}	Minimum/typical value for information only.	0.1	0.4		V
DS_223	Over-voltage switch-off threshold [a]	V_{OV_DISC}		9		15	V
DS_224	Over-voltage switch-off delay [a]	t_{OV_DISC}				10	ms

Requirement	Parameter	Symbol	Conditions	Min	Typ	Max	Unit
DS_225	Power-on time [a]	t_{PWR_ON}	V_{DDE} slew rate >0.1V/µs; POC is released; NVM CRC is verified.			4	ms
DS_226	Limitation threshold of internal supply voltage	$V_{OV\_LIM\_TH}$			5.8		V

[a] No measurement in mass production; parameter is guaranteed by design and/or quality observation.

[b] The specified resistor values are valid for connection loss at the bridge sensor input BR1P and BR1N pins.

- For detection of a connection loss at the positive bridge supply TOP pin, the voltage level at BR1P and/or BR1N must fall below 11% of the voltage level between the VDDA and VSSA pins.
- For detection of a connection loss at the negative bridge supply BOT pin, the voltage level at BR1P and/or BR1N must rise above 66% of the voltage level between the VDDA and VSSA pins.

[c] No bridge settling included in timing.

[d] Dependent on the configuration. The specified limit is valid only for ADC resolutions ≤ 15 bits.

[e] FSO: full-scale output. No sensor-caused effects are included in the overall error. ADC input range from 10% to 90% of V_{SENS}; DAC from 5% to 95% of output range.

[f] Power ON/OFF thresholds are tested for functionality in mass production; no level test is processed.

[g] Minimum is | I_OUT | ≥ 6mA driving current.

[h] Maximum limit is | I_OUT_MAX | ≤ 25mA

6. Interface Characteristics and Nonvolatile Memory

Table 5. Interface Characteristics and Nonvolatile Memory

Note: See important table notes at the end of the table.

Requirement	Parameter	Symbol	Conditions	Min	Typ	Max	Unit
6.1 I2C Interface – only for production purposes							
Informational	Power-on time [a]	t_{PWRUP_I2C}	Time to ready for communi-cation after power-on. V_{DDE} slew rate > 0.1V/µs			4	ms
Informational	I2C voltage level HIGH [a]	V_{I2C_HIGH}		0.8			V_{DDA}
Informational	I2C voltage level LOW [a]	V_{I2C_LOW}				0.2	V_{DDA}
Informational	Slave output level LOW [a]	$V_{I2C\_LOW\_OUT}$	Open drain. I_{OL} < 4mA			0.1	V_{DDA}
Informational	SDA load capacitance [a]	C_{I2C_SDA}				400	pF
Informational	SCL clock frequency [a]	f_{I2C}				400	kHz
Informational	Internal pull-up resistor [a]	R_{I2C_PULLUP}		25		100	kΩ

Requirement	Parameter	Symbol	Conditions	Min	Typ	Max	Unit
6.2 ZACwire™ One-Wire Interface (OWI at the AOUT pin) – only for production purposes							
Informational	Power-on time [a]	t_{PWRUP_OWI}	Time to ready for communication after power-on. V_{DDE} slew rate > 0.1V/µs			4.0	ms
DS_245	Power-on V_{DDE} slew rate	SR_{PWRUP_OWI}		0.01			V/µs
Informational	Start window [a]	$t_{OWI\_STARTWIN}$	OWI enabled latest 5ms after power-on. V_{DDE} slew rate > 0.1V/µs		250		ms
Informational	OWI voltage level HIGH [a]	$V_{OWI\_IN\_H}$	Master to slave	0.8			V_{DDE}
Informational	OWI voltage level LOW [a]	$V_{OWI\_IN\_L}$	Master to slave			0.2	V_{DDE}
Informational	Slave output level LOW [a]	$V_{OWI\_OUT\_L}$	Open drain. I_{OL} ≤ 2mA			0.1	V_{DDE}
6.3 Nonvolatile Memory (NVM)							
DS_240	Junction temperature for NVM programming [b]	T_{AMB_NVM}		-40		150	°C
DS_241	Re-write cycles [a]	N_{NVM_TQA}	For T_{TQA}.	100			
DS_242	Re-write cycles at 150°C [a]	N_{NVM_TQE}	For T_{TQE}.	10			
DS_243	Data retention [a]	t_{NVM_RET}	Temperature profile: 22h bake at 250°C.	15			Year
DS_244	Programming time [a]	t_{NVM_WRI}	Per written word		2.2	5	ms

[a] No measurement in mass production; parameter is guaranteed by design and/or quality observation.

[b] Valid for dice. Note: Additional package and temperature range cause restrictions.

7. Circuit Description

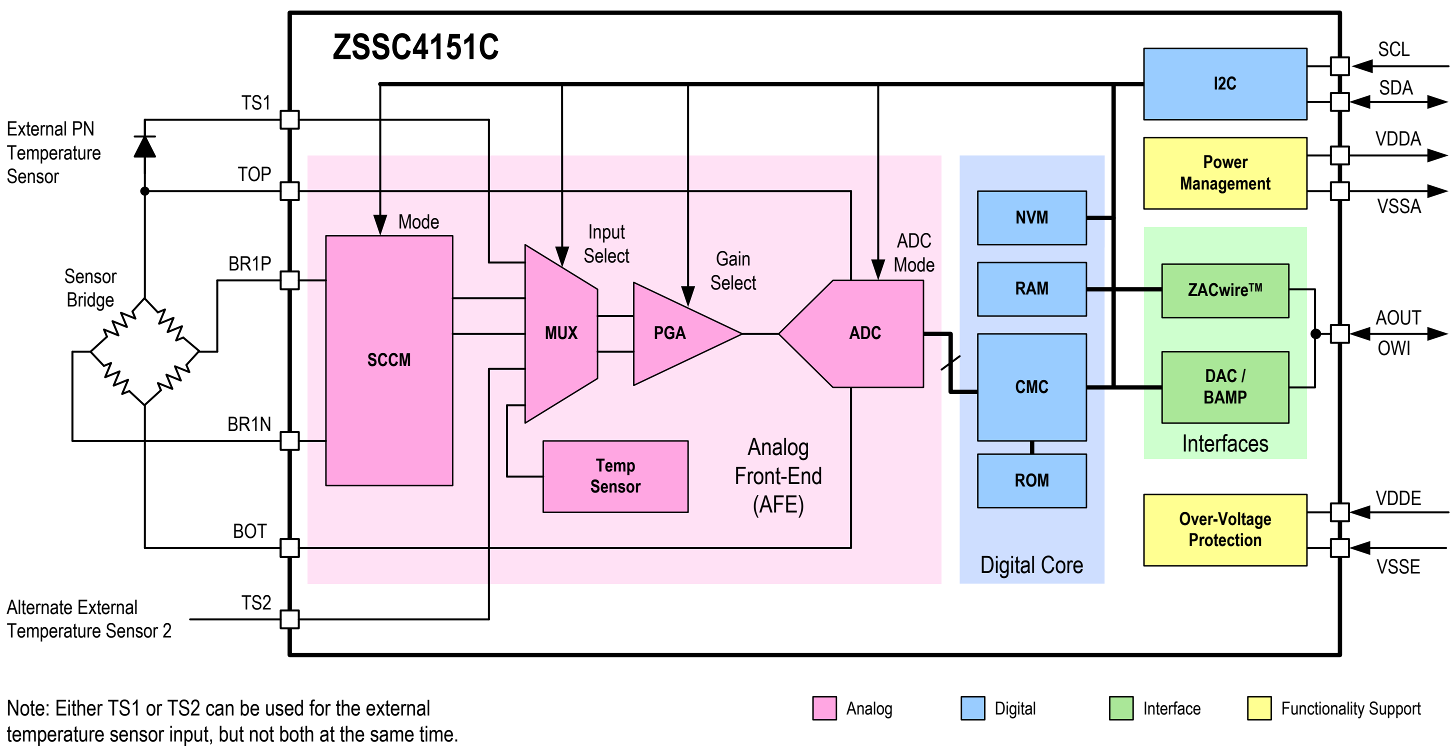
The ZSSC4151C Sensor Signal Conditioner (SSC) is a CMOS integrated circuit for highly accurate amplification and sensor-specific correction of resistive sensor element signals. Digital compensation of sensor offset, sensitivity, temperature drift, and non-linearity is accomplished via an internal 16-bit RISC microcontroller running a ROM-based correction algorithm with calibration coefficients stored in a nonvolatile memory (NVM).

The ZSSC4151C is adjustable to nearly all resistive sensor element types. Measured values are provided at the analog voltage output (AOUT). The digital interfaces OWI or I2C can be used for a simple PC-controlled calibration procedure to program a set of calibration coefficients into the on-chip NVM. The specific sensor element and the ZSSC4151C can be quickly calibrated together. The ZSSC4151C and the calibration equipment communicate digitally, so the noise sensitivity is greatly reduced. Digital calibration helps keep assembly cost low as no trimming by external devices or lasers is needed.

The ZSSC4151C is optimized for automotive environments by over-voltage and reverse-polarity protection circuitry, excellent electromagnetic compatibility, full automotive temperature range, and multiple diagnostic features.

Figure 3 provides a block diagram of the ZSSC4151C. Refer to section 14 for definitions of abbreviations.

Figure 3. ZSSC4151C Block Diagram



7.1 Signal Path

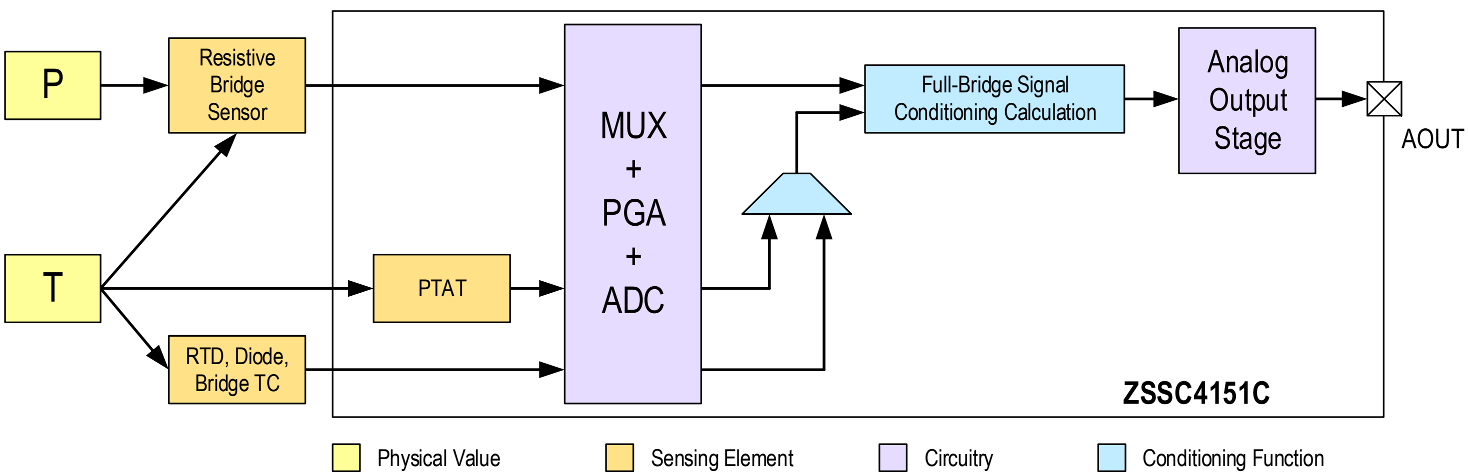
The ZSSC4151C signal path consists of the analog front-end (AFE), the digital signal processing unit, and the analog output stage. In addition, this is supported by a serial digital one-wire interface (ZACwire™) or I2C interface for calibration purposes.

The resistive bridge sensor element signal is input via the BR1P and BR1N pins and is handled as a fully differential signal. Both signal lines have a dynamic range symmetrical to the common mode potential (analog ground; equal to $V_{DDA}/2$) so that it is possible to process positive and negative differential input signals. These differential signals are pre-amplified by the programmable gain amplifier (PGA) and are converted to digital values by the A/D converter (ADC).

A multiplexer (MUX) selects and transmits the signals from either the bridge sensor or the selected temperature sensor to the analog-to-digital converter (ADC) in a defined sequence. Temperature sensors can either be an external diode, an external resistive temperature device (RTD), the internal proportional-to-absolute-temperature (PTAT), or an external bridge sensor element temperature coefficient. The temperature source is selected by NVM configuration.

The digital signal correction is processed in the calibration microcontroller (CMC) using ROM-resident correction formulas and sensor-specific coefficients stored in the NVM. The configuration data and the conditioning coefficients are programmed into the NVM during the calibration process by digital one-wire communication via the AOUT pin. During the calibration process, raw measurement values can be requested via the digital interfaces. Figure 4 illustrates the signal paths for measurement of a physical value P, such as pressure, via the external bridge sensor and measurement of a temperature value T.

Figure 4. Main Signal Path



7.2 Signal Measurement

7.2.1 Full Bridge Sensor Measurement

The ZSSC4151C measures a differential bridge sensor element signal (BR1P to BR1N). The signal path is ratiometric and fully differential. The ratiometric reference voltage V_{REF} is equal to (V_{TOP} – V_{BOT}).

7.2.2 Temperature Measurements

The ZSSC4151C supports different methods for acquiring temperature data needed for the conditioning of the sensor signal:

- Internal PTAT sensor
- External PN-junction temperature sensor connected to the TS1 or TS2 pin and referenced to the sensor top potential (TOP pin)
- External resistive half-bridge temperature sensors connected to the TS1 or TS2 pin
- Temperature coefficients of the connected resistive sensing element

7.2.3 Measurement Cycle

The measurement cycle is the sequence of measurement tasks processed continuously during the Normal Operation Mode (NOM). It delivers the raw measurement results from all connected sensor elements and from the supervision functions. The measurements are processed sequentially, all using the same ADC to convert the analog input voltages to a digital value.

All measurement tasks are executed at least once in the measurement cycle. Measurement tasks that are related to the bridge sensor element measurements are measured most frequently in the main measurement slots; all other measurements are inserted alternatively as auxiliary measurements.

The sequence of measurements is retained even if any fault check connected to a measurement is disabled. The sensor signal conditioning is synchronized to the main measurement tasks to ensure a regular internal output update rate.

The list of available measurements and the complete measurement cycle is described in the *ZSSC4151C Functional Description* in detail. Figure 5 shows the principle measurement cycle of the ZSSC4151C using the following abbreviations:

BR = Bridge Measurement

X_AZ = Auto-Zero Measurement

PTAT = Internal Temperature Sensor Measurement

BIST_AFE = Analog Frontend Built-in Self-Test

EXT_T = External Temperature Sensor Measurement

SCC = Sensor Connection Check

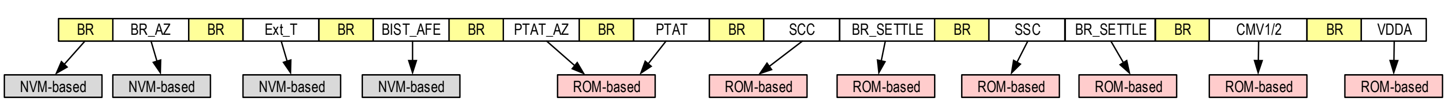
SSC = Sensor Short Check

BR_SETTLE = Bridge Settling Task

CMV = Common Mode Voltage Measurement

VDDA = V_{DDA} Measurement

Figure 5. ZSSC4151C Principle Measurement Cycle



7.3 Analog Front-End

7.3.1 Overview

The analog front-end (AFE) consists of the multiplexer (MUX), the programmable gain amplifier (PGA), and the analog-to-digital converter (ADC). The internal offset of the analog front-end is eliminated by an auto-zero compensation.

7.3.2 SCCM

The sensor check and common mode block (SCCM) implements the self-diagnostic features for the analog front-end. The SCCM block provides the sensor connection checks (short and open circuit) as well as several other diagnostic functions.

7.3.3 Input Multiplexer

The input multiplexer (MUX) selects one of the various inputs and connects it to the signal path utilizing a single ADC. It allows a very flexible signal routing between the sensor element and the ZSSC4151C.

7.3.4 Programmable Gain Amplifier

The sensor elements signal can be amplified by the on-chip programmable amplifier (PGA) using a gain between 2 and 200. Alternatively, the PGA can be bypassed and the sensor signal is applied directly to the ADC. The gain is adjustable for every single sensor measurement task individually in order to provide an ADC input signal span of greater than 50% FS.

Table 6 shows the adjustable gains for the PGA, the corresponding signal spans, and the common mode range limits.

Table 6. Adjustable PGA Gains and Resulting Sensor Signal Spans and Common Mode Ranges

Requirement	Nominal PGA Gain a_{PGA}	Maximum Input Span V_{IN_SPAN} [mV/V]	BR1P and BR1N Input Range [a] V_{IN_CM} [% V_{DDA}]
Informational	PGA bypassed	800	4 to 96
Informational	2.08	385	30 to 65
Informational	3.15	254	30 to 65
Informational	4.31	186	30 to 65
Informational	6.25	128	30 to 65
Informational	8.31	96	30 to 65
Informational	12.6	63	30 to 65
Informational	17.3	46	30 to 65
Informational	25.0	32	30 to 65
Informational	33.2	24	30 to 65
Informational	50.4	16	30 to 65
Informational	69.0	12	30 to 65
Informational	100.0	8	30 to 65
Informational	138.0	6	30 to 65
Informational	200.0	4 [b]	30 to 65

[a] Recommended range for common mode voltage of bridge (shorted BR1P and BR1P) is 40 to 60%.

[b] Digital zooming allows reducing the input span depending on application requirements.

Recommendation: To achieve the best stability and linearity performance of the AFE, operate the PGA in a differential output voltage range within 10% to 90% of the ratiometric reference voltage $V_{REF} = V_{SENS} = (V_{TOP} – V_{BOT})$. The gain must be selected to guarantee this constraint for the entire operating temperature range of the application and for the specified sensor bridge tolerances.

7.3.5 Analog-to-Digital Converter

The analog-to-digital converter is implemented using the full-differential switched-capacitor technique. The conversion is largely insensitive to short-term and long-term instabilities of the clock frequency. The ADC provides adjustability for the A/D conversion input voltage range shift.

7.4 Signal Conditioning

7.4.1 Full Bridge Sensor Signal Conditioning

The full-bridge sensor element signal conditioning uses ROM-resident formulas and sensor-element-specific coefficients stored in NVM. The calculation is processed every time that a new measurement result value is available from the analog-to-digital conversion. The conditioning calculation provides compensation of the temperature-dependent offset and gain and of the nonlinearity. All temperature sources can be selected for the conditioning calculation of the full-bridge sensor element signal.

The conditioning coefficients are stored as signed 16-bit values (sint16, two's complement) whereas the weights are stored as unsigned 4-bit values (uint4) in the NVM during the calibration process.

All intermediate results and the final conditioning results for the full-bridge are stored as signed 16-bit values (sint16, two's complement) in the RAM output memory.

7.4.2 Conditioning Cycle

The conditioning cycle is the sequence of equations and supervision functions processed during the Normal Operation Mode (NOM). It uses raw measurement results from measurement cycle and delivers conditioned output data for the analog output function.

7.5 Output Stage

The analog output is used for outputting the analog signal conditioning result and for "end of line" communication via the ZACwire™ interface one-wire communication interface (OWI). The ZSSC4151C supports four different modes of the analog output in combination with the OWI behavior:

- AOUT_CYC_OWI_DIS: Analog output will be activated after a ~7ms power on time. OWI is disabled. Only I2C communication is possible.
- AOUT_CYC: Analog output will be activated after a ~7ms power on time. OWI communication is enabled for a time window of ~250ms. Transmission of the START_CM command must occur during the time window in order to activate the Command Mode. For communication, the internal driven potential at AOUT must be overwritten by the external communication master (AOUT drive capability is current limited).
- AOUT_WIN: Analog output will be activated after the OWI start time window. OWI communication is enabled for a time window of ~250ms. Transmission of the "START_CM" command must occur during the time window.
- OWI: Analog output is deactivated; OWI communication is enabled.

The analog output potential is driven by a unity gain output buffer for which the input signal is generated by a 12-bit resistor-string DAC. The output buffer, which is a rail-to-rail op amp, is offset compensated and current limited. Therefore, a short-circuit of the analog output to ground or the power supply does not damage the ZSSC4151C.

8. Fault-Safe Operation

8.1 Fault-Safe Operation Modes

Fault checks verify the operation of the ZSSC4151C and of the connected sensing elements at power-on and during Normal Operation Mode (NOM). If a fault is detected, the Diagnostic Mode (DM) is activated and the fault status is provided via one of the two methods described below depending on the diagnostic mode.

The ZSSC4151C differentiates between two DMs with different behavior:

Static Diagnostic Mode

- Measurement and conditioning cycle are interrupted.
- Analog output transmission is stopped, and the output AOUT pin is either driven to a HIGH or LOW output level or is switched to high impedance.
- The ZACwire™ interface for one-wire communication (OWI) is enabled; both RAM output pages are readable. The command *StrtCmdMd* must be sent to switch to Command Mode for further command processing.
- If enabled, the ZSSC4151C is reset; i.e. the ZSSC4151C is restarted including a reset of all status registers.
- The ZSSC4151C can be restarted by a power-off/power-on sequence.

Temporary Diagnostic Mode

- Measurement and conditioning cycle are continuously processed.
- Fault checks are continuously processed including fault filtering (see below).
- Analog output transmission is continued; the output voltage will switch to the Lower or Upper Diagnostic Range (LDR or UDR) if enabled.
- The ZACwire™ interface for one-wire communication is enabled. The command *StrtCmdMd* must be sent to switch to Command Mode for further command processing (the analog output must be overwritten by the OWI master).
- The ZSSC4151C returns to Normal Operation Mode including normal analog output transmission of a valid sensor signal if fault checks do not detect continuation of fault conditions.

The **Fault Filtering** of the ZSSC4151C is defined as follows:

- Fault filtering is only processed for fault checks assigned to the Temporary DM.
- Fault filtering is a low-pass filter that delays the activation and deactivation of the Temporary DM.
- In the event of a fault detection, faults are re-checked before entering Temporary DM.
- In the case of Temporary DM, detected fault conditions that no longer exist are re-checked before returning from Temporary DM to NOM.
- Fault filtering is an up-and-down event counter with programmable increment, threshold, and hysteresis; the decrement is always 1.

8.1.1 Timing Definitions

The relevant timing parameters are listed in Table 7.

Table 7. Timing Parameters

Symbol	Parameter	Description
OUR	Output update rate	Internal update rate of the main signal data.
ORT	Output response time	Latency from the main signal event to the completion of the AOUT transmission of this signal event.
DTI	Diagnostic testing interval	Rate of fault check processing.
FMT	Fault messaging time	Latency from the fault event to the completion of the AOUT transmission of the fault message.

8.2 Diagnostic Output

ZSSC4151C provides various failsafe tasks to control the proper function of the device and the connected sensor element. When a fault is detected, a diagnostic output at the AOUT pin is activated if configured for this failsafe task. OWI Rx is enabled to make one-wire communication possible for reading out the failure status information. Diagnostic output means setting the analog output potential to a level in the lower diagnostic range (LDR) or in the upper diagnostic range (UDR). LDR and UDR levels are determined either by the external circuitry or are configured in the ZSSC4151C NVM.

Detected failures are messaged at AOUT pin by the following:

- UDR for ground loss (external load resistance connected to the external supply),
  LDR for ground loss (external load resistance connected to the external ground)
- UDR for supply loss (external load resistance connected to the external supply),
  LDR for supply loss (external load resistance connected to the external ground)
- LDR for oscillator fail
- LDR for NVM CRC failure and for all hardware faults until NVM content is evaluated after power-on
- LDR or UDR for all other detected faults according to the configuration in the NVM

8.3 Over-Voltage, Reverse-Polarity, and Short-Circuit Protection

ZSSC4151C is designed for a 5V supply provided by an electronic control unit (ECU).

ZSSC4151C and the connected resistive sensor element are protected from over-voltage and reverse-polarity damage by an internal supply voltage limiter. The analog output AOUT is protected regarding short circuit, over-voltage, and reverse polarity with all potentials in the protection range under all potential conditions at the VDDE and VSSE pins. These functions are described in detail in the *ZSSC4151C Technical Note – Power Management.*

ZSSC4151C protection applies when the device is operated in the application circuits shown in section 9. The protection voltage is ±40V as defined in the absolute maximum ratings (see Table 2). When the over-voltage protection is active, the device has a higher power dissipation. Depending on the ambient temperature and on the external sensor characteristics, the higher power dissipation of the device could lead to a violation of the maximum junction temperature.

Table 8 Protection Features

Requirement	VSSE Pin	AOUT Pin	VDDE Pin	Condition
DS_300	0	0 to 5V	5V	Normal Mode
DS_301	0	Open	40V	VDDE to VSSE
DS_302	0	Open	-40V	Reverse voltage
DS_303	0	40V	Open	AOUT to VSSE
DS_304	0	-40V	Open	Reverse voltage
DS_305	Open	0	40V	VDDE to AOUT
DS_306	Open	0	-40V	Reverse voltage
DS_307	0	0	40V	VDDE to (AOUT and VSSE)
DS_308	0	0	-40V	Reverse voltage
DS_309	0	40V	40V	(VDDE and AOUT) to VSSE
DS_310	0	40V	5.0V	AOUT to VSSE
DS_311	0	-40V	-40V	Reverse voltage
DS_312	0	40V	0	AOUT to (VDDE and VSSE)
DS_313	0	-40V	0	Reverse voltage AOUT
DS_314	0	-35V	5V	Reverse voltage AOUT

9. Application Circuit and External Components

Application features:

- 5V module is powered by the application's electronic control unit (ECU).
- Sensor module with 3-pin connector provides pressure measurement data via ratiometric analog output.
- The temperature signal for pressure signal correction can be derived either from the on-chip PTAT or from an external diode, PTC or bridge TC (connected to TS1 or TS2).
- End-of-line calibration uses one-wire communication via the AOUT pin.

Figure 6. 24-QFN Application Circuit Example: Pressure and Temperature Sensor with Analog Output

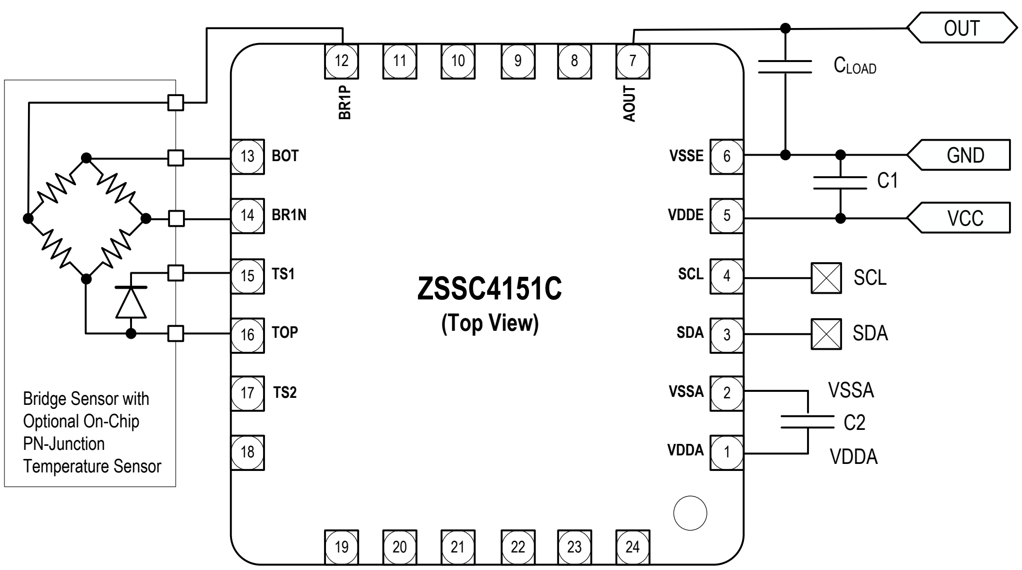


Figure 7. 16-TSSOP Application Circuit Example: Pressure and Temperature Sensor with Analog Output

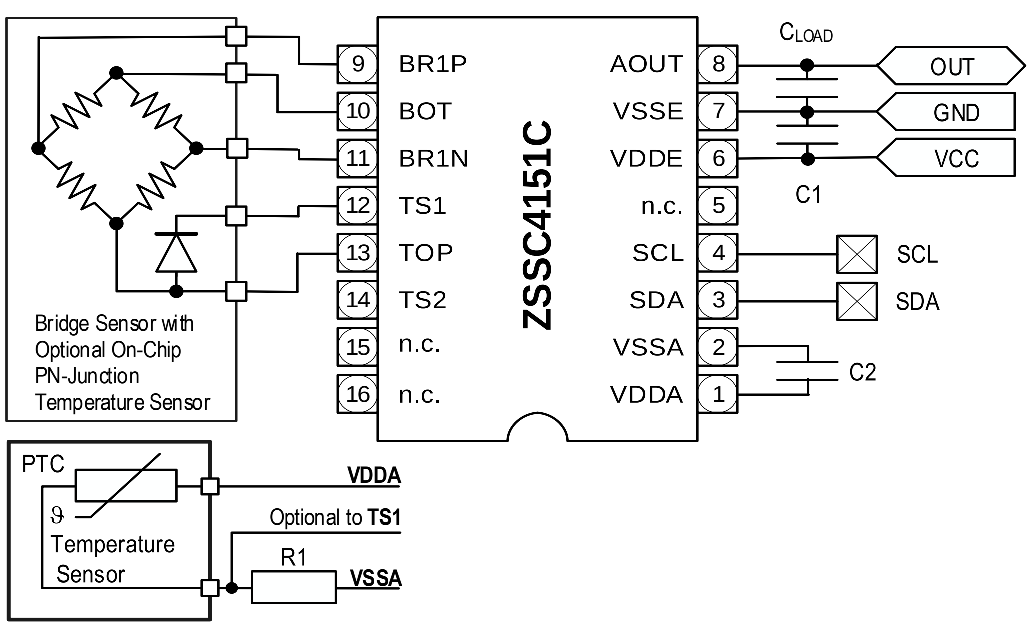


Table 9. Dimensioning of External Components for the Application Example

Note: The component values given here are examples and must be adapted to the requirements of the application, in particular to the EMC requirements.

Requirement	Component	Symbol	Conditions	Min	Typical	Max	Unit
Informational	Capacitor	C1	V_{MAX} ≥ 60V Low ESR type		100	1000 + 20%	nF
Informational	Capacitor	C2	V_{MAX} ≥ 10V Low ESR type	47 – 20%	100	220 + 20%	nF
Informational	Capacitor	C_{LOAD}	V_{MAX} ≥ 60V Low ESR type	4.7 – 20%	47	100 + 20%	nF

10. ESD Protection and EMC Specification

The level of ESD protection and EMC specifications are tested with devices in 24-QFN 4mm x 4mm packages during the product qualification.

10.1 ESD Protection

All pins have an ESD protection of ≥ 2000V according to the Human Body Model (HBM with 1.5kΩ/100pF, based on MIL883, Method 3015.7). The VDDE, VSSE, and AOUT pins have an additional ESD protection of ≥ 4000V (HBM with 1.5kΩ/100pF, based on MIL883, Method 3015.7).

In addition, Charged Device Model (CDM) tests are processed with protection levels of ≥ 750V for corner pins and ≥ 500V for all other pins.

10.2 Latch-Up Immunity

All pins pass Renesas's ±100mA latch-up test based on testing that conforms to the standard EIA/JESD 78.

10.3 Electromagnetic Emission

The wired emission of externally connected pins of the device is measured according to the following standard: *IEC 61967_4:2002 + A1:2006.*

Measurements must be performed with the application circuits described in section 9.

For the off-board pins, the spectral power measured with the 150Ω method must not exceed the limits according to *IEC 61967_4k, Annex B.4 code H10kN*. For the VSSE pin, the spectral power measured with the 1Ω method must not exceed the limits according to *IEC 61967_4k, Annex B.4 code 15KmO.*

10.4 Conducted Susceptibility (DPI)

The conducted susceptibility of externally connected pins of the device is measured according to the IEC 62132-4 standard, which describes the direct power injection (DPI) test method.

Measurements must be performed with the application circuit described in the section 9.

Measurements are performed with an internal reference capacitor and internal temperature sensor. The sensing element is replaced by a resistive divider. Calibration is parameterized so that ~50% V_{DDA} is output.

Table 10 gives the specifications for the DPI tests. RES refers to the coupling impedance.

Table 10. Conducted Susceptibility (DPI) Tests

Requirement	Test	Frequency Range	Target (dBm)	Load Pins	Protocol	Error Band	Notes
DS_350	DPI, direct coupled	1MHz to 300MHz	26	VDDE, AOUT	Analog out	± 1%	LOAD RES = 5kΩ LOAD CAP = 10nF
DS_351	DPI, direct coupled	300MHz to 1000MHz	32	VDDE, AOUT	Analog out	± 1%	LOAD RES = 5kΩ LOAD CAP = 10nF

11. Reliability and RoHS Conformity

The ZSSC4151C is qualified according to the AEC-Q100 standard, operating temperature grade 0. The qualification is extended to 1000 hours for the High Temperature Operating Life (HTOL) Test for one lot. Two manufacturing lots of extended HTOL qualification data (minimum of 1000 hours test time) for the ZSSC4151C or other products, using identical technology (metallization), the same package supplier, the same package style, and the same die size within a specific tolerance, are used to prove the package and bond reliability in the range of 1000 hours HTOL.

A FIT rate ≤ 10 FIT (temperature = 55°C, confidence level = 60%) is guaranteed. A typical FIT rate of TSMC's CV018BCD technology, which is used for the ZSSC4151C, is 1 FIT.

The ZSSC4151C complies with the RoHS directive and does not contain hazardous substances.

12. Package Outline Drawings

The package outline drawings are appended at the end of this document and are accessible from the link below. The package information is the most current data available.

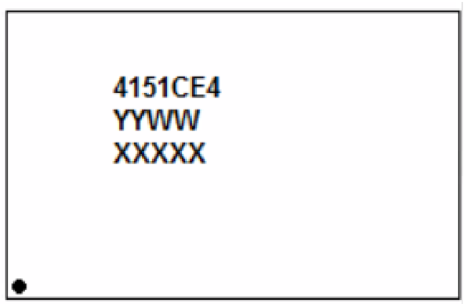
For the 24-QFN package:

24-VFQFPN, Package Outline Drawing 4.0 x 4.0 x 0.85 mm Body, 0.50mm Pitch, Epad 2.50 x 2.50 mm. Wettable Flank (Step Cut) NLG24S2 (renesas.com)

For the 16-TSSOP package:

16-TSSOP, Package Outline Drawing 5.0 x 4.4 mm Body, Epad 3.0 x 3.0 mm 0.65mm Pitch ENG16P1 (renesas.com)

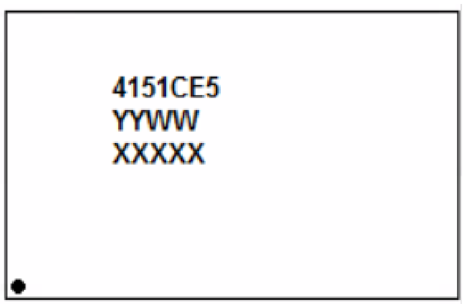
13. Marking Diagram



Line 1: “4151CE4” is the truncated part number.

Line 2: “YYWW” is the last digits of the year and week that the part was assembled.

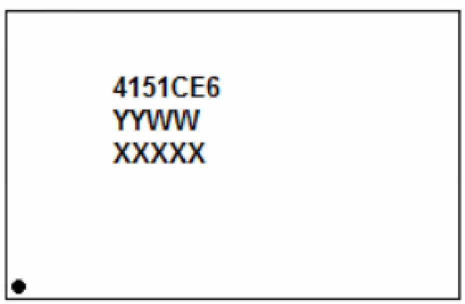
Line 3: “XXXXX” is the last digits of the lot number.



Line 1: “4151CE5” is the truncated part number.

Line 2: “YYWW” is the last digits of the year and week that the part was assembled.

Line 3: “XXXXX” is the last digits of the lot number.



Line 1: “4151CE6” is the truncated part number.

Line 2: “YYWW” is the last digits of the year and week that the part was assembled.

Line 3: “XXXXX” is the last digits of the lot number.

14. Ordering Information

Part Number	Description and Package	MSL Rating	Carrier Type	Temperature
ZSSC4151CE1B	Tested, unsawn wafer	N/A	Wafer	-40°C to 150°C
ZSSC4151CE1C	Tested, sawn die on frame	N/A	Frame	-40°C to 150°C
ZSSC4151CE1D	Tested, sawn die in waffle pack	N/A	Waffle Pack	-40°C to 150°C
ZSSC4151CE4R	4.0 mm × 4.0 mm 24-QFN, wettable flanks (step cut)	MSL1	13" Reel	-40°C to 150°C
ZSSC4151CE5R	5.0mm x 4.4mm 16-TSSOP with exposed pad, long-life version, AEC Q100 qualified part with extended HTOL test (5000 hours)	MSL1	13" Reel	-40°C to 150°C
ZSSC4151CE5T	5.0mm x 4.4mm 16-TSSOP with exposed pad, long-life version, AEC Q100 qualified part with extended HTOL test (5000 hours)	MSL1	Tube	-40°C to 150°C
ZSSC4151CE6R	5.0mm x 4.4mm 16-TSSOP with exposed pad, AEC Q100 qualified part	MSL1	13" Reel	-40°C to 150°C
ZSSC4151CE6T	5.0mm x 4.4mm 16-TSSOP with exposed pad, AEC Q100 qualified part	MSL1	Tube	-40°C to 150°C
ZSSC415XEVKV1P6	ZSSC4151 SSC Evaluation Kit: Communication Board, ZSSC415x/6x/7x Evaluation Board, Sensor Replacement Board, USB Cable, ZSSC415x Test PCB, Tweezer, 5 Samples.			

15. Glossary

Term	Description
ADC	Analog-to-Digital Converter
AEC	Automotive Electronics Council
AFE	Analog Front-End
BAMP	Buffer Amplifier
BR	Bridge Sensor
CDM	Charged Device Model
CM	Command Mode
CMC	Calibration Microcontroller
DAC	Digital-to-Analog Converter
DNL	Differential Nonlinearity
DPI	Direct Power Injection
EMC	Electromagnetic Compatibility
ESD	Electrostatic Discharge
EPAD	Exposed Pad – IC package with exposed metal plate on the bottom
FIT	Failures in Time
FSO	Full Scale Output
HBM	Human Body Model
HTOL	High Temperature Operating Life
I2C	Inter-Integrated Circuit—serial two-wire data bus
INL	Integral Nonlinearity
LSB	Least Significant Bit
MUX	Multiplexer
NVM	Nonvolatile Memory
OWI	One-Wire Interface
PGA	Programmable Gain Amplifier
PTAT	Proportional-to-Absolute Temperature
PTC	Thermistor – Positive Temperature Coefficient Resistor
PWR	Power Management and Protection Unit
QFN	Quad-Flat No-Leads – IC package
RAM	Random Access Memory
RISC	Reduced Instruction Set Computing
ROM	Read-Only Memory
RMS	Root-Mean-Square

Term	Description
RTD	Resistance Temperature Device
SCCM	Sensor Check and Common Mode Adjustment Unit
SCL	Serial Clock
SDA	Serial Data
sint	Signed Integer Value
SSC	Sensor Short Check (diagnostic feature) or Sensor Signal Conditioner
TQA, TQE	Temperature range identifier. See specification DS_052 for definition.
uint	Unsigned integer value
ZACwire™	Renesas-specific One-Wire Interface

16. Revision History

Date	Description
May 19, 2022	▪ ZSSC4151CE4W removed ▪ Renesas links updated
March 25, 2020	▪ Datasheet parameter DS_245 added ▪ Tolerance added to external component C2
September 12, 2019	▪ 16-TSSOP-related information added. ▪ Minor edits.
March 4, 2019	Initial release.

Notice

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

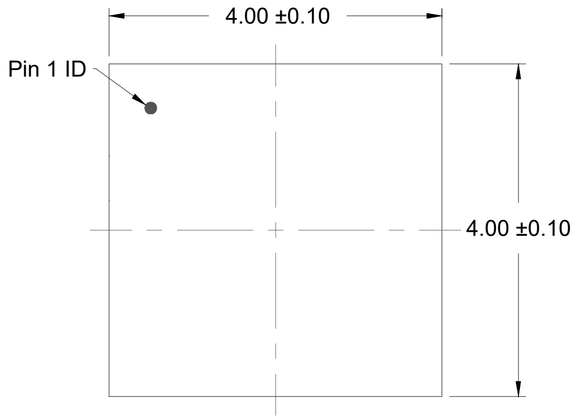
Contact information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit: www.renesas.com/contact/.

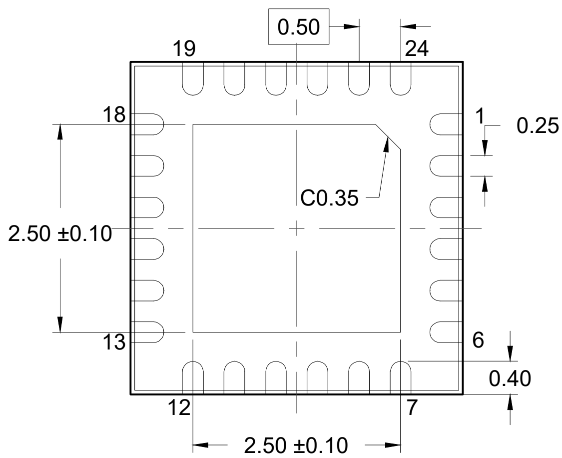
Trademarks

Package Outline Drawing

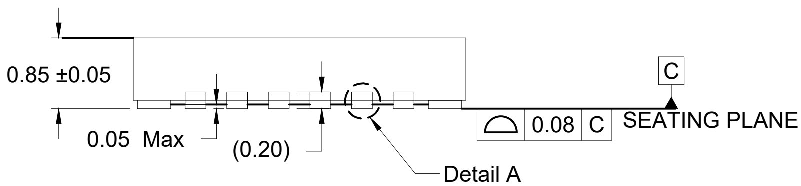
Package Code:NLG24S2
24-VFQFPN 4.0 x 4.0 x 0.85 mm Body, 0.5mm Pitch
PSC-4192-05, Revision: 06, Date Created: Aug 1, 2022



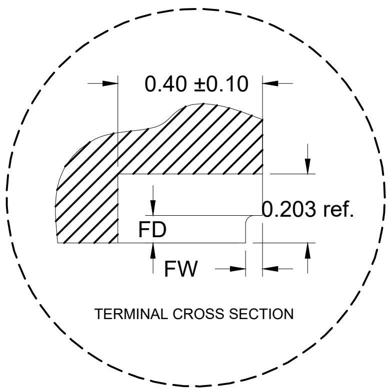
TOP VIEW



BOTTOM VIEW



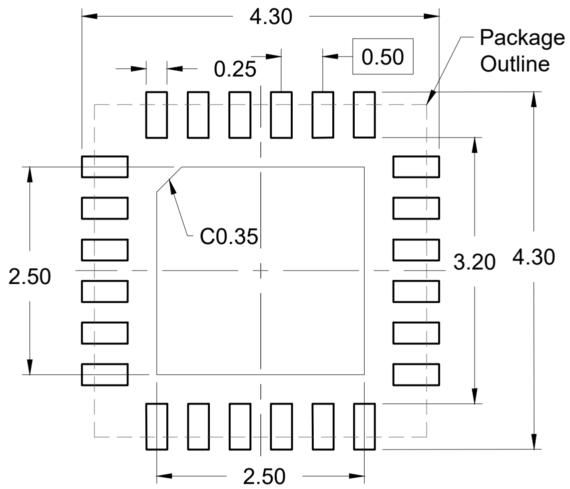
SIDE VIEW



DETAIL A

Table 1: Dimensions of wettable flank (DETAIL A)

Symbol	Unit (mm)	
	MIN	MAX
FD	0.100	-
FW	0.001	0.075



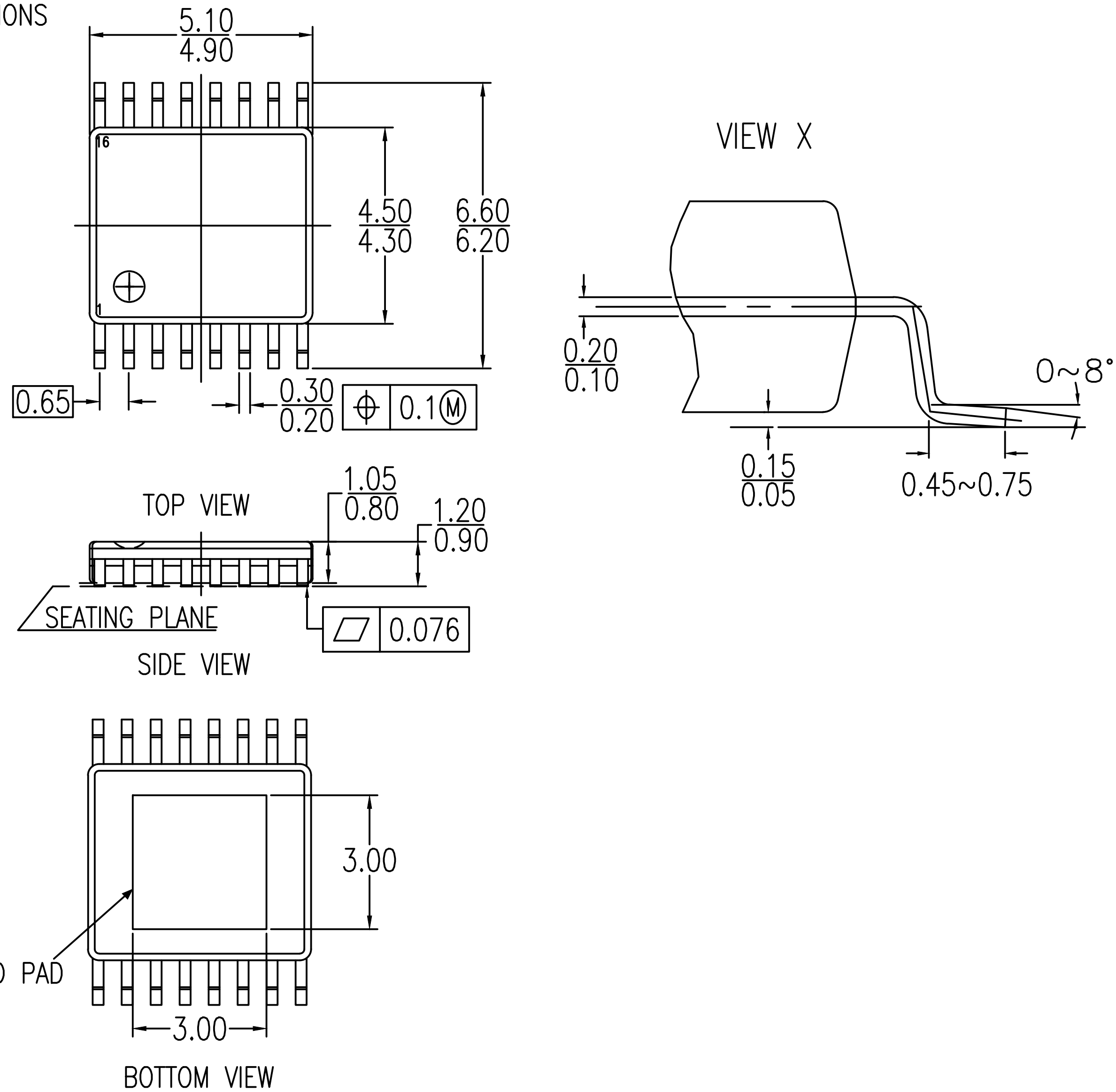
RECOMMENDED LAND PATTERN
(PCB Top View, NSMD Design)

NOTES:

1. JEDEC compatible.
2. All dimensions are in mm and angles are in degrees.
3. Use ±0.05 mm for the non-toleranced dimensions.
4. Numbers in ( ) are for references only.
5. Wettable flank (step cut).

BASED ON JEDEC JEP95: MO-153

1. DIMENSIONS



2. WEIGHT ≤ 0.05 g
3. BODY MATERIAL LOW STRESS EPOXY
4. LEAD MATERIAL Cu-ALLOY
5. LEAD FINISH SOLDER PLATING
6. LEAD FORM Z-BENDS

* WITHOUT MOLD FLASH
DIMENSIONS IN MILLIMETERS