

HCTS74MS

Radiation Hardened Dual-D Flip-Flop with Set and Reset

FN2143
Rev 2.00
September 1995

Features

- 3 Micron Radiation Hardened SOS CMOS
- Total Dose 200K RAD (Si)
- SEP Effective LET No Upsets: >100 MEV-cm²/mg
- Single Event Upset (SEU) Immunity < 2 x 10⁻⁹ Errors/Bit-Day (Typ)
- Dose Rate Survivability: >1 x 10¹² RAD (Si)/s
- Dose Rate Upset >10¹⁰ RAD (Si)/s 20ns Pulse
- Latch-Up Free Under Any Conditions
- Military Temperature Range: -55°C to +125°C
- Significant Power Reduction Compared to LSTTL ICs
- DC Operating Voltage Range: 4.5V to 5.5V
- LSTTL Input Compatibility
 - VIL = 0.8V Max
 - VIH = VCC/2 Min
- Input Current Levels $I_i \leq 5\mu\text{A}$ at VOL, VOH

Description

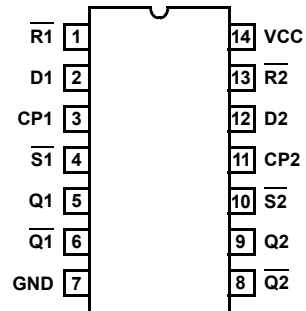
The Intersil HCTS74MS is a Radiation Hardened positive edge triggered flip-flop with set and reset.

The HCTS74MS utilizes advanced CMOS/SOS technology to achieve high-speed operation. This device is a member of radiation hardened, high-speed, CMOS/SOS Logic Family.

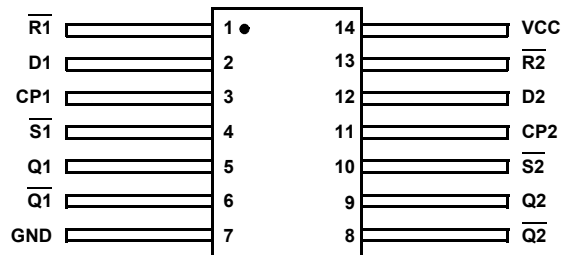
The HCTS74MS is supplied in a 14 lead Ceramic flatpack (K suffix) or a SBDIP Package (D suffix).

Pinouts

14 LEAD CERAMIC DUAL-IN-LINE
METAL SEAL PACKAGE (SBDIP)
MIL-STD-183S CDIP2-T14, LEAD FINISH C
TOP VIEW



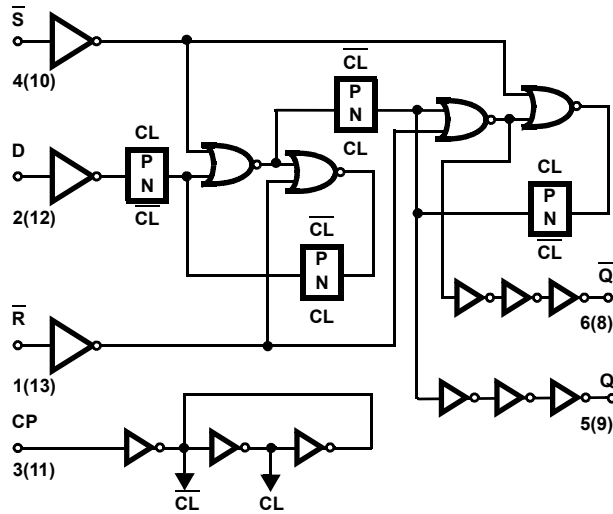
14 LEAD CERAMIC METAL SEAL
FLATPACK PACKAGE (FLATPACK)
MIL-STD-183S CDFP3-F14, LEAD FINISH C
TOP VIEW



Ordering Information

| PART NUMBER | TEMPERATURE RANGE | SCREENING LEVEL | PACKAGE |
|----------------|-------------------|-----------------------------|--------------------------|
| HCTS74DMSR | -55°C to +125°C | Intersil Class S Equivalent | 14 Lead SBDIP |
| HCTS74KMSR | -55°C to +125°C | Intersil Class S Equivalent | 14 Lead Ceramic Flatpack |
| HCTS74D/Sample | +25°C | Sample | 14 Lead SBDIP |
| HCTS74K/Sample | +25°C | Sample | 14 Lead Ceramic Flatpack |
| HCTS74HMSR | +25°C | Die | Die |

Functional Diagram



TRUTH TABLE

| INPUTS | | | | OUTPUTS | |
|-------------------------|---------------------------|----|---|---------|------------------------|
| $\overline{\text{SET}}$ | $\overline{\text{RESET}}$ | CP | D | Q | $\overline{\text{Q}}$ |
| L | H | X | X | H | L |
| H | L | X | X | L | H |
| L | L | X | X | H* | H* |
| H | H | | H | H | L |
| H | H | | L | L | H |
| H | H | L | X | Q0 | $\overline{\text{Q0}}$ |

NOTE: L = Logic Level Low, H = Logic Level High, X = Don't Care
 = Transition from Low to High Level

Q0 = The level of Q before the indicated input conditions were established.

* This configuration is non-stable, that is, it will not persist when set and reset inputs return to their inactive (High) level.

Absolute Maximum Ratings

| | |
|---|--------------------|
| Supply Voltage (VCC) | -0.5V to +7.0V |
| Input Voltage Range, All Inputs | -0.5V to VCC +0.5V |
| DC Input Current, Any One Input | ±10mA |
| DC Drain Current, Any One Output (All Voltage Reference to the VSS Terminal) | ±25mA |
| Storage Temperature Range (TSTG) | -65°C to +150°C |
| Lead Temperature (Soldering 10sec) | +265°C |
| Junction Temperature (TJ) | +175°C |
| ESD Classification | Class 1 |

Reliability Information

| | | |
|--|---------------|---------------|
| Thermal Resistance | θ_{JA} | θ_{JC} |
| SBDIP Package | 74°C/W | 24°C/W |
| Ceramic Flatpack Package | 116°C/W | 30°C/W |
| Maximum Package Power Dissipation at +125°C Ambient | | |
| SBDIP Package | 0.68W | |
| Ceramic Flatpack Package | 0.43W | |
| If device power exceeds package dissipation capability, provide heat sinking or derate linearly at the following rate: | | |
| SBDIP Package | 13.5mW/°C | |
| Ceramic Flatpack Package | 8.6mW/°C | |

CAUTION: As with all semiconductors, stress listed under "Absolute Maximum Ratings" may be applied to devices (one at a time) without resulting in permanent damage. This is a stress rating only. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. The conditions listed under "Electrical Performance Characteristics" are the only conditions recommended for satisfactory device operation.

Operating Conditions

| | | | |
|--|-----------------|--------------------------|--------------|
| Supply Voltage (VCC) | +4.5V to +5.5V | Input Low Voltage (VIL) | 0.0V to 0.8V |
| Operating Temperature Range (T _A) | -55°C to +125°C | Input High Voltage (VIH) | VCC/2 to VCC |
| Input Rise and Fall Times at VCC = 4.5V (TR, TF) | 100ns/V Max. | | |

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

| PARAMETER | SYMBOL | (NOTE 1) CONDITIONS | GROUP A SUB- GROUPS | TEMPERATURE | LIMITS | | UNITS |
|-----------------------------------|--------|---|---------------------------|----------------------|-------------|------|-------|
| | | | | | MIN | MAX | |
| Quiescent Current | ICC | VCC = 5.5V, VIN = VCC or GND | 1 | +25°C | - | 20 | μA |
| | | | 2, 3 | +125°C, -55°C | - | 400 | μA |
| Output Current (Sink) | IOL | VCC = 4.5V, VIH = 4.5V, VOUT = 0.4V, VIL = 0V | 1 | +25°C | 4.8 | - | mA |
| | | | 2, 3 | +125°C, -55°C | 4.0 | - | mA |
| Output Current (Source) | IOH | VCC = 4.5V, VIH = 4.5V, VOUT = VCC - 0.4V, VIL = 0V | 1 | +25°C | -4.8 | - | mA |
| | | | 2, 3 | +125°C, -55°C | -4.0 | - | mA |
| Output Voltage Low | VOL | VCC = 4.5V, VIH = 2.25V, IOL = 50μA, VIL = 0.8V | 1, 2, 3 | +25°C, +125°C, -55°C | - | 0.1 | V |
| | | VCC = 5.5V, VIH = 2.75V, IOL = 50μA, VIL = 0.8V | 1, 2, 3 | +25°C, +125°C, -55°C | - | 0.1 | V |
| Output Voltage High | VOH | VCC = 4.5V, VIH = 2.25V, IOH = -50μA, VIL = 0.8V | 1, 2, 3 | +25°C, +125°C, -55°C | VCC -0.1 | - | V |
| | | VCC = 5.5V, VIH = 2.75V, IOH = -50μA, VIL = 0.8V | 1, 2, 3 | +25°C, +125°C, -55°C | VCC -0.1 | - | V |
| Input Leakage Current | IIN | VCC = 5.5V, VIN = VCC or GND | 1 | +25°C | - | ±0.5 | μA |
| | | | 2, 3 | +125°C, -55°C | - | ±5.0 | μA |
| Noise Immunity Functional Test | FN | VCC = 4.5V, VIH = 2.25V, VIL = 0.8V (Note 2) | 7, 8A, 8B | +25°C, +125°C, -55°C | - | - | - |

NOTES:

- All voltages reference to device GND.
- For functional tests VO ≥ 4.0V is recognized as a logic "1", and VO ≤ 0.5V is recognized as a logic "0".
- Force/Measure functions may be interchanged.

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

| PARAMETER | SYMBOL | (NOTES 1, 2) CONDITIONS | GROUP A SUB- GROUPS | TEMPERATURE | LIMITS | | UNITS |
|------------------------|--------|----------------------------|---------------------------|---------------|--------|-----|-------|
| | | | | | MIN | MAX | |
| CP to Q, \bar{Q} | TPHL | VCC = 4.5V | 9 | +25°C | 2 | 31 | ns |
| | | | 10, 11 | +125°C, -55°C | 2 | 37 | ns |
| | TPLH | VCC = 4.5V | 9 | +25°C | 2 | 27 | ns |
| | | | 10, 11 | +125°C, -55°C | 2 | 31 | ns |
| \bar{S} to Q | TPLH | VCC = 4.5V | 9 | +25°C | 2 | 21 | ns |
| | | | 10, 11 | +125°C, -55°C | 2 | 24 | ns |
| \bar{S} to \bar{Q} | TPHL | VCC = 4.5V | 9 | +25°C | 2 | 33 | ns |
| | | | 10, 11 | +125°C, -55°C | 2 | 38 | ns |
| R to Q | TPHL | VCC = 4.5V | 9 | +25°C | 2 | 35 | ns |
| | | | 10, 11 | +125°C, -55°C | 2 | 40 | ns |
| R to \bar{Q} | TPLH | VCC = 4.5V | 9 | +25°C | 2 | 29 | ns |
| | | | 10, 11 | +125°C, -55°C | 2 | 34 | ns |

NOTES:

1. All voltages referenced to device GND.
2. AC measurements assume $R_L = 500\Omega$, $C_L = 50\text{pF}$, Input $T_R = T_F = 3\text{ns}$, $V_{IL} = \text{GND}$, $V_{IH} = 3\text{V}$.

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

| PARAMETER | SYMBOL | CONDITIONS | NOTES | TEMPERATURE | LIMITS | | UNITS |
|------------------------------------|--------------|----------------------|-------|---------------|--------|-----|-------|
| | | | | | MIN | MAX | |
| Capacitance Power Dissipation | CPD | VCC = 5.0V, f = 1MHz | 1 | +25°C | - | 53 | pF |
| | | | 1 | +125°C, -55°C | - | 55 | pF |
| Input Capacitance | CIN | VCC = Open, f = 1MHz | 1 | +25°C | - | 10 | pF |
| | | | 1 | +125°C, -55°C | - | 10 | pF |
| Output Transition Time | TTHL TTLH | VCC = 4.5V | 1 | +25°C | - | 15 | ns |
| | | | 1 | +125°C, -55°C | - | 22 | ns |
| Max Operating Frequency | FMAX | VCC = 4.5V | 1 | +25°C | - | 25 | MHz |
| | | | 1 | +125°C, -55°C | - | 16 | MHz |
| Data to CP Set-up Time | TSU | VCC = 4.5V | 1 | +25°C | 11 | - | ns |
| | | | 1 | +125°C, -55°C | 12 | - | ns |
| Hold Time | TH | VCC = 4.5V | 1 | +25°C | 3 | - | ns |
| | | | 1 | +125°C, -55°C | 3 | - | ns |
| Removal Time R, \bar{S} to CP | TREM | VCC = 4.5V | 1 | +25°C | 5 | - | ns |
| | | | 1 | +125°C, -55°C | 6 | - | ns |
| Pulse Width \bar{R} , \bar{S} | TW | VCC = 4.5V | 1 | +25°C | 14 | - | ns |
| | | | 1 | +125°C, -55°C | 16 | - | ns |
| Pulse Width CP | TW | VCC = 4.5V | 1 | +25°C | 14 | - | ns |
| | | | 1 | +125°C, -55°C | 16 | - | ns |

NOTE:

1. The parameters listed in Table 3 are controlled via design or process parameters. Min and Max Limits are guaranteed but not directly tested. These parameters are characterized upon initial design release and upon design changes which affect these characteristics.

TABLE 4. DC POST RADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS

| PARAMETERS | SYMBOL | (NOTES 1, 2) CONDITIONS | TEMPERATURE | 200K RAD LIMITS | | UNITS |
|--------------------------------|--------|--|-------------|--------------------|-----|-------|
| | | | | MIN | MAX | |
| Quiescent Current | ICC | VCC = 5.5V, VIN = VCC or GND | +25°C | - | 0.4 | mA |
| Output Current (Sink) | IOL | VCC = 4.5V, VIN = VCC or GND, VOUT = 0.4V | +25°C | 4.0 | - | mA |
| Output Current (Source) | IOH | VCC = 4.5V, VIN = VCC or GND, VOUT = VCC - 0.4V | +25°C | -4.0 | - | mA |
| Output Voltage Low | VOL | VCC = 4.5V and 5.5V, VIH = VCC/2, VIL = 0.8V, IOL = 50µA | +25°C | - | 0.1 | V |
| Output Voltage High | VOH | VCC = 4.5V and 5.5V, VIH = VCC/2, VIL = 0.8V, IOH = -50µA | +25°C | VCC -0.1 | - | V |
| Input Leakage Current | IIN | VCC = 5.5V, VIN = VCC or GND | +25°C | - | ±5 | µA |
| Noise Immunity Functional Test | FN | VCC = 4.5V, VIH = 2.25V, VIL = 0.8V, (Note 3) | +25°C | - | - | - |
| CP to Q, \bar{Q} | TPHL | VCC = 4.5V | +25°C | 2 | 37 | ns |
| | TPLH | VCC = 4.5V | +25°C | 2 | 31 | ns |
| \bar{S} to Q | TPLH | VCC = 4.5V | +25°C | 2 | 24 | ns |
| \bar{S} to \bar{Q} | TPHL | VCC = 4.5V | +25°C | 2 | 38 | ns |
| \bar{R} to Q | TPHL | VCC = 4.5V | +25°C | 2 | 40 | ns |
| \bar{R} to \bar{Q} | TPLH | VCC = 4.5V | +25°C | 2 | 34 | ns |

NOTES:

- All voltages referenced to device GND.
- AC measurements assume $R_L = 500\Omega$, $C_L = 50\text{pF}$, Input $T_R = T_F = 3\text{ns}$, $V_{IL} = \text{GND}$, $V_{IH} = 3\text{V}$.
- For functional tests $V_O \geq 4.0\text{V}$ is recognized as a logic "1", and $V_O \leq 0.5\text{V}$ is recognized as a logic "0".

TABLE 5. BURN-IN AND OPERATING LIFE TEST, DELTA PARAMETERS (+25°C)

| PARAMETER | GROUP B SUBGROUP | DELTA LIMIT |
|-----------|---------------------|----------------|
| ICC | 5 | 6µA |
| IOL/IOH | 5 | -15% of 0 Hour |

TABLE 6. APPLICABLE SUBGROUPS

| CONFORMANCE GROUPS | METHOD | GROUP A SUBGROUPS | READ AND RECORD |
|--------------------------------|-----------|-------------------|-----------------|
| Initial Test (Preburn-In) | 100%/5004 | 1, 7, 9 | ICC, IOL/H |
| Interim Test I (Postburn-In) | 100%/5004 | 1, 7, 9 | ICC, IOL/H |
| Interim Test II (Postburn-In) | 100%/5004 | 1, 7, 9 | ICC, IOL/H |
| PDA | 100%/5004 | 1, 7, 9, Deltas | |
| Interim Test III (Postburn-In) | 100%/5004 | 1, 7, 9 | ICC, IOL/H |

TABLE 6. APPLICABLE SUBGROUPS (Continued)

| CONFORMANCE GROUPS | | METHOD | GROUP A SUBGROUPS | READ AND RECORD |
|--------------------|--------------|-------------|---------------------------------------|--|
| PDA | | 100%/5004 | 1, 7, 9, Deltas | |
| Final Test | | 100%/5004 | 2, 3, 8A, 8B, 10, 11 | |
| Group A (Note 1) | | Sample/5005 | 1, 2, 3, 7, 8A, 8B, 9, 10, 11 | |
| Group B | Subgroup B-5 | Sample/5005 | 1, 2, 3, 7, 8A, 8B, 9, 10, 11, Deltas | Subgroups 1, 2, 3, 9, 10, 11, (Note 2) |
| | Subgroup B-6 | Sample/5005 | 1, 7, 9 | |
| Group D | | Sample/5005 | 1, 7, 9 | |

NOTES:

1. Alternate Group A testing in accordance with method 5005 of MIL-STD-883 may be exercised.
2. Table 5 parameters only.

TABLE 7. TOTAL DOSE IRRADIATION

| CONFORMANCE GROUPS | METHOD | TEST | | READ AND RECORD | |
|--------------------|--------|---------|----------|-----------------|-----------------|
| | | PRE RAD | POST RAD | PRE RAD | POST RAD |
| Group E Subgroup 2 | 5005 | 1, 7, 9 | Table 4 | 1, 9 | Table 4 (Note1) |

NOTE:

1. Except FN test which will be performed 100% Go/No-Go.

TABLE 8. STATIC AND DYNAMIC BURN-IN TEST CONNECTIONS

| OPEN | GROUND | 1/2 VCC = 3V ± 0.5V | VCC = 6V ± 0.5V | OSCILLATOR | |
|------------------------------------|-------------------------------|---------------------|--------------------------------|------------|-------|
| | | | | 50kHz | 25kHz |
| STATIC BURN-IN I TEST CONNECTIONS | | | | | |
| 5, 6, 8, 9 | 1, 2, 3, 4, 7, 10, 11, 12, 13 | | 14 | | |
| STATIC BURN-IN II TEST CONNECTIONS | | | | | |
| 5, 6, 8, 9 | 7 | | 1, 2, 3, 4, 10, 11, 12, 13, 14 | | |
| DYNAMIC BURN-IN TEST CONNECTIONS | | | | | |
| - | 7 | 5, 6, 8, 9 | 1, 4, 10, 13, 14 | 3, 11 | 2, 12 |

NOTES:

1. Each pin except VCC and GND will have a resistor of 10KΩ ± 5% for static burn-in.
2. Each pin except VCC and GND will have a resistor of 1KΩ ± 5% for dynamic burn-in.

TABLE 9. IRRADIATION TEST CONNECTIONS

| OPEN | GROUND | VCC = 5V ± 0.5V |
|------------|--------|--------------------------------|
| 5, 6, 8, 9 | 7 | 1, 2, 3, 4, 10, 11, 12, 13, 14 |

NOTE: Each pin except VCC and GND will have a resistor of 47KΩ ± 5% for irradiation testing. Group E, Subgroup 2, sample size is 4 dice/wafer 0 failures.

Intersil Space Level Product Flow - 'MS'

| | |
|--|--|
| Wafer Lot Acceptance (All Lots) Method 5007 (Includes SEM) | 100% Interim Electrical Test 1 (T1) |
| GAMMA Radiation Verification (Each Wafer) Method 1019, 4 Samples/Wafer, 0 Rejects | 100% Delta Calculation (T0-T1) |
| 100% Nondestructive Bond Pull, Method 2023 | 100% Static Burn-In 2, Condition A or B, 24 hrs. min., +125°C min., Method 1015 |
| Sample - Wire Bond Pull Monitor, Method 2011 | 100% Interim Electrical Test 2 (T2) |
| Sample - Die Shear Monitor, Method 2019 or 2027 | 100% Delta Calculation (T0-T2) |
| 100% Internal Visual Inspection, Method 2010, Condition A | 100% PDA 1, Method 5004 (Notes 1 and 2) |
| 100% Temperature Cycle, Method 1010, Condition C, 10 Cycles | 100% Dynamic Burn-In, Condition D, 240 hrs., +125°C or Equivalent, Method 1015 |
| 100% Constant Acceleration, Method 2001, Condition per Method 5004 | 100% Interim Electrical Test 3 (T3) |
| 100% PIND, Method 2020, Condition A | 100% Delta Calculation (T0-T3) |
| 100% External Visual | 100% PDA 2, Method 5004 (Note 2) |
| 100% Serialization | 100% Final Electrical Test |
| 100% Initial Electrical Test (T0) | 100% Fine/Gross Leak, Method 1014 |
| 100% Static Burn-In 1, Condition A or B, 24 hrs. min., +125°C min., Method 1015 | 100% Radiographic, Method 2012 (Note 3) |
| | 100% External Visual, Method 2009 |
| | Sample - Group A, Method 5005 (Note 4) |
| | 100% Data Package Generation (Note 5) |

NOTES:

- Failures from Interim electrical test 1 and 2 are combined for determining PDA 1.
- Failures from subgroup 1, 7, 9 and deltas are used for calculating PDA. The maximum allowable PDA = 5% with no more than 3% of the failures from subgroup 7.
- Radiographic (X-Ray) inspection may be performed at any point after serialization as allowed by Method 5004.
- Alternate Group A testing may be performed as allowed by MIL-STD-883, Method 5005.
- Data Package Contents:
 - Cover Sheet (Intersil Name and/or Logo, P.O. Number, Customer Part Number, Lot Date Code, Intersil Part Number, Lot Number, Quantity).
 - Wafer Lot Acceptance Report (Method 5007). Includes reproductions of SEM photos with percent of step coverage.
 - GAMMA Radiation Report. Contains Cover page, disposition, Rad Dose, Lot Number, Test Package used, Specification Numbers, Test equipment, etc. Radiation Read and Record data on file at Intersil.
 - X-Ray report and film. Includes penetrometer measurements.
 - Screening, Electrical, and Group A attributes (Screening attributes begin after package seal).
 - Lot Serial Number Sheet (Good units serial number and lot number).
 - Variables Data (All Delta operations). Data is identified by serial number. Data header includes lot number and date of test.
 - The Certificate of Conformance is a part of the shipping invoice and is not part of the Data Book. The Certificate of Conformance is signed by an authorized Quality Representative.

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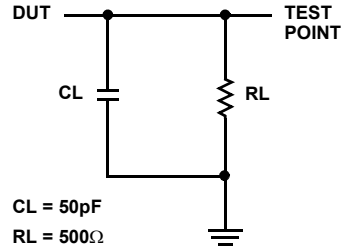
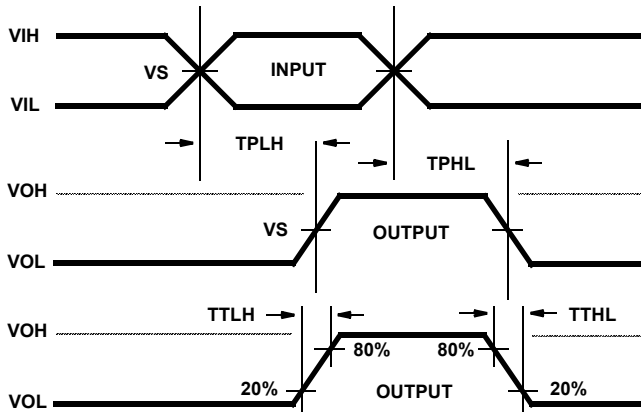
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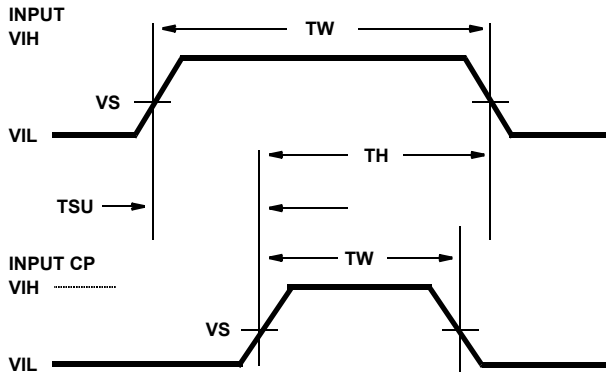
AC Timing Diagrams and Load Circuit



AC VOLTAGE LEVELS

| PARAMETER | HCTS | UNITS |
|-----------|------|-------|
| VCC | 4.50 | V |
| VIH | 3.00 | V |
| VS | 1.30 | V |
| VIL | 0 | V |
| GND | 0 | V |

Pulse Width, Setup, Hold Timing Diagram Positive Edge Trigger



VOLTAGE LEVELS

| PARAMETER | HCTS | UNITS |
|-----------|------|-------|
| VCC | 4.50 | V |
| VIH | 3.00 | V |
| VS | 1.30 | V |
| VIL | 0 | V |
| GND | 0 | V |

TH = HOLD TIME
 TSU = SETUP TIME
 TW = PULSE WIDTH

Die Characteristics

DIE DIMENSIONS:

89 x 88 mils
2.25 x 2.24mm

METALLIZATION:

Type: SiAl
Metal Thickness: $11\text{k}\text{\AA} \pm 1\text{k}\text{\AA}$

GLASSIVATION:

Type: SiO_2
Thickness: $13\text{k}\text{\AA} \pm 2.6\text{k}\text{\AA}$

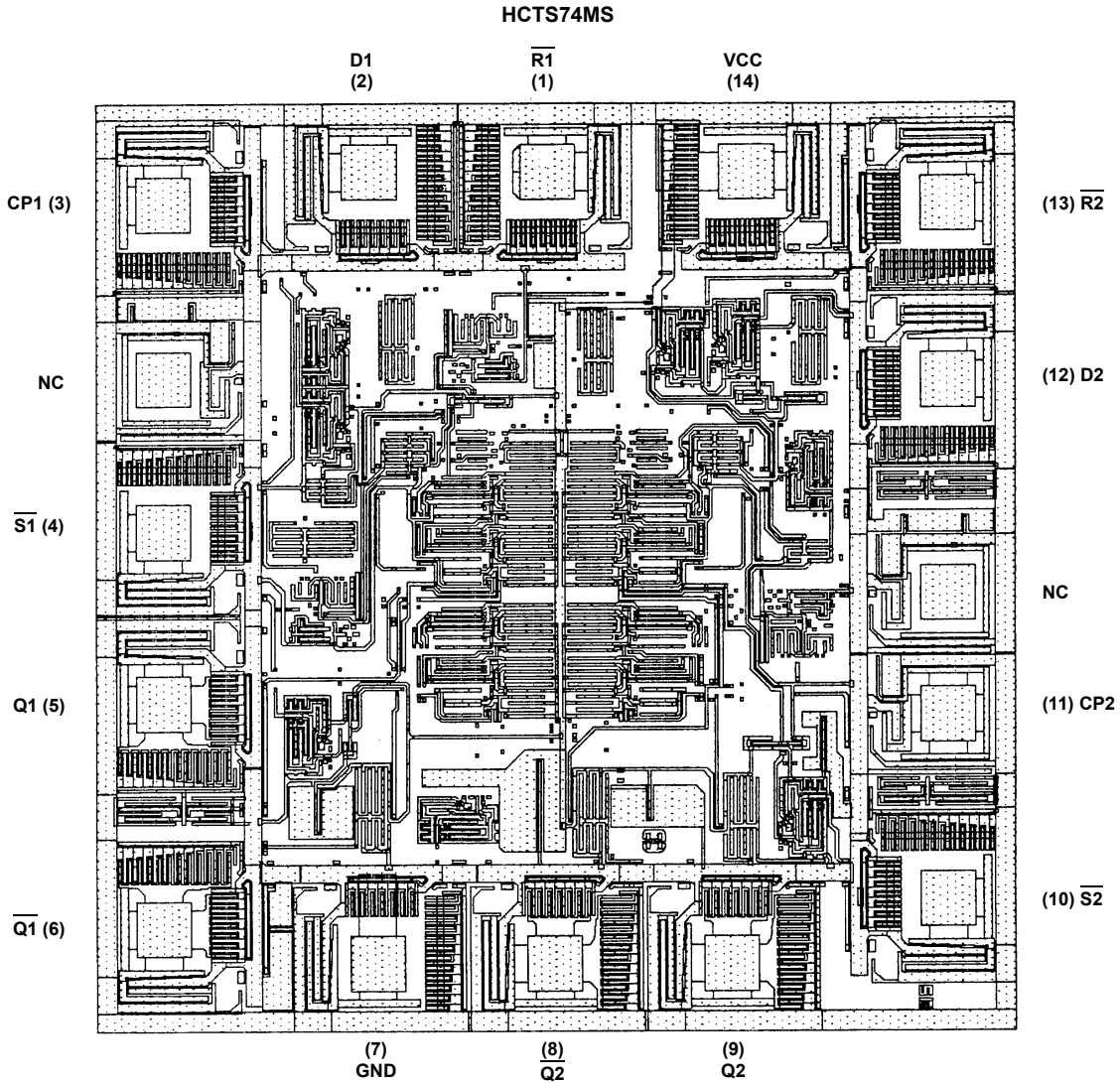
WORST CASE CURRENT DENSITY:

$<2.0 \times 10^5 \text{A/cm}^2$

BOND PAD SIZE:

$100\mu\text{m} \times 100\mu\text{m}$
4 mils x 4 mils

Metallization Mask Layout



NOTE: The die diagram is a generic plot from a similar HCS device. It is intended to indicate approximate die size and bond pad location. The mask series for the HCTS74 is TA14438A.