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瑞萨电子公司网址：<http://www.renesas.com>

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瑞萨电子公司

【发行】瑞萨电子公司（<http://www.renesas.com>）

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中断嵌套

Trouble

用户反映，基于 Renesas M16C 内核的 MCU 中断不能嵌套

Analyze

检查程序，发现用户在进行中断声明时，没有正确的声明。

Do

以下说明关于在接受中断请求后到执行中断程序为止的中断顺序：

中断顺序运行如下。。

- (1) 通过读地址00000h， CPU 获得中断信息（中断序号、中断请求级）。此后，该中断的IR 位变为“0”（无中断请求）。
- (2) 将中断顺序前的FLG 寄存器保存到CPU 内部的暂存器（注1）。
- (3) FLG 寄存器中的I 标志、D 标志、U 标志变为：
I 标志为“0”（禁止中断）
D 标志为“0”（禁止单步中断）
U 标志为“0”（指定ISP）
但是，在执行软件中断序号32 ~ 63 的INT 指令时， U 标志不变。
- (4) 将CPU 内部的暂存器（注1）压栈。
- (5) 将PC 压栈。
- (6) 给IPL 设定接受中断的中断优先级。
- (7) 中断向量所设定的中断程PC。序的起始地址存入
在中断顺序结束后，从中断程序的起始地址执行指令。

从上面的表述可以看出：

因为FLG 寄存器中的I 标志是允许或者禁止可屏蔽中断的标志，在中断响应后，I 标志为“0”（禁止中断），所以中断不能嵌套。

处理方法如下：

在#pragma INTERRUPT 后加上/E 参数，C 编译器将自动生成允许其它中断的代码。



Trouble Shoot Document

RTSHCMCAN0006-0100 Rev.1.00

MCU

文档适用于 Renesas M16C 内核的 MCU