

AN-1069 12V/5V Power Mux Author: Ramzy Ammar Date: May 18, 2015

#### Introduction

Mobile devices are the dominant gadgets in our routine lives. Continuous use therefore requires regular charging from various power sources: batteries when on the go, power outlets when at home or the office, and USB when in vehicles. Power switching has become an important factor for mobile devices. GreenPAK (Programmable Mixed Signal) and GreenFET (Integrated Power Switch) provide a simple, cost-effective solution for switching between supplies; they occupy the smallest area and can be programmed in seconds. Signals are super clean and have features like ramp rate control, multiple protection circuitries, and smallest packages available. Due to the demand for such an application, the company introduced a simple design block that senses, sets priority, and switches power lines in the cleanest possible way (noiseless and smooth transition) using GPAK and GFET in combination with generic MOSFETs that supply different power rails. In the following application, we will be using 12V (VPWR1) and 5V (VPWR2) rails to illustrate the circuit behavior. Test data will be generated using the company's validation module which can be imported into any design block once it is verified to work for the specific application. See Figure 1 for the validation module schematics.



Figure 1. Power Mux validation module schematic





Figure 2. SLG7NT4111V Functionality

## **Device detail and functionalities**

There are three devices that are used in the module design:

GPAK (SLG7NT4111V)

GFET (SLG55021V)

Generic MOSFET (IRFHM830 in this application)

#### GreenPAK (SLG7NT4111)

This device is user-configured and programmable, it senses when the MOSFET's are ON and decides which supply will have the priority to provide power to the IC board.

The following Power Mux example includes both a 12V and a 5V power Supply. The 12V power supply always has the priority over the 5V power supply. When the 12V power supply is not present, the 5V power supply provides power to the IC board.

Once the 12V power supply is available, the 5V MOSFET will be turned OFF and the 12V MOSFET will be turned ON. There will be a 50ms delay when switching between supplies. See table below for clarification.

|           | Switching to   |              |               |                |  |  |  |
|-----------|----------------|--------------|---------------|----------------|--|--|--|
| Switching |                | No<br>Supply | VPWR2<br>(5V) | VPWR1<br>(12V) |  |  |  |
| From      | No<br>Supply   |              | No<br>Delay   | No<br>Delay    |  |  |  |
|           | VPWR2<br>(5V)  | No<br>Delay  |               | 50ms<br>Delay  |  |  |  |
|           | VPWR1<br>(12V) | No<br>Delay  | 50ms<br>Delay |                |  |  |  |

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Table 1. SLG7NT4111V Switching delay between supplies
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## Input and Output Signals:

The following describes the input and output functionality of the GreenPAK device:

## GreenFET (SLG55021)

This device is a high voltage gate driver used to turn the MOSFET gate ON and OFF. It incorporates many features that are required for a robust design:



#### Figure 3. SLG7NT4111V Pinout

Pin2, CHG\_DET, this input signal detects the change at the Drain of the MOSFET, then sets the priority and switches the supply.

Pin3, VPWR1\_SENSE, this input coupled with CHG\_DET and VPWR2\_SENSE decide on which MOSFET is to be turned on.

Pin4, VPWR2\_SENSE, this input coupled with CHG\_DET and VPWR1\_SENSE decide on which MOSFET is to be turned on.

Pin5/6/8, PG\_VPWR2, PG\_VPWR1 and VOUT\_VPWR1/VPWR2\_SENSE, these signals detect Power Good and make sure the MOSFET output is available by sending a high signal to Pin9 (PWR\_GOOD) output.

Pin10/11,VPWR2\_FET\_DRIVE\_ONandVPWR1\_FET\_DRIVE\_ON outputs are used to turneither MOSFET gate ON based on priority

Pin12, VPWR1\_PRESENT, this output indicates the presence of VPWR1.

- Drain Voltage Range 1.0V to 20V
- Internal Gate Voltage Charge Pump
- Controlled Turn on Delay
- Controlled Load Discharge Rate
- Controlled Turn on Slew Rate
- Stable Slew Rate (±2% typ) over Temperature Range
- TDFN-8 Package

See below Figure 4 for device schematics.





Figure 4. SLG55021V Schematic



Figure 5. SLG55021V Reverse current blocking schematic

#### **Generic MOSFET**

The Power Mux uses four MOSFET devices connected back to back via their source to create a reverse current blocking environment. This feature is required during normal operation. If VPWR1 rail MOSFET is ON and the VPWR2 rail MOSFET is OFF or when one is at higher potential then the other, then there will be a current flow back to the lower potential power supply causing undesirable behavior and current waste. This is why a reverse current block is required to prevent this condition from occurring. See Figure 5 for illustration.

#### Module design

Since this circuitry is widely used in current designs, a validation module was built as a proof of concept and to emulate the power muxing application under different conditions. This module provides the designer a fast tool to validate their design in a timely manner by connecting it to their board to verify functionality before importing the design block. Figure 6 shows the populated module with pin connections as well as the added LEDs for monitoring the module functionality.



Figure 6. Power Mux module showing pin connections



## **Module Testing and Verification**

The following are the test results of the Power Mux using two external power supplies.

Test conditions as follows:

VPWR1 = 12V, VPWR2 = 5V

VDD = 5V (SLG7NT4111V, SLG55021V)

Output Loading: 10Ω, 10uF

Waveforms were captured using the conditions listed in Table 1 above.



# Condition#1: VPWR1 (12V) = Ramping Up, VPWR2 (5V) = 0V

Figure 7 shows the output (VOUT\_VPWR1/VPWR2) starts to ramp up as soon as the gate control signal (VPWR1\_FET\_DRIVE\_ON, Pin11) switches high.





Figure 7. PowerMux Output Waveform for Condition#1



# Condition#2: VPWR1 (12V) = Ramping Down, VPWR2 (5V) = 0V

Figure 8 shows the output (VOUT\_VPWR1/VPWR2) starts to ramp down as soon as the gate control signal (VPWR1\_FET\_DRIVE\_ON, Pin11) switches low.



Figure 8. PowerMux Output Waveform for Condition#2



## Condition#3: VPWR1 (12V) = 0V, VPWR2 (5V) = Ramping Up

Figure 9 shows the output (VOUT\_VPWR1/VPWR2) starts to ramp up as soon as the gate control signal (VPWR2\_FET\_DRIVE\_ON, Pin10) switches high.



Figure 9. PowerMux Output Waveform for Condition#3





## Condition#4: VPWR1 (12V) = 0V, VPWR2 (5V) = Ramping Down

Figure 10 shows the output (VOUT\_VPWR1/ VPWR2) starts to ramp down as soon as the gate control signal (VPWR2\_FET\_DRIVE\_ON, Pin10) switches low.









# Condition#5: VPWR1 (12V) = Ramping Up, VPWR2 (5V) = 5V

Figure 11 shows, as soon as the 12V Power Supply is detected, the output (VOUT\_VPWR1/VPWR2) starts switching from 5V to 0V, remains at 0V for 50ms (Break before Make), then, the gate control signal (VPWR1\_FET\_DRIVE\_ON, Pin11) switches high and the output starts ramping up to 12V regardless of the 5V Power Supply being up.





Figure 11. Power Mux output waveform for condition#5



## Condition#6: VPWR1 (12V) = Ramping Down, VPWR2 (5V) = 5V

Figure 12 shows, as soon as the 12V Power Supply is lost, the gate control signal (VPWR1\_FET\_DRIVE\_ON, Pin11) switches low and the output (VOUT\_VPWR1/VPWR2) starts switching from 12V to 0V, remains at 0V for 50ms (break before make), then, starts ramping back up to 5V.

|      | L            | .oa                      | d:                     | 100                     | Ω&                                      | 10µl                                    | F            |                      |                  |      |        |         |
|------|--------------|--------------------------|------------------------|-------------------------|---|---|--------------|----------------------|------------------|------|--------|---------|
|      | B<br>Y<br>Te | lue =<br>ellow<br>est: 5 | 12V<br>v = V(<br>v = 0 | _Fet_<br>OUT_1<br>N, 12 | Drive<br>12V/5V<br>V=Turr               | _ON (P<br>/<br>ning Of                  | ?in11)<br>FF |                      |                  |      |        |         |
| RIG  | DL           | ST                       | 0P                     |                         | <b>F</b> ~~~~                           | ~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~ |              | <u>~</u> ~~~         | ~~~~             | 12   | 2      | 160mU   |
|      |              |                          |                        |                         |   |   |              |                      |                  |      |        |         |
|      |              |                          |                        |                         | *****                                   |   |              |                      |                  |      |        |         |
|      |              |                          |                        |                         |   |   |              |                      |                  |      |        |         |
|      |              |                          |                        |                         |   |   |              |                      |                  |      |        |         |
|      |              |                          |                        |                         |   |   |              |                      |                  |      | م<br>م |         |
| T    |              |                          |                        |                         |   |   |              |                      |                  |      | 1      |         |
|      |              |                          |                        |                         |   |   |              |                      |                  |      |        |         |
| •    |              |                          |                        |                         |   |   | -            |                      |                  |      | , l.,. |         |
| CH 1 |              | 2.0                      | ดบเ                    | 8                       | - 12 - 14 - 14 - 14 - 14 - 14 - 14 - 14 | 2.000                                   |              | Time                 | 10.              | 90ms |        | - ABBWS |
| CITI | _            | 2.0                      |                        | Sca                     | ale:                                    | <mark>2V/I</mark>                       | Div          | <mark>&amp; 1</mark> | <mark>l0m</mark> | s/D  | iv     | .0000   |
|      |              |                          |                        |                         |   |   |              |                      |                  |      |        |         |



Figure 12. Power Mux output waveform for Condition#6



# Condition#7&8: VPWR1 (12V) = 12V, VPWR2 (5V) = Ramping Up and Down

Load: 10Ω &10µF

Figure 13 &14 show, when the 12V power supply is available, regardless of the 5V power supply availability (Blue plot= 5V power supply drain waveform), the output (VOUT\_VPWR1/VPWR2) remains at 12V.



Figure 13. Power Mux output waveform for condition#7



Figure 14. Power Mux output waveform for Condition#8

# RENESAS

## Conclusion

Dialog has been offering low cost products with state of the art enhancement features that help designers facilitate and ease their design challenges and space requirements. The following products are widely used. They are production-ready or can be designed and programmed in minutes:

**GreenPAK:** NVM programmable mixed-signal ASICs is useful for integrating many discrete ICs and surrounding circuitry into a single device.

**GreenFET:** Integrated Load Switches that replace discrete FET and FET Switch Circuitry.

They include an integrated MOSFET, a charge pump, a ramp control circuitry, Low RDS(on), thermal shutdown protection with current limit and reverse current block option.

Our packaging offers: TDFN, 1.5x2.0mm, 1.0x1.6mm and 1.0x1.0mm - the smallest packages available.