[Notes]

Smart Configurator for RH850

R20TS0806EC0100 Rev.1.00 Feb. 01, 2022

Outline

When using Smart Configurator for RH850, note the following points.

- 1. Notes on using T&H path self-diagnosis function of A/D Converter
- 2. Notes on redundant macros and wrong comments in A/D Converter header file
- 1. Notes on using T&H path self-diagnosis function of A/D Converter

1.1 Applicable Products

Smart Configurator for RH850 V1.2.0 or later version

1.2 Applicable Devices

RH850 family: RH850/U2A group

- > RH850/U2A16 (516-pin product, 292-pin product)
- RH850/U2A8 (292-pin product)

1.3 Details

When using T&H path self-diagnosis function of A/D Converter (refer to Figure1-1) on the following peripherals, the function can't be enabled/disabled correctly even if the T&H path self-diagnosis function is already selected/unselected on GUI. The actual generated code is the opposite of the GUI setting.

- RH850/U2A16 (516-pin product, 292-pin product)
 ADCJ0, ADCJ1, ADCJ2
- > RH850/U2A8 (292-pin product)

ADCJ0, ADCJ1, ADCJ2

Advanced setting		
Safty-related setting T&H path self-diagnosis enable		
Pin-Level self-diagnosis level setting	Туре 3	~
Addition mode wiring-break detection en	able	
Wiring-break detection pulse width	1 state (of internal clock)	\sim
Trigger overlap check function enable		

Figure 1-1 T&H path self-diagnosis setting

1.4 Workaround

Manually modify the code in the following source file

- Source file: "r_cg_ad.h".
- Macro value: _ADC_TH_PATH_SELF_DIAGNOSIS_ENABLE,

_ADC_TH_PATH_SELF_DIAGNOSIS_DISABLE

Note: If code is generated again, the previous state will be restored. Modification is necessary each time after performing code generation.



This is an example of the required modification. Manually change the macro values in "r_cg_ad.h". In the following example, the code in red color is wrong code before modification, while the code in blue color is correct code after modification.

Before modification:

```
/*
   Pin level self-diagnostic control register (ADCJnTDCR)
 */
   /* T&H path self-diagnosis enable (THSDE) */
   #define _ADC_TH_PATH_SELF_DIAGNOSIS_ENABLE (0x00UL) /* T&H path self-
   diagnosis is enable */
   #define _ADC_TH_PATH_SELF_DIAGNOSIS_DISABLE (0x80UL) /* T&H path self-
   diagnosis is disabled */
   .....
```

After modification:

```
/*
   Pin level self-diagnostic control register (ADCJnTDCR)
 */
   /* T&H path self-diagnosis enable (THSDE) */
   #define _ADC_TH_PATH_SELF_DIAGNOSIS_ENABLE (0x80UL) /* T&H path self-
diagnosis is enable */
   #define _ADC_TH_PATH_SELF_DIAGNOSIS_DISABLE (0x00UL) /* T&H path self-
diagnosis is disabled */
   .....
```

1.5 Schedule for Fixing the Problem

This problem will be fixed in next version. (Scheduled to be released in Jul 2022.)



2. Notes on redundant macros and wrong comments in A/D Converter header file

2.1 Applicable Products

Smart Configurator for RH850 V1.2.0 and later version

2.2 Applicable Devices

RH850 family: RH850/U2A group

- RH850/U2A16 (516-pin product, 292-pin product)
- > RH850/U2A8 (292-pin product)

2.3 Details

When using A/D Converter on the following peripherals, there are mistakes in header file(r_cg_ad.h).

• Redundant macros: _ADC_VIRTUAL_CHANNEL_END_INT_DISABLE,

_ADC_VIRTUAL_CHANNEL_END_INT_ENABLE

• Wrong comments: comments of _ADC_VIRTUAL_END_INT_ENABLE,

_ADC_VIRTUAL_END_INT_ DISABLE

- RH850/U2A16 (516-pin product, 292-pin product)
 ADCJ0, ADCJ1, ADCJ2
- RH850/U2A8 (292-pin product)

ADCJ0, ADCJ1, ADCJ2

/*			
Virtual channel control register (ADCJnVCRj)			
*/			
/* A/D conversion end interrupt enable (ADIE) */			
#define _ADC_VIRTUAL_CHANNEL_END_INT_DISABLE	(0x0000000UL) /	<pre>/* not generated */</pre>	Redundant macros
#define _ADC_VIRTUAL_CHANNEL_END_INT_ENABLE	(0x00000100UL) /	/* generated */	Redundant macros
<pre>/* Upper limit/lower limit table select (VCULLMTB</pre>	S[3:0]) */		
<pre>#define _ADC_LIMIT_TABLE_SELECT_NONE</pre>	(0x0000000UL) /	/* Upper limit and lower	limit are not checked */
<pre>#define _ADC_LIMIT_TABLE_SELECT_0</pre>	(0x1000000UL) /	/* Upper limit and lower	limit are checked for VCULLMTBR0 */
<pre>#define _ADC_LIMIT_TABLE_SELECT_1</pre>	(0x20000000UL) /	/* Upper limit and lower	limit are checked for VCULLMTBR1 */
<pre>#define _ADC_LIMIT_TABLE_SELECT_2</pre>	(0x30000000UL) /	/* Upper limit and lower	limit are checked for VCULLMTBR2 */
<pre>#define _ADC_LIMIT_TABLE_SELECT_3</pre>	(0x40000000UL) /	/* Upper limit and lower	limit are checked for VCULLMTBR3 */
<pre>#define _ADC_LIMIT_TABLE_SELECT_4</pre>	(0x50000000UL) /	<pre>/* Upper limit and lower</pre>	limit are checked for VCULLMTBR4 */
<pre>#define _ADC_LIMIT_TABLE_SELECT_5</pre>	(0x6000000UL) /	/* Upper limit and lower	limit are checked for VCULLMTBR5 */
<pre>#define _ADC_LIMIT_TABLE_SELECT_6</pre>	(0x70000000UL) /	<pre>/* Upper limit and lower</pre>	limit are checked for VCULLMTBR6 */
<pre>#define _ADC_LIMIT_TABLE_SELECT_7</pre>	(UU00000008x0) /	/* Upper limit and lower	limit are checked for VCULLMTBR7 */
<pre>/* Wait time table select (WTTS[3:0]) */</pre>			
<pre>#define _ADC_WAIT_TIME_SELECT_NONE</pre>	(0x0000000UL) /	/* Wait time are not chec	ked */
<pre>#define _ADC_WAIT_TIME_TABLE_0</pre>	(0x01000000UL) /	/* Wait time are checked	for WAITTRO */
<pre>#define _ADC_WAIT_TIME_TABLE_1</pre>	(0x02000000UL) /	/* Wait time are checked	for WAITTR1 */
<pre>#define _ADC_WAIT_TIME_TABLE_2</pre>		/* Wait time are checked	
<pre>#define _ADC_WAIT_TIME_TABLE_3</pre>	(0x04000000UL) /	/* Wait time are checked	for WAITTR3 */
<pre>#define _ADC_WAIT_TIME_TABLE_4</pre>	(0x05000000UL) /	/* Wait time are checked	for WAITTR4 */
<pre>#define _ADC_WAIT_TIME_TABLE_5</pre>	(0x0600000UL) /	/* Wait time are checked	for WAITTR5 */
<pre>#define _ADC_WAIT_TIME_TABLE_6</pre>		/* Wait time are checked	
<pre>#define _ADC_WAIT_TIME_TABLE_7</pre>	(0x08000000UL) /	/* Wait time are checked	for WAITTR7 */
/* GTM entry enable (GTMENT) */			
<pre>#define _ADC_GTM_ENTRY_ENABLE</pre>	(0x00100000UL) /	/* GTM entry enable */	
<pre>#define _ADC_GTM_ENTRY_DISABLE</pre>	(0x0000000UL) /	/* GTM entry disabled */	
<pre>/* A/D conversion type (CNVCLS[3:0]) */</pre>			
#define _ADC_NORMAL		/* Normal A/D conversion	-
#define _ADC_HOLD_VALUE		/* Hold value A/D convers	
#define _ADC_EXTENDED_SAMPLING	(0x00001000UL) /	/* Normal A/D conversion	at extended sampling cycle */
#define _ADC_AD_CORE_DIAGNOSIS		/* ADcore self-diagnosis	
#define _ADC_ADDITION_MODE		/* Addition mode A/D conv	
#define _ADC_MPX_NORMAL		/* MPX normal A/D convers	
<pre>#define _ADC_MPX_ADDITION_MODE</pre>		/* MPX addition mode A/D	-
<pre>#define _ADC_PIN_LEVEL_DIAGNOSIS</pre>		/* Pin level self-diagnos	
<pre>#define _ADC_BREAK_MODE1</pre>			ng-break detection mode 1 */
<pre>#define _ADC_BREAK_MODE2_PULLDOWN</pre>			ng-break detection mode 2 (physical
<pre>#define _ADC_BREAK_MODE2_PULLUP</pre>			ng-break detection mode 2 (physical
<pre>#define _ADC_BREAK_MODE1_DIAGNOSIS</pre>	(UU0088000L) /	/* Self-diagnosis A/D con	version in wiring-break detection mo
<pre>#define _ADC_BREAK_MODE2_PULLDOWN_DIAGNOSIS</pre>	(0x00009000) \A	Irona commonte: thor	se 2 comments are reversed.
<pre>#define _ADC_BREAK_MODE2_PULLUP_DIAGNOSIS</pre>	(0x00009800 VV	nong comments. the	
<pre>#define _ADC_DATA_PATH_DIAGNOSIS</pre>	(0x0000A000),	mp conversion of mp	conterceron anon paon aragnooro (moti
/* Virtual channel end interrupt enable (ADIE) */			
<pre>#define _ADC_VIRTUAL_END_INT_ENABLE</pre>			at the end of virtual channel */
<pre>#define _ADC_VIRTUAL_END_INT_DISABLE</pre>	(UX0000000UL) /	/* INT_ADx is output at t	he end of virtual channel */

Figure 2-1 mistakes in header file



2.4 Workaround

The mistakes do not have effect on A/D Converter operation, please ignore and do not use the redundant macros. For wrong comments, please take care that the meanings are reversed.

2.5 Schedule for Fixing the Problem

This problem will be fixed in next version. (Scheduled to be released in Jul 2022.)



Revision History

		Description		
Rev.	Date	Page	Summary	
1.00	Feb.01.22	-	First edition issued	

Renesas Electronics has used reasonable care in preparing the information included in this document, but Renesas Electronics does not warrant that such information is error free. Renesas Electronics assumes no liability whatsoever for any damages incurred by you resulting from errors in or omissions from the information included herein.

The past news contents have been based on information at the time of publication. Now changed or invalid information may be included.

The URLs in the Tool News also may be subject to change or become invalid without prior notice.

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu, Koto-ku, Tokyo 135-0061, Japan

www.renesas.com

Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.

Contact information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit: www.renesas.com/contact/

© 2022 Renesas Electronics Corporation. All rights reserved. TS Colophon 4.3

