Old Company Name in Catalogs and Other Documents

On April 1st, 2010, NEC Electronics Corporation merged with Renesas Technology Corporation, and Renesas Electronics Corporation took over all the business of both companies. Therefore, although the old company name remains in this document, it is a valid Renesas Electronics document. We appreciate your understanding.

Renesas Electronics website: http://www.renesas.com

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Send any inquiries to http://www.renesas.com/inquiry.



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RENESAS TECHNICAL UPD

Nippon Bldg., 2-6-2, Ohte-machi, Chiyoda-ku, Tokyo 100-0004, Japan Renesas Technology Corp.

Product Category	User Development Environment		Document No.	TN-EML-A124A/E	Rev.	1.0
Title	Limitation due to a conflict between the refresh controller and break interrupts		Information Category	Technical Notification		
Applicable Product	H8S/2378F E10A Emulator (V 1.01) (HS2378KCM01H or HS2378KCI01H) H8S/2170F E10A Emulator (V 1.00) (HS2170KCM01H or HS2170KCI01H) E10A-USB Emulator (V 1.3.00) (HS0005KCU01H or HS0005KCU02H)	Lot No. See the applicable products	Reference Document	H8S/2378, H8S/2378R Group Hardware Manual (REJ09B0109-0400O Rev.4.00) H8S/2172 Group Hardware Manual (REJ09B0149-0200Z Rev.2.00)		

If you use an E10A or E10A-USB emulator with the H8S/2377R SDRAM interface or the H8S/2172F DRAM interface, the limitation on refresh control will be applied. Please read this document carefully before use.

[Problem]

While using the H8S/2377R SDRAM interface or the H8S/2172F DRAM interface, the program counter (PC) will be located at an incorrect address if you stop the program execution or perform stepping after setting the refreshing interval.

[Limitation]

It is not possible to prevent this problem completely due to the specifications of the device, though setting the refreshing interval longer decreases the number of times that this problem occurs. Please avoid use of the SDRAM or DRAM interface where possible because the evaluation of the interface with the E10A or E10A-USB emulator cannot be done correctly.

If you fully understood this limitation and still wish to use the SDRAM or DRAM interface, we recommend that you take any of the following ways to adjust the refreshing interval so that the frequency of this problem will be decreased:

- Set bits RTCK2 to RTCK0 in REFCR to make the refresh count clock as low as possible within the range defined by the refreshing interval specification for the SDRAM or DRAM used.
- Set the compare match cycle of registers RTCNT and RTCOR as long as possible within the range defined by the refreshing interval specification for the SDRAM or DRAM used.

