ISL70024SEH, ISL73024SEH

Introduction

This report documents the results of low and high dose rate total dose testing and subsequent high temperature biased annealing of the ISL70024SEH and ISL73024SEH 200V, 7.5A N-Channel enhancement mode GaN transistor. The tests were conducted to provide an assessment of the total dose hardness of the part and to provide an estimate of dose rate, bias, or anneal sensitivity. Parts were irradiated under three different bias conditions:

- T_{OFF} – gate and source grounded; drain connected to 160V ±4V
- T_{ON} – gate connected to 4.5V ±10%; drain and source connected to ground
- All pins grounded at Low Dose Rate (LDR) and at High Dose Rate (HDR)

Figure 2, Figure 3, and Figure 4 show the bias schematics for each of these test conditions. The ISL70024SEH is rated at 100krad(Si) at HDR (50rad – 300rad(Si)/s) and at 75krad(Si) at LDR (0.01rad(Si)/s) and is acceptance tested on a lot-by-lot basis to these limits. The ISL73024SEH is rated at 75krad(Si) at LDR (0.01rad(Si)/s) and is acceptance tested to these limits. Both parts use the same die and the dataset reported in this document applies to both.

Product Description

The ISL70024SEH is a 200V N-channel enhancement mode GaN power transistor. Applications for these devices include commercial aerospace, medical, and nuclear power generation. GaN's exceptionally high electron mobility and low temperature coefficient allows for a very low $r_{DS(ON)}$ of 55mΩ (typical), while its lateral device structure and majority carrier diode provide an exceptionally low Q_G of 2.5nC (typical) and near zero Q_{RR}. The end result is a device that can operate at a higher switching frequency with more efficiency while reducing the overall solution size.

The ISL70024SEH operates across the -55°C to +125°C temperature range and is offered in a hermetically sealed Surface Mount Device (SMD) 4-pin package. Manufacturing in a MIL-PRF-38535 like flow results in best-in-class power transistors, which are ideally suited for high reliability applications.

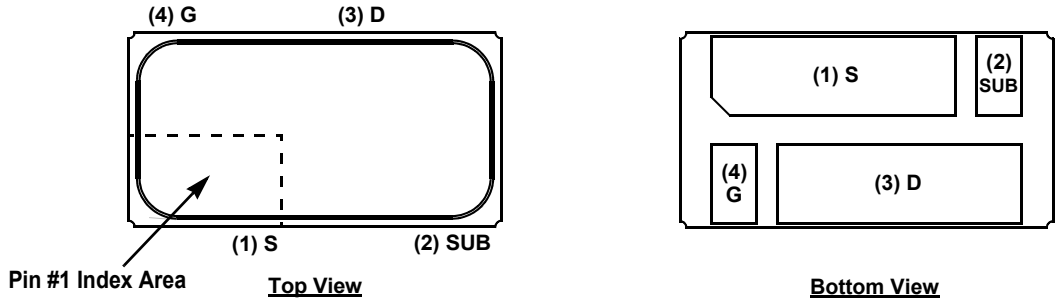
Related Literature

For a full list of related documents, visit our website

- ISL70024SEH, ISL73024SEH product page
- MIL-STD-883 Test Method 1019

1. Pin Configuration

ISL70024SEH
(4 Pin SMD)



Note:The ESD triangular mark is indicative of Pin #1. It is a part of the device marking and is placed on the lid in the quadrant where Pin #1 is located.

Figure 1. ISL70024SEH Pinout Configuration

Table 1. ISL70024SEH Pin Descriptions

Pin Number	Pin Name	Description
1	S	Source connection for the GaN FET.
2	SUB	Substrate connection for the GaN FET, which is internally shorted in to source. Tie this pin to source on the PCB.
3	D	Drain connection for the GaN FET
4	G	Gate connection for the GaN FET. Minimize trace inductance from driver to reduce over-stressing the gate.
NA	Lid	Internally tied to the source pin.

2. Test Description

2.1 Irradiation Facilities

HDR testing was performed at 167.5rad(Si)/s using a Gammacell industry standard irradiator located in the Palm Bay, Florida Renesas facility. LDR testing was performed at 0.01rad(Si)/s using the Renesas Palm Bay Hopewell Designs N40 panoramic irradiator. Both irradiators use PbAl spectrum hardening filters to shield the test board and devices under test against low energy secondary gamma radiation. Biased irradiation and annealing were performed on all samples following irradiation, at +100°C for 168 hours in a small temperature chamber.

2.2 Test Fixturing

Figure 2, Figure 3, and Figure 4 show the configurations used for biased irradiation at both dose rates.

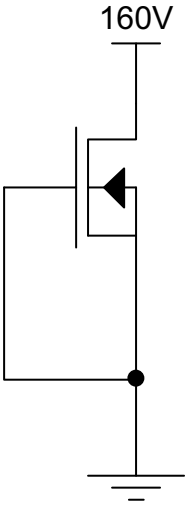


Figure 2. ISL70024SEH TID Bias Schematics (T_{OFF})

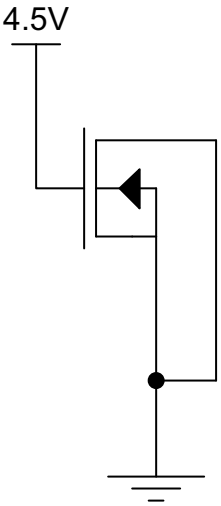


Figure 3. ISL70024SEH TID Bias Schematics (T_{ON})

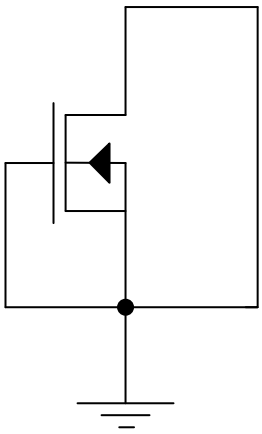


Figure 4. ISL70024SEH TID Bias Schematics (Grounded)

2.3 Characterization Equipment and Procedures

All electrical testing was performed at room temperature outside the irradiator, using production Automated Test Equipment (ATE) with datalogging at each downpoint.

2.4 Experimental Matrix

Irradiation was performed in accordance with the guidelines of MIL-STD-883 Test Method 1019. The experimental matrix consisted of 20 samples irradiated at LDR under T_{OFF} bias, 20 samples irradiated at LDR under T_{ON} bias, 20 samples irradiated at LDR with all pins grounded, 16 samples irradiated at HDR under T_{OFF} bias, 16 samples irradiated at HDR under T_{ON} bias, and 16 samples irradiated at HDR with all pins grounded. At anneal, the parts with all leads grounded parts were split, with half of units biased in the T_{OFF} configuration and half of the units biased in the T_{ON} configuration. The worst case of the two data points was plotted. Three control units were used.

The ISL70024SEH HDR samples were drawn equally from two wafer lots: QUALJSD2 and QUALJSD3. The LDR samples were drawn equally from wafer lots QUALJSD3 and QUALJSD4. All samples were packaged in the hermetic 42mm^2 4-pin surface mount package (code J4.A). Samples were processed through the standard burn-in cycle before irradiation.

2.5 Downpoints

Downpoints for the LDR tests were 0, 10, 30, 50, and 75krad(Si). Downpoints for the HDR tests were 0, 30, 50, 100, and 150krad(Si). All irradiations were followed by a 168 hour high temperature anneal at +100°C under bias.

3. Test Results

3.1 Attributes Data

Table 2 summarizes the results of the ISL70024SEH total dose testing.

Table 2. ISL70024SEH Total Dose Test Attributes Data

Dose Rate (rad(Si)/s)	Bias	Sample Size	Downpoint	Pass[1]	Fail
0.01	T_{OFF}, Figure 2	20	Pre-irradiation	20	
			10krad(Si)	20	0
			30krad(Si)	20	0
			50krad(Si)	20	0
			75krad(Si)	20	0
			Anneal	20	0
0.01	T_{ON}, Figure 3	20	Pre-irradiation	20	
			10krad(Si)	20	0
			30krad(Si)	20	0
			50krad(Si)	20	0
			75krad(Si)	20	0
			Anneal	20	0
0.01	GND, Figure 4	20	Pre-irradiation	20	
			10krad(Si)	20	0
			30krad(Si)	20	0
			50krad(Si)	20	0
			75krad(Si)	20	0
			Anneal	20	0
167.5	T_{OFF}, Figure 2	16	Pre-irradiation	16	
			10krad(Si)	16	0
			30krad(Si)	16	0
			50krad(Si)	16	0
			75krad(Si)	16	0
			Anneal	16	0

Table 2. ISL70024SEH Total Dose Test Attributes Data (Cont.)

Dose Rate (rad(Si)/s)	Bias	Sample Size	Downpoint	Pass[1]	Fail
167.5	T_{ON}, Figure 3	16	Pre-irradiation	16	
			10krad(Si)	16	0
			30krad(Si)	16	0
			50krad(Si)	16	0
			75krad(Si)	16	0
			Anneal	16	0
167.5	GND, Figure 4	16	Pre-irradiation	16	
			10krad(Si)	16	0
			30krad(Si)	16	0
			50krad(Si)	16	0
			75krad(Si)	16	0
			Anneal	16	0

1. A Pass indicates a sample that passes all datasheet limits.

3.2 Key Parameter Listing

Table 3 lists 11 key parameters that are indicative of part performance. These parameters are plotted in Figure 5 through Figure 15. All limits are taken from the *ISL70024SEH datasheet*. See the datasheet for further detail.

Table 3. ISL70024SEH Key Total Dose Datasheet Parameters (T_A = 25°C)

Figure	Symbol	Parameter	Limit, Low	Limit, High	Unit	Conditions
5	I_{DSS}	Drain-Source Leakage Current	-	115	µA	V_{DS} = 160V, V_{GS} = 0V
6	I_{GSX}	Drain-Gate Leakage Current	-115	-	µA	V_{DS} = 160V, V_{GS} = 0V
7	I_{GSS}	Gate-Source Forward Leakage	-	2.5	mA	V_{GS} = 5V
8		Gate-Source Reverse Leakage	-100	-	µA	V_{GS} = -4V
9	$V_{GS(th)}$	Gate Threshold Voltage	0.8	2.5	V	V_{DS} = V_{GS}, I_D = 1.5mA
10	$R_{DS(ON)}$	Drain-Source On Resistance	-	110	mΩ	V_{GS} = 5V, I_D = 1.5A
11	V_{SD}	Source-Drain Forward Voltage	0.8	3.5	V	I_S = 0.5A, V_{GS} = 0V
12	Q_{GD}	Gate-Drain Charge	-	2	nC	V_{DS} = 100V, I_D = 7A
13	Q_{GS}	Gate-Source Charge	-	2	nC	V_{DS} = 100V, I_D = 7A
14	Q_G	Total Gate Charge	-	5	nC	V_{DS} = 100V, I_D = 7A, V_{GS} = 5V
15	C_{OSS}	Output Capacitance	-	200	pF	V_{DS} = 100V, V_{GS} = 0V

3.3 Key Parameters Variables Data

The plots in Figure 5 through Figure 15 illustrate the TID response of the key datasheet parameters outlined in Key Parameter Listing. The plots show the average tested values of the key parameters shown in Table 3 as a function of total dose for each of the three irradiation conditions (T_{OFF}, T_{ON}, and GND) at HDR and LDR. For example, the legend LDR_Toff indicates the average LDR response for parts biased in the T_{OFF} configuration. PA_L on the graphs stands for Post-Anneal Low Dose and PA_H represents the Post-Anneal High Dose results. Note that the worst case of the two bias configurations of the samples that were irradiated with all terminals grounded, as described in Experimental Matrix, is plotted. The plots also include error bars at each downpoint, representing the minimum and maximum measured values of the samples, although in some plots the error bars are not visible due to their values as compared to the scale of the graph. Also, in some plots the datasheet limits, which are set by temperature, are not shown to better display the actual measurements, which are orders of magnitude less.

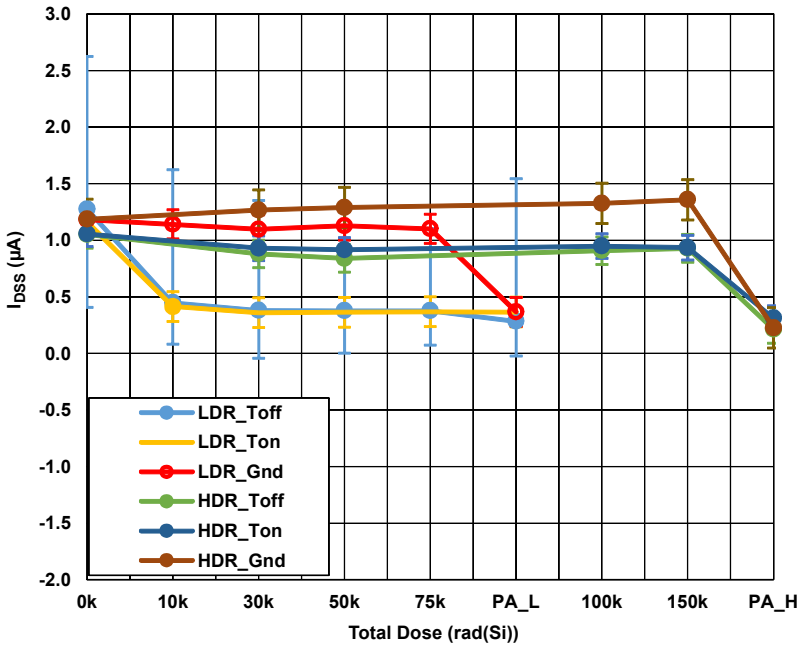


Figure 5. ISL70024SEH drain-to-source leakage current, I_{DSS}, with V_{DS} = 160V and V_{GS} = 0V, as a function of total dose irradiation at LDR and HDR for all three bias cases. The datasheet limit, which is set by temperature, is 115µA maximum, but is not shown to better display the actual measurements, which are orders of magnitude less.

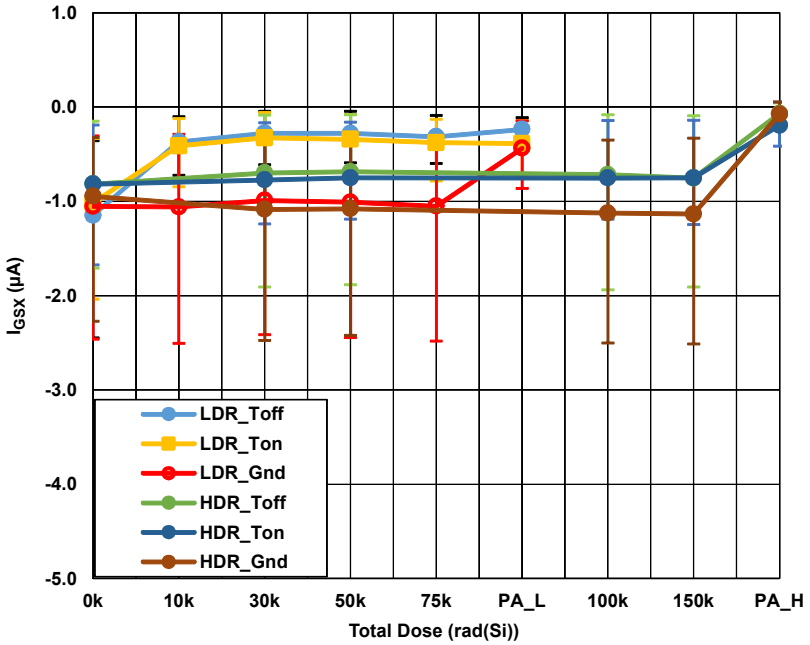


Figure 6. ISL70024SEH drain-to-gate leakage current, I_{GSX}, with V_{DS} = 160V and V_{GS} = 0V, as a function of total dose irradiation at LDR and HDR for all three bias cases. The datasheet limit, which is set by temperature, is -115µA minimum, but is not shown to better display the actual measurements, which are orders of magnitude less.

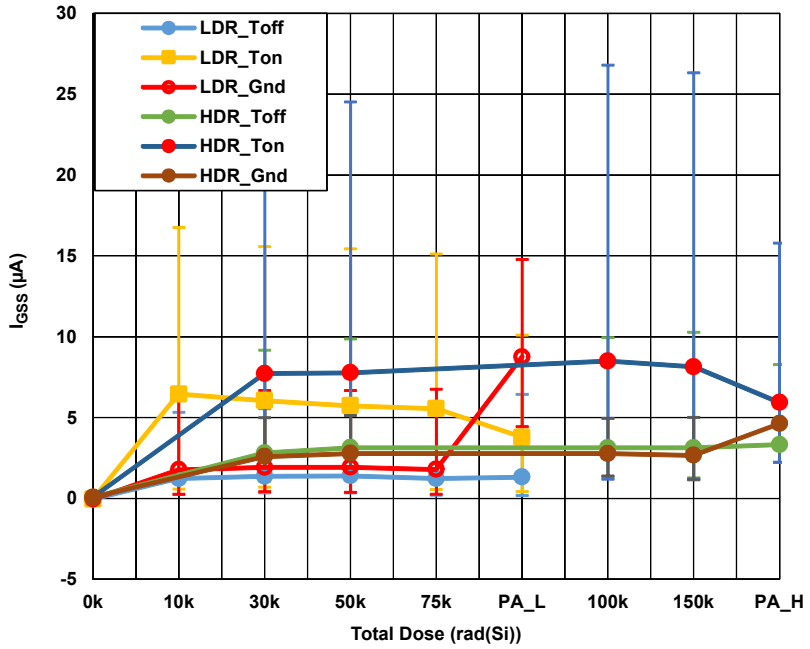


Figure 7. ISL70024SEH gate-to-source forward leakage current, I_{GSS}, with V_{GS} = 5V, as a function of total dose irradiation at LDR and HDR for all three bias cases. The datasheet limit, which is set by temperature, is 2500µA maximum, but is not shown to better display the actual measurements, which are orders of magnitude less.

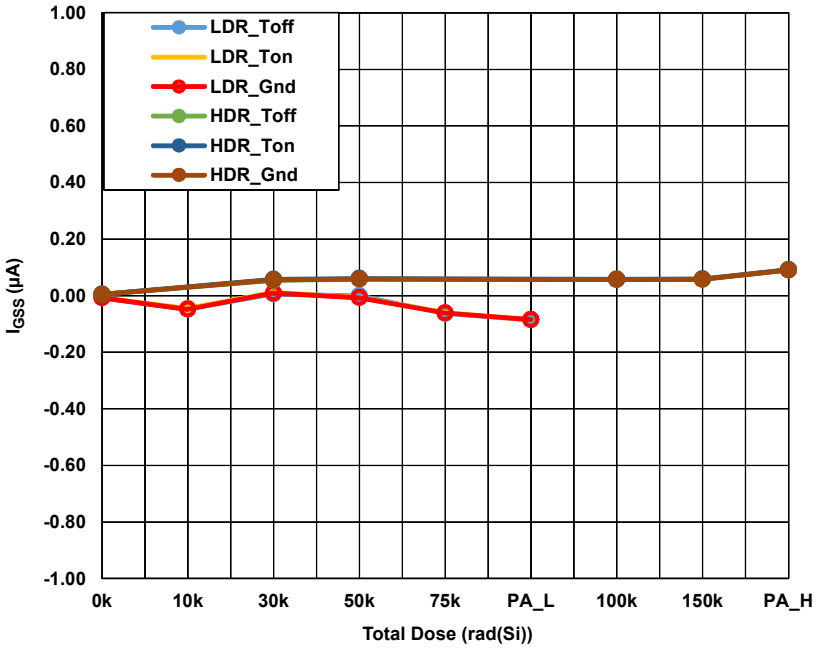


Figure 8. ISL70024SEH gate-to-source reverse leakage current, I_{GSS}, with V_{GS} = -4V, as a function of total dose irradiation at LDR and HDR for all three bias cases. The datasheet limit, which is set by temperature, is -100µA minimum, but is not shown to better display the actual measurements, which are orders of magnitude less.

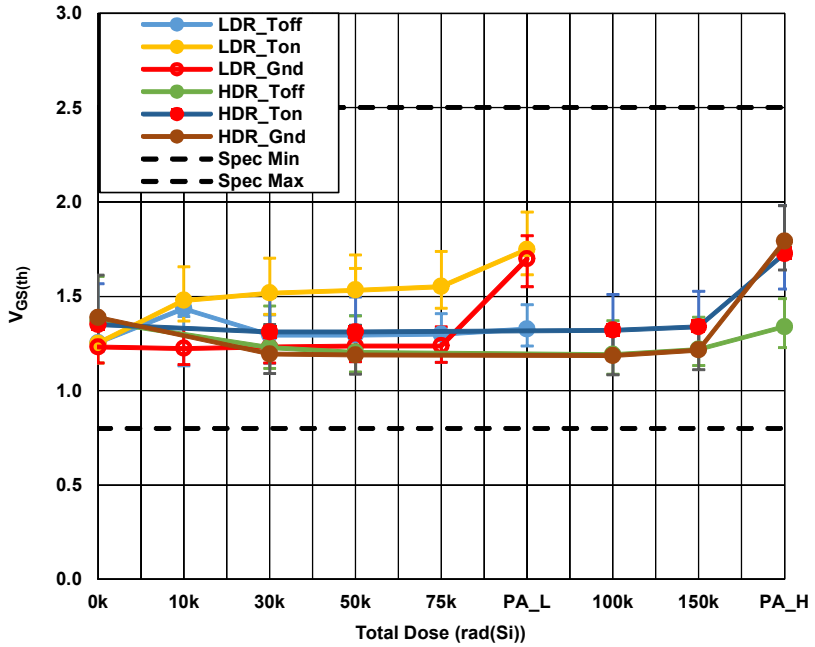


Figure 9. ISL70024SEH gate threshold voltage, $V_{GS(th)}$, with V_{DS} = V_{GS}, I_{DS} = 1.5mA, as a function of total dose irradiation at LDR and HDR for all three bias cases. The datasheet limits are 0.8V minimum and 2.5V maximum.

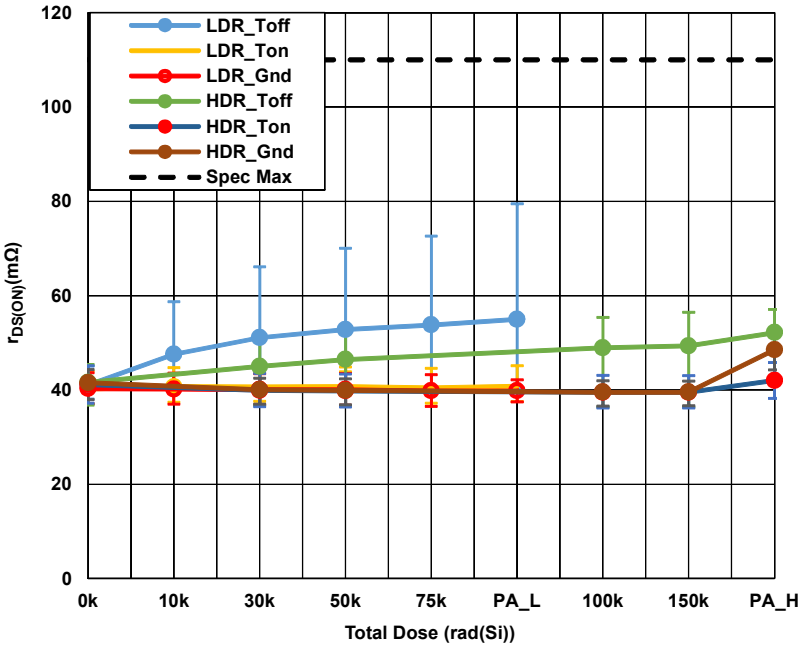


Figure 10. ISL70024SEH drain-to-source On-Resistance, $r_{DS(ON)}$, with V_{GS} = 5V, I_D = 7A, as a function of total dose irradiation at LDR and HDR for all three bias cases. The datasheet limit is 110mΩ maximum.

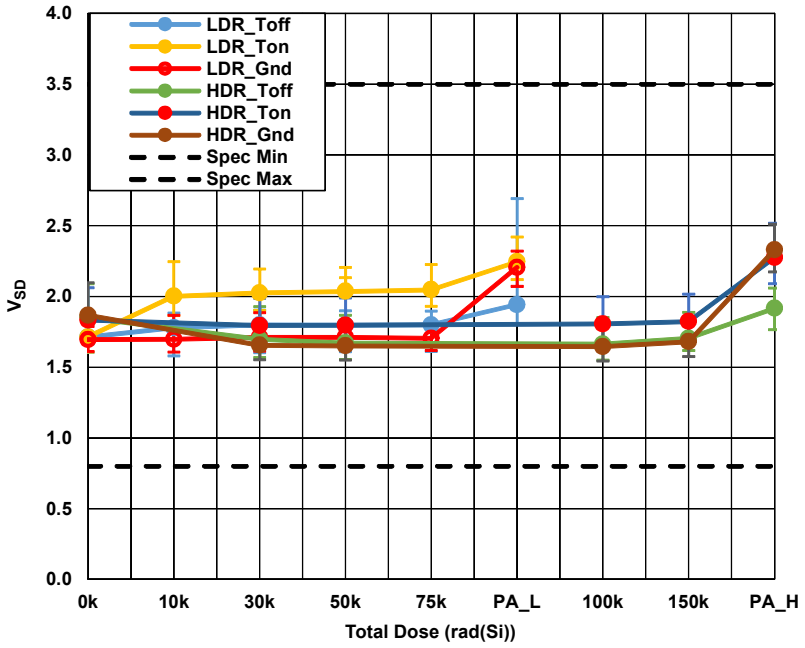


Figure 11. ISL70024SEH source-to-drain forward voltage, V_{SD}, with I_S = 0.5A, V_{GS} = 0V, as a function of total dose irradiation at LDR and HDR for all three bias cases. The datasheet limits are 0.8V minimum and 3.5V maximum.

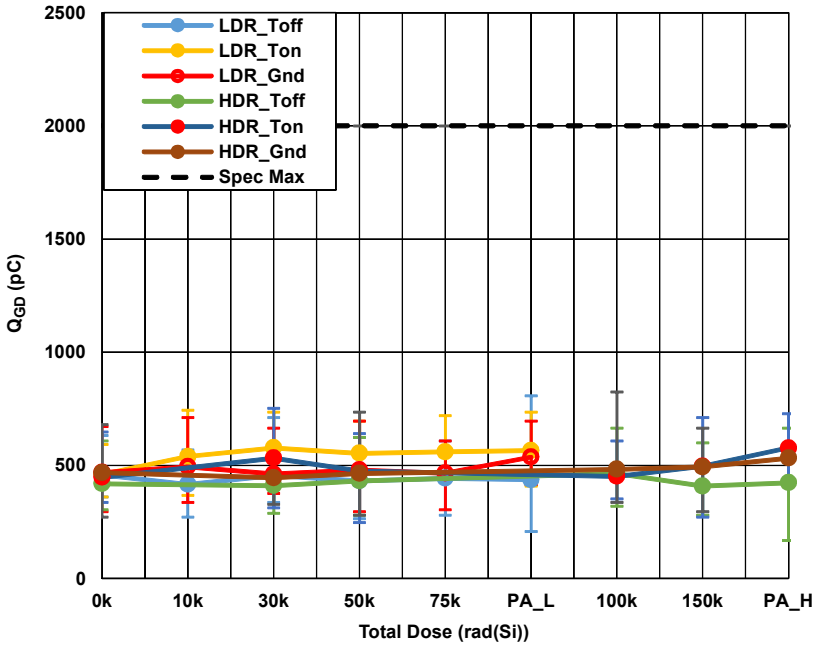


Figure 12. ISL70024SEH gate-to-drain charge, Q_{GD}, with V_{DS} = 100V, I_D = 7A, as a function of total dose irradiation at LDR and HDR for all three bias cases. The datasheet limit is 2nC maximum.

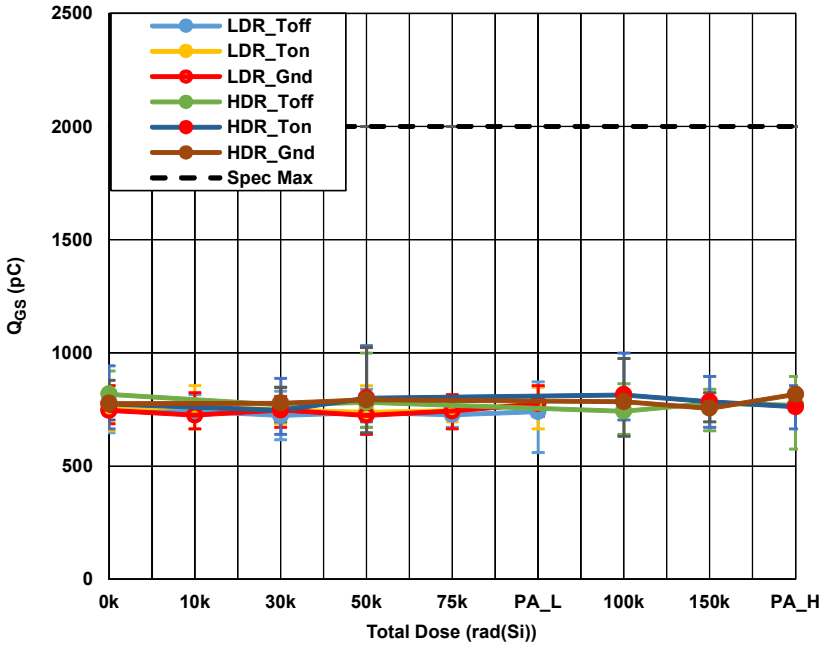


Figure 13. ISL70024SEH gate-to-source charge, Q_{GS}, with V_{DS} = 100V, I_D = 7A, as a function of total dose irradiation at LDR and HDR for all three bias cases. The datasheet limit is 2nC maximum.

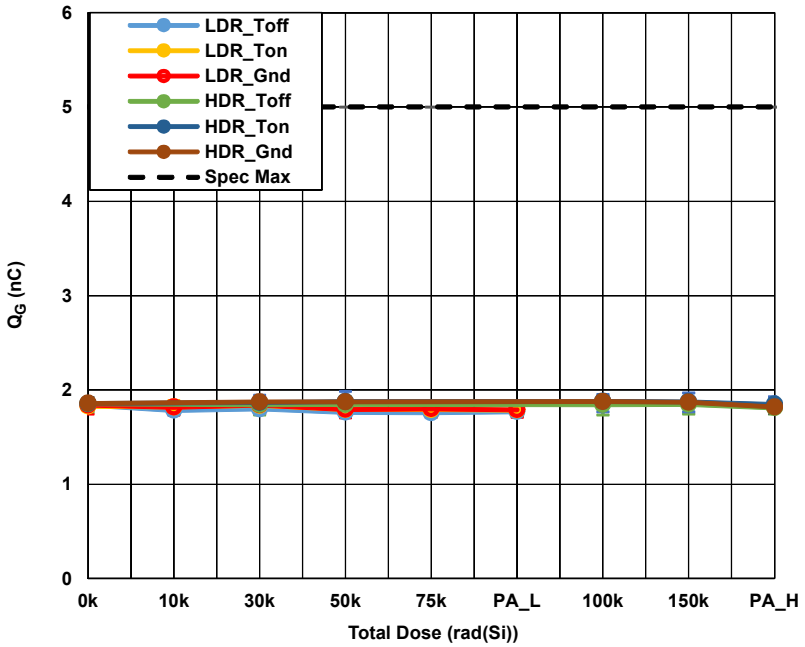


Figure 14. ISL70024SEH total gate charge, Q_G, with V_{DS} = 100V, I_D = 7A, V_{GS} = 5V, as a function of total dose irradiation at LDR and HDR for all three bias cases. The datasheet limit is 5nC maximum.

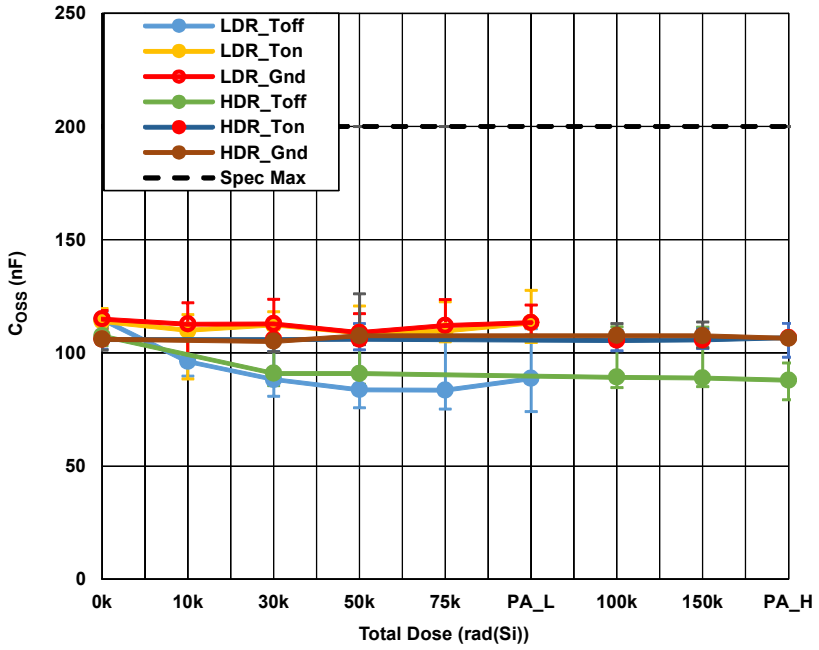


Figure 15. ISL70024SEH output capacitance, C_{OSS}, with V_{DS} = 100V, V_{GS} = 0V, as a function of total dose irradiation at LDR and HDR for all three bias cases. The datasheet limit is 200pF maximum.

4. Discussion and Conclusion

We report the results of an LDR and HDR total dose test of the ISL70024SEH 200V, 7.5A N-Channel enhancement mode GaN transistor. All irradiations were followed by a 168-hour anneal at +100°C under bias. Attributes Data summarizes the attributes data for the test. Key Parameter Listing summarizes the 11 critical parameters for the part. Key Parameters Variables Data provides plots of the total dose and anneal response for the critical parameters.

All parameters remained well within the datasheet limits at all downpoints and showed no significant differences in total dose response between LDR and HDR irradiations. However, some slight bias variances can be seen in a few plots. The T_{ON} bias configuration responses differ somewhat from the others in Figure 7, Figure 9, and Figure 11, both during exposure and anneal. In Figure 7, both sets of samples biased in the T_{ON} configurations show an increase in $_{IGSS}$ leakage current over the other two bias configurations, and although the average increase was ≤ 6µA, there were some significantly higher measurements as illustrated by the upper error bars.

Anneal sensitivity is present in some parameters, with the samples biased in the T_{ON} configuration, including the parts that were exposed in the GND bias configuration, showing more shift than the parts biased in the T_{OFF} configuration.

In Figure 9, $V_{GS(th)}$ shows about a 0.3V increase during exposure for the LDR_Ton bias configuration, while the HDR_Ton displays a slight increase over the other samples. However, during anneal there is a significant increase in the $V_{GS(th)}$ measurement for all samples biased in the T_{ON} configuration, including the parts that were exposed in the GND bias configuration. A similar response can be seen for the V_{SD} measurements in Figure 11. These positive post-anneal voltage shifts are probably caused by the release of holes that become trapped during TID exposure, and/or their neutralization by electrons from the channel. The T_{ON} bias configuration exacerbates this shift.

In Figure 10, it can be seen that the samples biased in the T_{OFF} configuration, show an increase in $r_{DS(on)}$ as compared to the other bias configurations; however, all measurements are well below the limit of 110mΩ.

5. Revision History

Rev.	Date	Description
1.00	Nov 28, 2022	Applied new template. Added ISL73024SEH information to page 1.
0.00	Dec 4, 2017	Initial release

IMPORTANT NOTICE AND DISCLAIMER

RENESAS ELECTRONICS CORPORATION AND ITS SUBSIDIARIES (“RENESAS”) PROVIDES TECHNICAL SPECIFICATIONS AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for developers skilled in the art designing with Renesas products. You are solely responsible for (1) selecting the appropriate products for your application, (2) designing, validating, and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. Renesas grants you permission to use these resources only for development of an application that uses Renesas products. Other reproduction or use of these resources is strictly prohibited. No license is granted to any other Renesas intellectual property or to any third party intellectual property. Renesas disclaims responsibility for, and you will fully indemnify Renesas and its representatives against, any claims, damages, costs, losses, or liabilities arising out of your use of these resources. Renesas' products are provided only subject to Renesas' Terms and Conditions of Sale or other applicable terms agreed to in writing. No use of any Renesas resources expands or otherwise alters any applicable warranties or warranty disclaimers for these products.

(Rev.1.0 Mar 2020)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit:
www.renesas.com/contact/