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H8SX Series

PWM 15-Phase Output

Introduction

As well as having an architecture that is upward-compatible with each CPU of the H8/300, H8/300H, and H8S series, so as to inherit a full complement of peripheral functions, the H8SX microcomputer series has a maximum operating frequency of 50 MHz and uses a 32-bit H8SX core CPU as well as an on-chip multiplier/divider to improve performance.

This H8SX series Application Note provides information you may need during software and hardware design. This is a basic edition that provides operation examples that each use a single H8SX series on-chip peripheral function.

Although the operation of each program, circuit, and other aspects covered by this application note has been checked, make sure that you conduct your own operation checks before actually using the H8SX series.

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1. Overview

The six channels of the 16-bit timer pulse unit (TPU) of the H8SX series are all used to output 15-phase PWM waveforms. You can control up to 15 phases for PWM waveform output by setting the timer operating mode of each channel to PWM mode 2 and enabling synchronous operation.

2. Configuration

When synchronous operation is specified for all the channels of the 16-bit timer pulse unit (TPU), the count and clear operations of the timer counters (TCNT_0 to TCNT_5) of all the channels are performed synchronously. The sample shown below uses timer general register A (TGRA_0) of channel 0 for PWM cycle setting and the other timer general registers for the duty setting. This sample outputs pulses at any duty cycle from the output compare output pin (TIOCB0, TIOCC0, TIOCD0, TIOCA1, ..., or TIOCB5) for each timer general register other than TGRA_0. When the peripheral module clock (P ϕ) is 25 MHz and the count clock is P ϕ /1, you can set any output pulse cycle between 80 nsec and 2.62 msec. You can also set a duty cycle with a resolution of 1/65535.

In the following explanation, channel 0 of the 16-bit timer pulse unit is called TPU0 while channel 1 is called TPU1. Figure 1 is a block diagram.

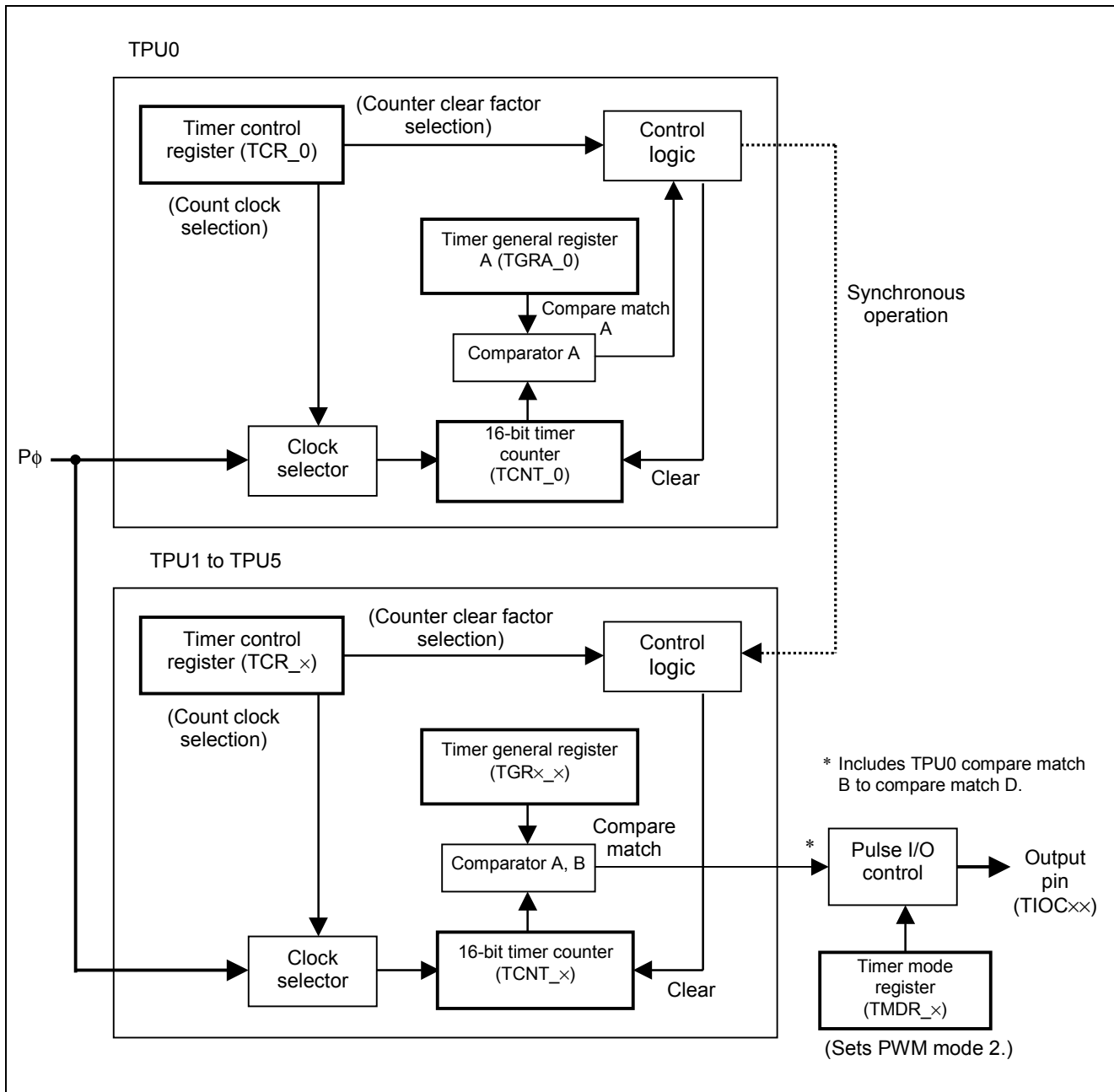


Figure 1 Block Diagram of PWM 15-Phase Output

Figure 2 shows an example of PWM 15-phase output.

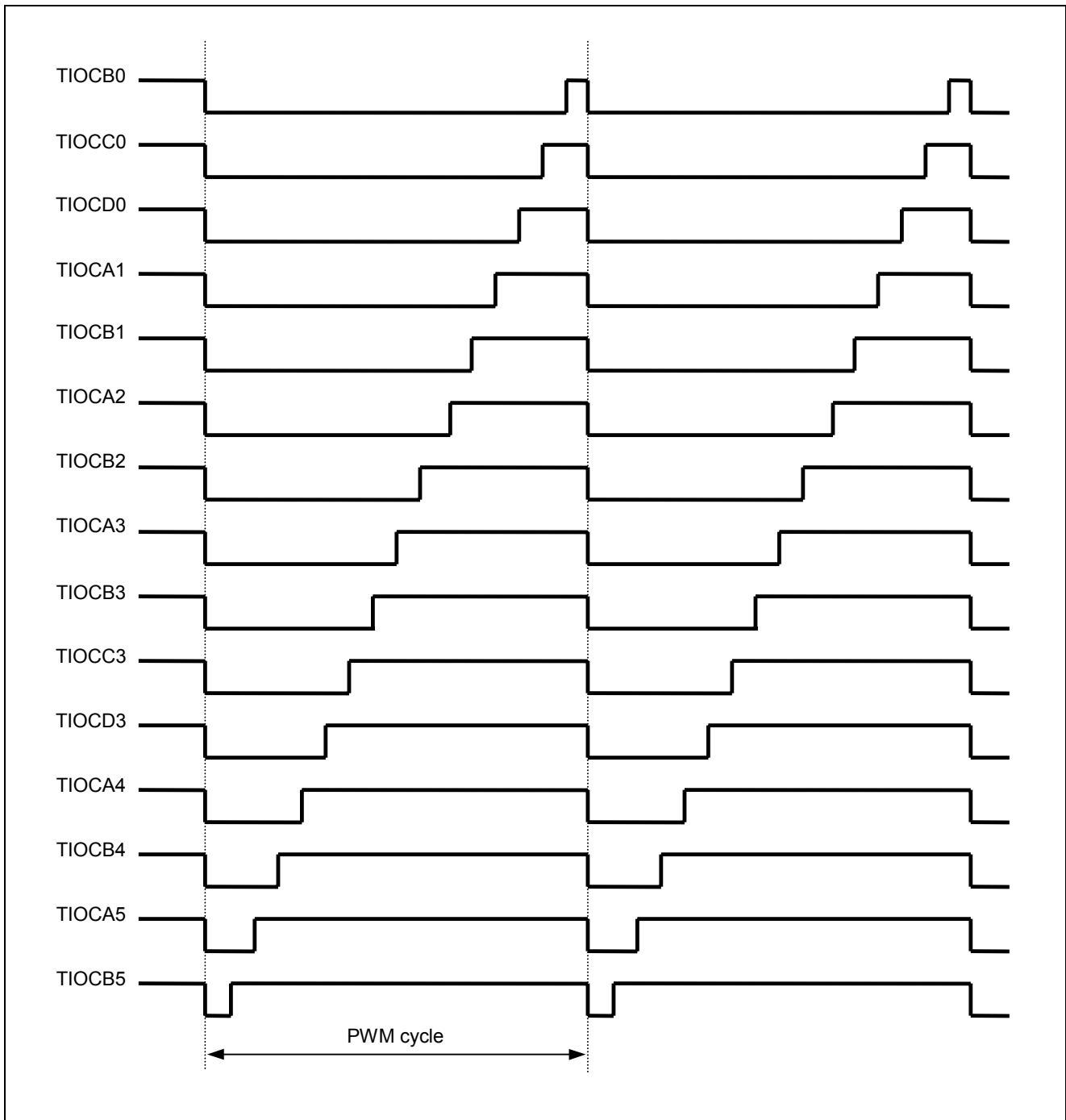


Figure 2 Example of PWM 15-Phase Output

3. Sample Program

3.1 Function

This sample program outputs PWM waveforms according to the timer value for the PWM cycle and each duty cycle (low or high width). You can calculate the timer value for the PWM cycle and each pulse low width using the following equations:

$$\text{PWM-cycle} = \text{timer-value} \times \text{TPU1-count clock}$$

$$\text{low-width} = \text{timer-value} \times \text{TPU1-count-clock}$$

Assume that the TPU1 count clock is peripheral module (P ϕ)/1. When P ϕ is 25 MHz, the TPU1 count clock will be 40 nsec. Figure 3 shows an example of operation.

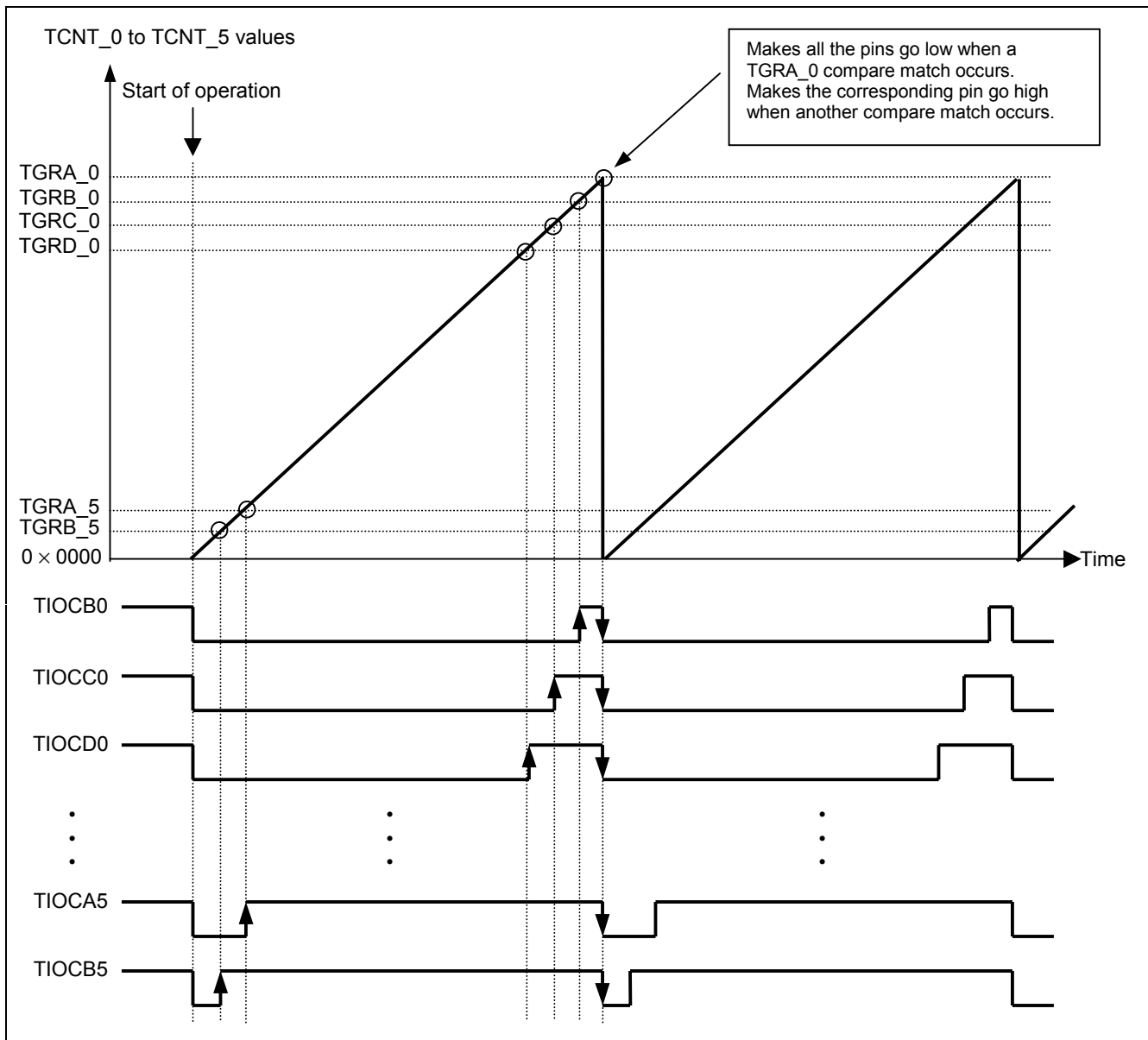


Figure 3 Example of PWM 15-Phase Output Operation

Table 1 lists the function allocations of the 16-bit timer pulse unit (TPU).

Table 1 Function Allocation of the TPU

Type		Name	Function
Common	Register	MSTPCRA	Cancels the TPU module stop mode.
		TSYR	Sets synchronous operation of TPU channels 0 to 5.
		TSTR	Specifies whether to start or stop timer count of TPU channels 0 to 5.
TPU0	Register	TMDR_0	Sets the TPU0 operating mode (PWM mode 2).
		TCR_0	Sets the TCNT_0 count clock and counter clear factor.
		TGRA_0	Sets the compare match counter value for the PWM cycle.
		TGRB_0 to	Sets the compare match counter value for the pulse output low width of each corresponding pin.
		TGRD_0	
		TIORH_0	Sets the output level when a compare match occurs.
	TIORL_0		
Output pin	TIOCB0 to TIOCD0	Compare match output pins	
TPU1	Register	TMDR_1	Sets the TPU1 operating mode (PWM mode 2).
		TCR_1	Sets the TCNT_1 count clock and counter clear factor.
		TGRA_1 to	Sets the compare match counter value for the pulse output low width of each corresponding pin.
		TGRB_1	
	TIOR_1	Sets the output level when a compare match occurs.	
Output pin	TIOCA1 to TIOCB1	Compare match output pins	
TPU2	Register	TMDR_2	Sets the TPU2 operating mode (PWM mode 2).
		TCR_2	Sets the TCNT_2 count clock and counter clear factor.
		TGRA_2 to	Sets the compare match counter value for the pulse output low width of each corresponding pin.
		TGRB_2	
	TIOR_2	Sets the output level when a compare match occurs.	
Output pin	TIOCA2 to TIOCB2	Compare match output pins	
TPU3	Register	TMDR_3	Sets the TPU3 operating mode (PWM mode 2).
		TCR_3	Sets the TCNT_3 count clock and counter clear factor.
		TGRA_3 to	Sets the compare match counter value for the pulse output low width of each corresponding pin.
		TGRD_3	
	TIORH_3	Sets the output level when a compare match occurs.	
Output pin	TIOCA3 to TIOCD3	Compare match output pins	
TPU4	Register	TMDR_4	Sets the TPU4 operating mode (PWM mode 2).
		TCR_4	Sets the TCNT_4 count clock and counter clear factor.
		TGRA_4 to	Sets the compare match counter value for the pulse output low width of each corresponding pin.
		TGRB_4	
	TIOR_4	Sets the output level when a compare match occurs.	
Output pin	TIOCA4 to TIOCB4	Compare match output pins	
TPU5	Register	TMDR_5	Sets the TPU5 operating mode (PWM mode 2).
		TCR_5	Sets the TCNT_5 count clock and counter clear factor.
		TGRA_5 to	Sets the compare match counter value for the pulse output low width of each corresponding pin.
		TGRB_5	
	TIOR_5	Sets the output level when a compare match occurs.	
Output pin	TIOCA5 to TIOCB5	Compare match output pins	

3.2 Function Specifications

The function that sets the PWM 15-phase output is shown as a sample program. The function specifications are listed below.

```
void pwm15_set ( unsigned short *low_count, unsigned short cyc_count )
```

Argument	Description
*low_count	<p>Start address of the array for storing the timer value for the low width of each PWM pulse.</p> <p>A value between 0×0001 and $0 \times FFFE$ can be specified for each array element. The value must be smaller than cyc_count.</p> <p>If 0×0000 or a value greater than or equal to cyc_count is specified, normal operation is not performed.</p> <p>Each array suffix corresponds to a PWM output pin, as follows:</p> <ul style="list-style-type: none"> [0] ... TIOCB0 [1] ... TIOCC0 [2] ... TIOCD0 [3] ... TIOCA1 [4] ... TIOCB1 [5] ... TIOCA2 [6] ... TIOCB2 [7] ... TIOCA3 [8] ... TIOCB3 [9] ... TIOCC3 [10] ... TIOCD3 [11] ... TIOCA4 [12] ... TIOCB4 [13] ... TIOCA5 [14] ... TIOCB5 <p>The count clock is fixed to $P\phi/1$.</p>
cyc_count	<p>Specifies the timer value for the PWM cycle.</p> <p>A value of between 0×0002 and $0 \times FFFF$ can be specified. The value must be greater than each low_count element.</p> <p>If 0×0000 or a value smaller than or equal to low_count is specified, normal operation is not performed.</p> <p>The count clock is fixed to $P\phi/1$.</p>
Return value	Description
None	—

Example)

```

#define CYCLE_TIME    2400                // Pulse cycle: 2400 μsec
#define LOW_TIME_U    150                 // Low width: 150 μsec
#define P_CLOCK       25                  // Pφ (MHz)
                                           // External function reference declaration
extern void pwm15_set ( unsigned short *, unsigned short );
void main( void )                          // Main routine
{
    char                i;                // Loop counter
    unsigned long       cyc_count;        // Timer value for the pulse cycle
    unsigned long       low_work;
    unsigned short      low_count[15];    // Timer value for the low width

    cyc_count = ((unsigned long)CYCLE_TIME*P_CLOCK);
    for ( i= 0; i<15; i++ )
    {
        low_work      =((unsigned long)(CYCLE_TIME - LOW_TIME_U*(i+1))*P_CLOCK);
        low_count [i]=(unsigned short)low_work;
    }
                                           // Sets pulse output.
    pwm15_set ( low_count, (unsigned short)cyc_count );

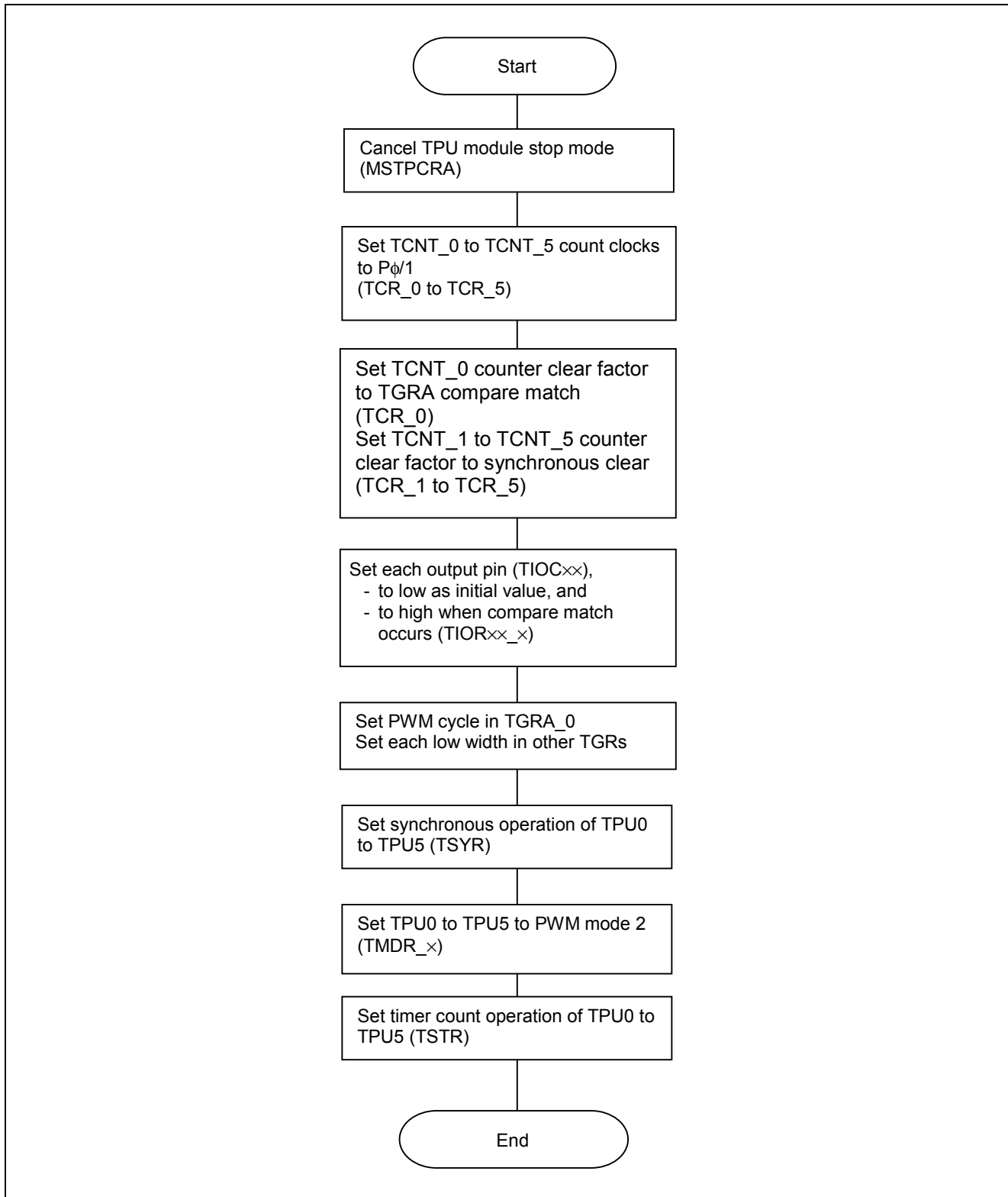
    ..

}

```

3.3 Flowchart

The processing flow is shown below.



3.4 Program Listing

A source program listing is shown below. In this source program, Renesas's standard definition (file automatically generated by High-performance Embedded Workshop: iodefine.h) defines the I/O register structure. To specify your own definition, change the I/O register structure in the sample program.

```

/*****
/* include file
/*****
#include <machine.h>
#include "iodefine.h"

/*****
/* function prototype
/*****
void pwm15_set( unsigned short *, unsigned short );

/*****
/* function definition
/*****
void  pwm15_set( unsigned short *low_count,
                unsigned short  cyc_count )
{
    P_MSTPCRA.BIT.MSTPA0 = 0;    // reset module-standby for TPU

    P_TPU0.TCR.BIT.TPSC = 0;    // set TPU countup clock source
    P_TPU1.TCR.BIT.TPSC = 0;
    P_TPU2.TCR.BIT.TPSC = 0;
    P_TPU3.TCR.BIT.TPSC = 0;
    P_TPU4.TCR.BIT.TPSC = 0;
    P_TPU5.TCR.BIT.TPSC = 0;

    P_TPU0.TCR.BIT.CCLR = 1;    // set TPU counter clear cause
    P_TPU1.TCR.BIT.CCLR = 3;
    P_TPU2.TCR.BIT.CCLR = 3;
    P_TPU3.TCR.BIT.CCLR = 3;
    P_TPU4.TCR.BIT.CCLR = 3;
    P_TPU5.TCR.BIT.CCLR = 3;

    P_TPU0.TIOR.BIT.IOA = 0;    // set TPU output for terminal
    P_TPU0.TIOR.BIT.IOB = 2;
    P_TPU0.TIOR.BIT.IOC = 2;
    P_TPU0.TIOR.BIT.IOD = 2;
    P_TPU1.TIOR.BIT.IOA = 2;
    P_TPU1.TIOR.BIT.IOB = 2;
    P_TPU2.TIOR.BIT.IOA = 2;
    P_TPU2.TIOR.BIT.IOB = 2;
    P_TPU3.TIOR.BIT.IOA = 2;
    P_TPU3.TIOR.BIT.IOB = 2;
    P_TPU3.TIOR.BIT.IOC = 2;
    P_TPU3.TIOR.BIT.IOD = 2;
    P_TPU4.TIOR.BIT.IOA = 2;
    P_TPU4.TIOR.BIT.IOB = 2;

```

```

P_TPU5.TIOR.BIT.IOA = 2;
P_TPU5.TIOR.BIT.IOB = 2;

// set TPU compare value
P_TPU0.TGRA = (unsigned int)cyc_count;
P_TPU0.TGRB = (unsigned int)low_count [ 0];
P_TPU0.TGRC = (unsigned int)low_count [ 1];
P_TPU0.TGRD = (unsigned int)low_count [ 2];
P_TPU1.TGRA = (unsigned int)low_count [ 3];
P_TPU1.TGRB = (unsigned int)low_count [ 4];
P_TPU2.TGRA = (unsigned int)low_count [ 5];
P_TPU2.TGRB = (unsigned int)low_count [ 6];
P_TPU3.TGRA = (unsigned int)low_count [ 7];
P_TPU3.TGRB = (unsigned int)low_count [ 8];
P_TPU3.TGRC = (unsigned int)low_count [ 9];
P_TPU3.TGRD = (unsigned int)low_count [10];
P_TPU4.TGRA = (unsigned int)low_count [11];
P_TPU4.TGRB = (unsigned int)low_count [12];
P_TPU5.TGRA = (unsigned int)low_count [13];
P_TPU5.TGRB = (unsigned int)low_count [14];

P_TPU.TSYR.BIT.SYNC0 = 1; // set TPU0~TPU5 synchronous
P_TPU.TSYR.BIT.SYNC1 = 1;
P_TPU.TSYR.BIT.SYNC2 = 1;
P_TPU.TSYR.BIT.SYNC3 = 1;
P_TPU.TSYR.BIT.SYNC4 = 1;
P_TPU.TSYR.BIT.SYNC5 = 1;

P_TPU0.TMDR.BIT.MD = 3; // set TPU0~TPU5 PWM-mode-2
P_TPU1.TMDR.BIT.MD = 3;
P_TPU2.TMDR.BIT.MD = 3;
P_TPU3.TMDR.BIT.MD = 3;
P_TPU4.TMDR.BIT.MD = 3;
P_TPU5.TMDR.BIT.MD = 3;

P_TPU.TSTR.BIT.CST0 = 1; // start TPU0~TPU5
P_TPU.TSTR.BIT.CST1 = 1;
P_TPU.TSTR.BIT.CST2 = 1;
P_TPU.TSTR.BIT.CST3 = 1;
P_TPU.TSTR.BIT.CST4 = 1;
P_TPU.TSTR.BIT.CST5 = 1;
}

```

Revision Record

Rev.	Date	Description	
		Page	Summary
1.00	Sept.19.03	—	First edition issued

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