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SH7280 Group

Data Transfer between Memory Areas with DMAC

Introduction

This application note provides an example of transferring data between memory areas with the direct memory access controller (DMAC) of the SH7285.

Target Device

SH7285

Contents

1. Preface

1.1 Specifications

- DMAC channel 0 is used to transfer data from the on-chip RAM to external memory. Data are transferred in cycle-stealing mode.
- Auto-request mode (software transfer request) is used for requesting DMA transfer.

1.2 Module Used

- Direct memory access controller (DMAC channel 0)

1.3 Applicable Conditions

- MCU: SH7285/SH7286/SH7243
- Operating frequency: Internal clock 100 MHz
  Bus clock 50 MHz
  Peripheral clock 50 MHz
- C compiler: SuperH RISC engine family C/C++ compiler package Ver.9.01 Release01 from Renesas Technology Corp.
- Compiler options: -cpu=sh2a -include="$(WORKSPDIR)\inc" -object="$(CONFIGDIR)\$(FILELEAF).obj" -debug -gbr=auto -chgincpath-errorpath -global_volatile=0 -opt_range=all -infinite_loop=0-del_vacant_loop=0 -struct_alloc=1 -nologo

2. Description of the Sample Application

This sample application employs the direct memory access controller (DMAC) to transfer data from the on-chip RAM to external memory.

2.1 Summary of MCU Module Used

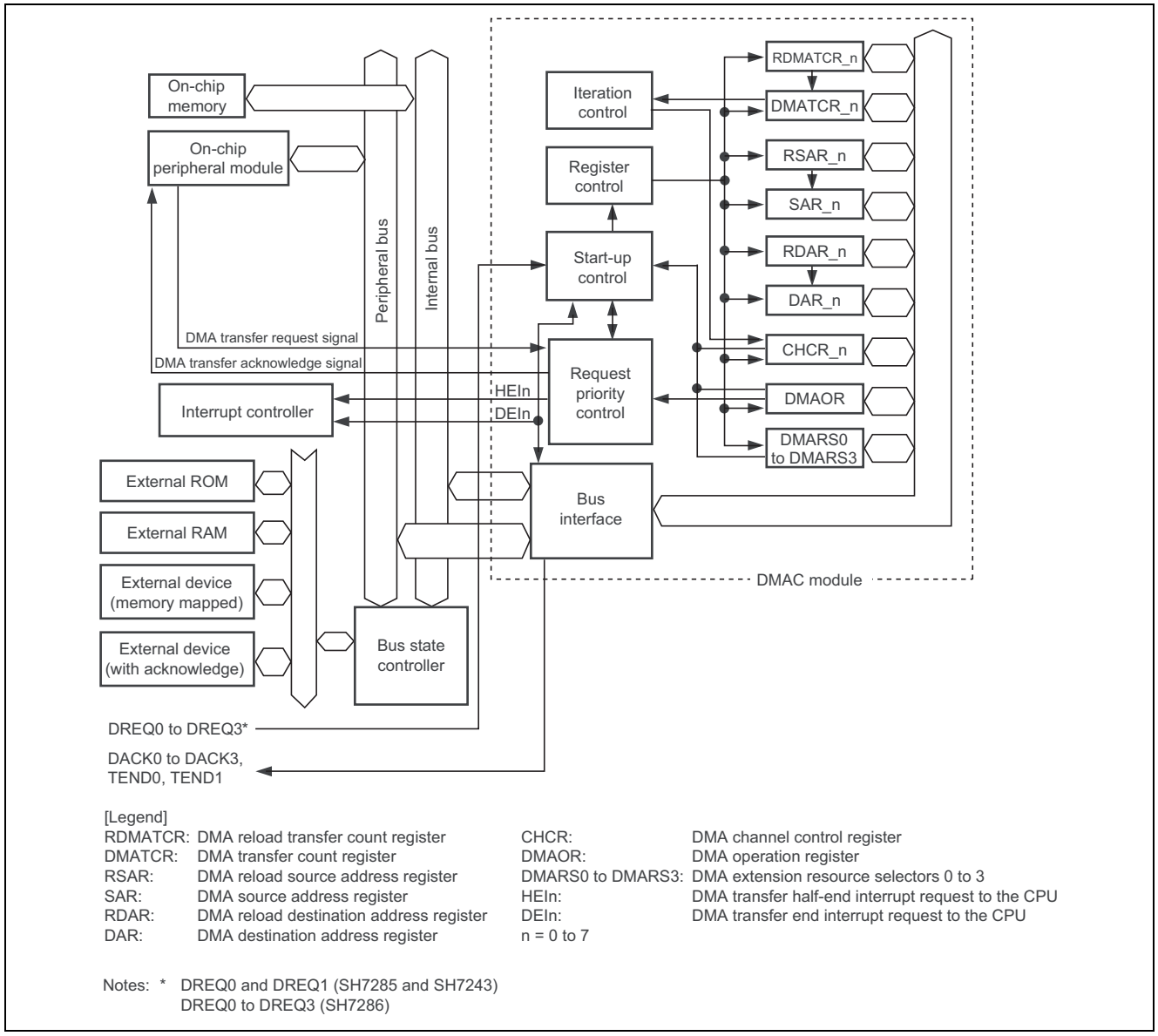
When a DMA transfer request is made, the DMAC starts to transfer data in order of priority of predetermined channels. Then, it continues the transfer operation until transfer end condition is met. It has three transfer request modes: auto request, external request, and on-chip peripheral module request. The bus mode is selectable from burst mode and cycle-stealing mode.

An overview of the DMAC is given in table 1. Also, a block diagram of the DMAC is shown in figure 1.

Table 1 Overview of DMAC

Item	Description
Number of channels	8 channels (CH0 to CH7) Only 3 channels (CH0 to CH2) can receive external requests.
Address space	4 Gbytes
Length of transfer data	Byte, word (2 bytes), longword (4 bytes), and 16 bytes (longword × 4)
Maximum transfer count	16,777,216 (24 bits) transfers
Address mode	Single address mode and dual address mode
Transfer request	Auto request, external request, and on-chip peripheral module request (SCIF: 2 sources, IIC3: 2 sources, A/D converter: 1 source, MTU2: 5 sources, CMT: 2 sources, USB: 2 sources, SSU: 2 sources, RCAN: 1 source)
Bus mode	Cycle-stealing mode and burst mode
Priority level	Channel priority fixed mode and round-robin mode
Interrupt request	An interrupt request to the CPU is made when half or all of a transfer process is completed.
External request detection	DREQ input low/high level detection, rising/falling edge detection
Transfer request acknowledge signal/transfer end signal	Active levels for DACK and TEND can be set independently

Note: For details on the DMAC, refer to the section on the direct memory access controller in the *SH7280 Group Hardware Manual*.



[Legend]

RDMATCR:	DMA reload transfer count register	CHCR:	DMA channel control register
DMATCR:	DMA transfer count register	DMAOR:	DMA operation register
RSAR:	DMA reload source address register	DMARS0 to DMARS3:	DMA extension resource selectors 0 to 3
SAR:	DMA source address register	HEIn:	DMA transfer half-end interrupt request to the CPU
RDAR:	DMA reload destination address register	DEIn:	DMA transfer end interrupt request to the CPU
DAR:	DMA destination address register	n = 0 to 7	

Notes: * DREQ0 and DREQ1 (SH7285 and SH7243)
DREQ0 to DREQ3 (SH7286)

Figure 1 Block Diagram of DMAC

2.2 Procedure for Setting the Module Used

This section describes the procedure for specifying initial settings for transferring data between memory areas with the DMAC. Auto request mode is used for transfer requests. A flowchart of initializing the DMAC is shown in figure 2. For details on registers, refer to the SH7280 Group Hardware Manual.

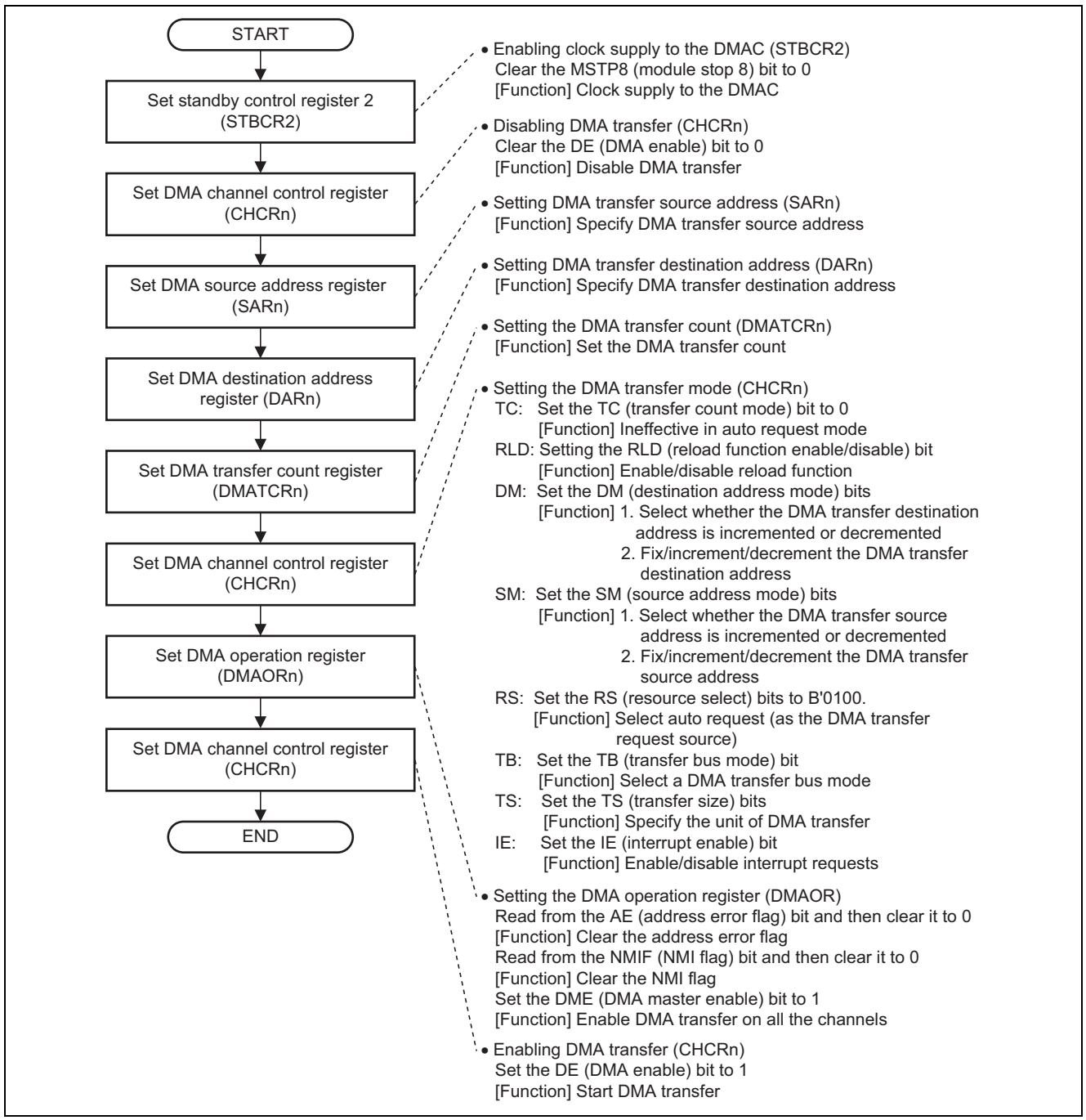


Figure 2 Flowchart of DMAC Initialization

2.3 Description of the Sample Program

In this sample program, DMAC channel 0 is activated by auto request, and data are transferred from the on-chip RAM to external memory in cycle-stealing mode. In cycle-stealing transfer operation, the DMAC gives the bus mastership to the CPU after each round of transferring a single unit of data. An operation timing of the sample application is shown in figure 3.

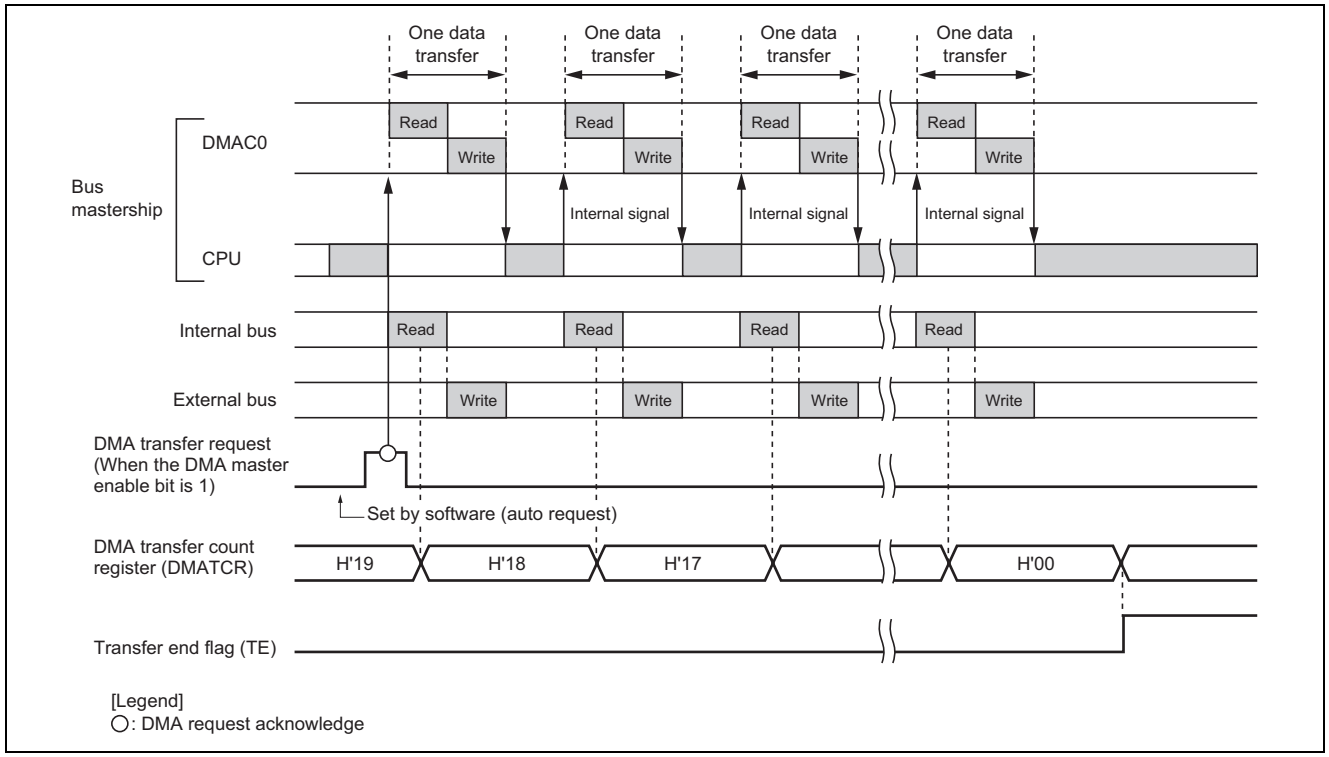


Figure 3 Operation Timing of Sample Application

2.4 Usage Notes on Sample Program

In the reference program, the addresses where the source and destination areas of the transfer start are assigned as absolute addresses for clarity. Ensure that sections used by the user program do not overlap with the source and destination regions that start from the absolute addresses.

2.5 Procedure for Processing by the Sample Program

In this sample program 100-byte data stored in the on-chip RAM are transferred to external memory by DMA transfer. The transfer end flag (TE bit) is used to check whether DMA transfer is completed.

The register settings for the sample program are listed in table 2. The macro definitions used in this sample program are also listed in table 3. A flowchart of the sample program is illustrated in figure 4.

Table 2 Register Settings for Sample Program

Register Name	Address	Setting Value	Description
Standby control register 2 (STBCR2)	H'FFFE 0018	H'00	MSTP8 = "0": DMAC operates
DMA channel control register_0 (CHCR0)	H'FFFE 100C	H'0000 0000	DE = "0": Disables DMA transfer
		H'0000 5410	TC = "0": Ineffective in auto-request mode RLDSAR = "0": Disables the SAR reload function RLDDAR = "0": Disables the DAR reload function DM = "B'01": Increments destination address SM = "B'01": Increments source address RS = "B'0100": Auto request TB = "0": Cycle-stealing mode TS = "B'10": Longword transfer IE = "0": Disables interrupt request
		H'0000 5411	DE = "1": Enables DMA transfer
DMA source address register_0 (SAR0)	H'FFFE 1000	H'FFF8 4000	Set start address of transfer source in an on-chip RAM area
DMA destination address register_0 (DAR0)	H'FFFE 1004	H'0C00 0000	Set start address of transfer destination in an external memory area*
DMA transfer count register_0 (DMATCR0)	H'FFFE 1008	H'64	Transfer count: 100 transfers (H'64)
DMA operation register (DMAOR)	H'FFFE 1200	H'0001	DME = "1": Enables DMA transfer on all the channels
DMA extension resource selector_0 (DMARS0)	H'FFFE 1300	H'0000	Not used for auto request

Note: * The address of external memory area varies depending on the target board to be used.

Table 3 Macro Definitions Used in Sample Program

Macro Definition	Setting Value	Description
SDRAM_DST_ADR	H'0C00 0000	• Start address of SDRAM
SRAM_SRC_ADR	H'FFF8 4000	• Start address of on-chip RAM
SIZE	H'64	• Transfer count
DMA_SIZE_BYTE	H'0000	• Byte transfer
DMA_SIZE_WORD	H'0001	• Word transfer
DMA_SIZE_LONG	H'0002	• Longword transfer
DMA_SIZE_LONGx4	H'0003	• 16-byte transfer
DMA_INT_DISABLE	H'0000	• DMA transfer end interrupt not in use
DMA_INT_ENABLE	H'0010	• DMA transfer end interrupt in use

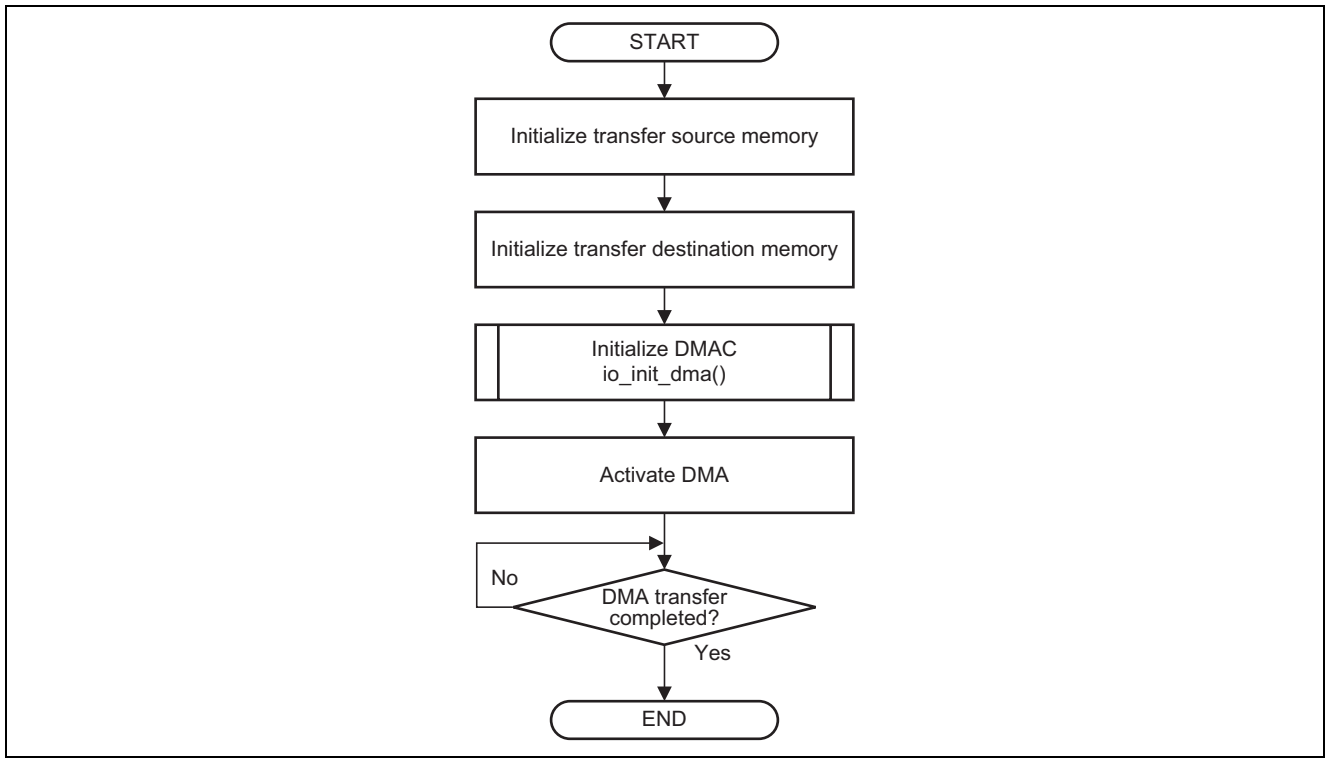


Figure 4 Flowchart of Sample Program

3. Listing of the Sample Program

1. Sample Program Listing: main.c (1)

```
/*""FILE COMMENT""*****************************************************************
*
*       System Name : SH7285 Sample Program
*       File Name   : main.c
*       Contents    : DMAC Sample Program
*       Version     : 1.00.00
*       Model       : M3A-HS85
*       CPU         : SH7285
*       Compiler    : SHC9.1.1.0
*       note        : A sample program for transferring data with the DMAC.
*                   : Software triggers are used to transfer 100-byte data
*                   : from the on-chip SRAM to the external SDRAM.
*
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*
*       history   : 2008.02.26 ver.1.00.00
*""FILE COMMENT END""*************************************************************/
#include <machine.h>
#include <stdio.h>
#include "iodefine.h"       /* SH7285 iodefine  */

/* ==== symbol definition ==== */
#define SDRAM_DST_ADR ((void *)0x0c000000)  /* External SDRAM top address */
#define SRAM_SRC_ADR ((void *)0xfff84000)   /* Internal SRAM address  */
#define SIZE 100                            /* Transmission bytes         */
#define DMA_SIZE_BYTE 0x0000u
#define DMA_SIZE_WORD 0x0001u
#define DMA_SIZE_LONG 0x0002u
#define DMA_SIZE_LONGx4 0x0003u
#define DMA_INT_DISABLE 0x0000u
#define DMA_INT_ENABLE 0x0010u
#define DMA_INT (DMA_INT_ENABLE >> 4u)

/* ==== prototype declaration ==== */
void main(void);
void io_init_dma(void *src, void *dst, size_t size, unsigned int mode);
void io_dma_enable(void);
void io_dma_stop(void);

```

2. Sample Program Listing: main.c (2)

```
46    /*""FUNC COMMENT""*****************************************************
47     * Outline     : Sample program main
48     *-------------------------------------------------------------------------
49     * Include     : #include "iodefine.h"
50     *             : #include <machine.h>
51     *-------------------------------------------------------------------------
52     * Declaration : void main(void);
53     *-------------------------------------------------------------------------
54     * Function    : Sample program main
55     *-------------------------------------------------------------------------
56     * Argument    : void
57     *-------------------------------------------------------------------------
58     * Return Value: void
59     *-------------------------------------------------------------------------
60     * Notice      :
61     *""FUNC COMMENT END""*************************************************/
62    void main(void)
63    {
64        int i;
65        volatile unsigned char *ptr;
66
67        /* ==== Initialize source memory ==== */
68        ptr = SRAM_SRC_ADR;
69        for(i=0; i < SIZE; i++){
70            *ptr++ = 0x55;
71        }
72
73        /* ==== Initialize destination memory ==== */
74        ptr = SDRAM_DST_ADR;
75        for(i=0; i < SIZE; i++){
76            *ptr++ = 0;
77        }
78
79        /* ==== Setting of DMAC ==== */
80        io_init_dma(SRAM_SRC_ADR, SDRAM_DST_ADR, SIZE , DMA_SIZE_LONG | DMA_INT_DISABLE);
81
82        /* ---- DMA start ---- */
83        io_dma_enable();
84
85        /* ---- DMA stop ---- */
86        io_dma_stop();
87
88        while(1){
89            /* Program end */
90        }
91    }
92
```

3. Sample Program Listing: main.c (3)

```
 93    /*""FUNC COMMENT""************************************************
 94     * Outline     : Initialization for DATA transfer between memory areas with DMAC
 95     *-----------------------------------------------------------------------
 96     * Include     : #include "iodefine.h"
 97     *-----------------------------------------------------------------------
 98     * Declaration : void io_init_dma(void *src, void *dst, size_t size, unsigned int mode);
 99     *-----------------------------------------------------------------------
100     * Function    : The DMAC transfers the amount of data specified by “size”
101     *             : from the source address “src” to the destination address “dst.”
102     *             : Auto request mode is used to transfer data.
103     *             : Transfer size and use or non-use of interrupts are specified for the
104     *             : “mode”.
105    *-----------------------------------------------------------------------
106     * Argument    : void *src   : Source address
107     *             : void *dst   : Destination address
108     *             : size_t size : Transfer size (byte)
109     *             : unsigned int mode : Combos of the transfer and the following modes are
110     *             : obtained by logical OR.
111     *             :     DMA_SIZE_BYTE  (0x0000) Byte transfer
112     *             :     DMA_SIZE_WORD  (0x0001) Word transfer
113     *             :     DMA_SIZE_LONG  (0x0002) Longword transfer
114     *             :     DMA_SIZE_LONGx4(0x0003) 16-byte transfer
115     *             :     DMA_INT_DISABLE(0x0000) DMA transfer end interrupt not in use
116     *             :     DMA_INT_ENABLE (0x0010) DMA transfer end interrupt in use
117     *-----------------------------------------------------------------------
118     * Return Value: void
119     *-----------------------------------------------------------------------
120     * Notice       : Operation is not guaranteed when the source/destination address is not
121     *              : on a boundary corresponding to the transfer size.
122     *              : If interrupts are to be used, the interrupt routines must be registered.
123     *""FUNC COMMENT END""************************************************/
124    void io_init_dma(void *src, void *dst, size_t size, unsigned int mode)
125    {
126        unsigned int ts;
127        unsigned long ie;
128
129        ts = mode & 0x3u;
130        ie = (mode & 0x00f0u ) >> 4u;
131
132        /* ==== Setting of DMAC ==== */
133        /* ==== Setting of power down mode ==== */
134        STB.CR2.BIT._DMAC = 0x0;        /* Clear the DMAC module standby mode */
135
136        /* ---- DMA Channel Control Registers(CHCR) ---- */
137        DMAC0.CHCR.BIT.DE = 0ul;        /* DMA disable */
138
139        /* ---- DMA Source Address Registers(SAR) ---- */
140        DMAC0.SAR = (void *)src;
141
142        /* ---- DMA Destination Address Registers(DAR) ---- */
143        DMAC0.DAR = (void *)dst;
```

4. Sample Program Listing: main.c (4)

```
143         /* ---- DMA Transfer Count Registers(DMATCR) ---- */
144         switch(ts){
145         case DMA_SIZE_BYTE:
146             DMAC0.DMATCR = size;             /* Specify transfer count (1/1) */
147             DMAC0.RDMATCR = size;
148             break;
149         case DMA_SIZE_WORD:
150             DMAC0.DMATCR = size >> 1u;        /* Specify transfer count (1/2) */
151             DMAC0.RDMATCR = size >> 1u;
152             break;
153         case DMA_SIZE_LONG:
154             DMAC0.DMATCR = size >> 2u;        /* Specify transfer count (1/4) */
155             DMAC0.RDMATCR = size >> 2u;
156             break;
157         case DMA_SIZE_LONGx4:
158             DMAC0.DMATCR = size >> 4u;        /* Specify transfer count (1/16) */
159             DMAC0.RDMATCR = size >> 4u;
160             break;
161         default:
162             break;
163         }
164         /* ---- DMA Channel Control Registers(CHCR) ---- */
165         DMAC0.CHCR.LONG = 0x00005400ul | (ts << 3u) | (ie << 2u) ;
166                               /* Destination address is incremented */
167                               /* Source address is incremented      */
168                               /* Auto request                       */
169                               /* Cycle steal mode                   */
170                               /* Transfer Size : Longword unit      */
171
172         /* ---- DMA Operation Register(DMAOR) ---- */
173         DMAC.DMAOR.WORD &= 0xfff9u;     /* AE,NMIF clear */
174
175         if(DMAC.DMAOR.BIT.DME == 0ul){  /* DMA Master Enable */
176             DMAC.DMAOR.BIT.DME = 1ul;
177         }
178     }
180
```

5. Sample Program Listing: main.c (5)

```
/*""FUNC COMMENT""*************************************************
 * Outline     : DMAC Activation
 *-----------------------------------------------------------------
 * Include     : #include "iodefine.h"
 *-----------------------------------------------------------------
 * Declaration : void io_dma_enable(void);
 *-----------------------------------------------------------------
 * Function    : Performs DMA transfer
 *-----------------------------------------------------------------
 * Argument    : void
 *-----------------------------------------------------------------
 * Return Value: void
 *-----------------------------------------------------------------
 * Notice      :
 *""FUNC COMMENT END""*************************************************/
void io_dma_enable(void)
{
    /* ---- DMA start ---- */
    DMAC0.CHCR.BIT.DE = 1ul;    /* DMA enable */
}
/*""FUNC COMMENT""*************************************************
 * Outline     : DMAC Stop
 *-----------------------------------------------------------------
 * Include     : #include "iodefine.h"
 *-----------------------------------------------------------------
 * Declaration : void io_dma_stop(void);
 *-----------------------------------------------------------------
 * Function    : Checks whether the transfer is completed and stops the DMA transfer.
 *-----------------------------------------------------------------
 * Argument    : void
 *-----------------------------------------------------------------
 * Return Value: void
 *-----------------------------------------------------------------
 * Notice      :
 *""FUNC COMMENT END""*************************************************/
void io_dma_stop(void)
{
    /* Transmission end detection */;
    while(DMAC0.CHCR.BIT.TE == 0ul){
        /* wait TE bit set */
    }
    /* ---- DMA stop ---- */
    DMAC0.CHCR.BIT.DE = 0ul;    /* DMA disable */
}

/* End of File */
```

4. Documents for Reference

- Software Manual
  SH-2A, SH2A-FPU Software Manual
  The most up-to-date version of this document is available on the Renesas Technology Website.
- Hardware Manual
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