Application Circuit to Generate Plus and Minus Supplies Using the ISL97701 Boost Regulator

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Introduction

This application note will discuss a method to combine the operation of a boost regulator and a negative voltage converter. The circuit described will generate both a positive and a negative supply from a single low voltage supply. The circuit in Figure 5 shows the standard ISL97701 application circuit for a +20V supply along with two ISL28107 op amps, two diodes and two capacitors to generate a well regulated -20V supply.

Understanding the Boost Topology

Before we add the additional circuitry to generate the negative supply, it is important to understand how the boost convertor produces an output voltage that is always greater than the input voltage. In order to do this, we analyze the boost circuits in Figure 1 and the current waveforms in Figure 2. For this analysis, we account for all the losses in the charging and discharging loops in our equations. This should help to give a complete understanding of the circuit.

However, the ISL97701's output voltage is not dependent upon any losses in the circuit. This is because all the losses are inside the circuit's feedback loop of the ISL97701, and are automatically accounted for. The output voltage is defined from the feedback resistor network shown in Figure 5 and calculated in Equation 1, where V_{refFB} is the internal reference voltage of the ISL97701.

$$V_{OUT} = V_{refFB} \bullet (R_1 + R_2) / R_2$$

$$V_{OUT} = 1.15V \bullet (R_1 + R_2) / R_2 \qquad \text{(EQ. 1)}$$

Positive Supply

Figure 1A shows the basic boost converter circuit. During one switching cycle, the transistor Q_1 turns on and turns off. During the time Q_1 is on, the inductor L_1 is placed in series with the V_{IN} supply through the ISL97701's integrated boost FET (Q_1). The diode D_1 is reversed biased and the circuit reduces to that shown in Figure 1B. The voltage across the boost inductor (L_1) is equal to V_{IN} - (V_{DS} + I_{L1} x R_{L1}) and the current ramps up linearly in inductor L_1 to a peak value at time DT. The peak inductor current ($\Delta I_{L1(on)}$) is calculated in Equation 3 and shown graphically in Figure 1B. Any load requirements during this phase are supplied by the output capacitor C_1.

$$V_L = L \times \frac{di_L}{dt} \Rightarrow i_{Lpk} = \frac{V_L}{L} \int_{T_0}^{DT} dt \qquad \text{(EQ. 2)}$$

$$\Delta I_{L1(on)} = \frac{V_{IN} - (V_{DS} + I_{L1} \times R_{L1})}{L} \times DT \qquad \text{(EQ. 3)}$$

When Q_1 turns off, since the current in an inductor cannot change instantaneously, the voltage in L_1 reverses and the circuit becomes that shown in Figure 1C. Now the no-dot end of L_1 is positive with respect to the dot end and D_1 becomes forward biased. Since the dot end is at V_{IN}, L_1 delivers its stored energy to C_1 and charges it up to a higher voltage than V_{IN}. This energy supplies the load current and replenishes the charge drained away from C_1. During this time, energy is also supplied to the load from V_{IN}. The voltage applied to the dot end of the inductor is (V_{IN} - I_{L1} x R_{L1}). The voltage applied to the no-dot end of L_1 is now the output voltage, V_O, plus the diode forward voltage V_D. The voltage across the inductor during the off-state is ((V_O + V_{D1} + I_{L1} x R_{L1}) - V_{IN}). The inductor current during the off-time of the switch (T-DT) is calculated in Equation 4 and shown graphically in Figure 1C.

$$\Delta I_{L1(off)} = \frac{(V_O + V_{D1} + I_{L1} \times R_{L1}) - V_{IN}}{L} \times (T - DT) \qquad \text{(EQ. 4)}$$

In steady-state conditions, the current increases during the on-time of the switch and decreases during the off-time of the switch, reference Figure 2. Both on-time and off-time currents are equal to prevent the inductor core from saturating. Setting both currents equal to each other and solving for V_O results in the continuous conduction mode boost voltage shown in Equation 5.

$$V_O = \frac{V_{IN} - I_L \times R_L}{1 - D} - V_{D1} - V_{DS} \times \frac{D}{1 - D} \qquad \text{(EQ. 5)}$$

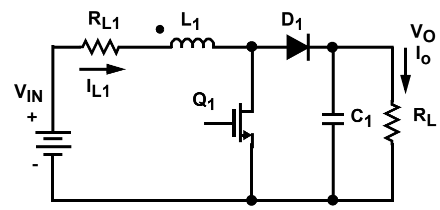

FIGURE 1A.

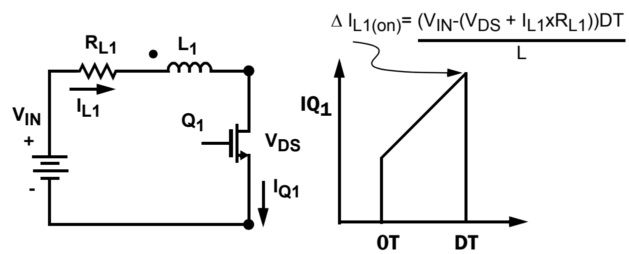

FIGURE 1B.

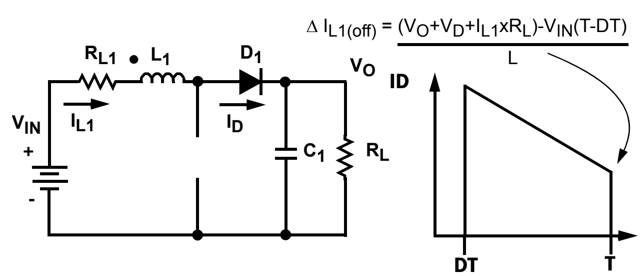

FIGURE 1C.

FIGURE 1. BASIC BOOST TOPOLOGY

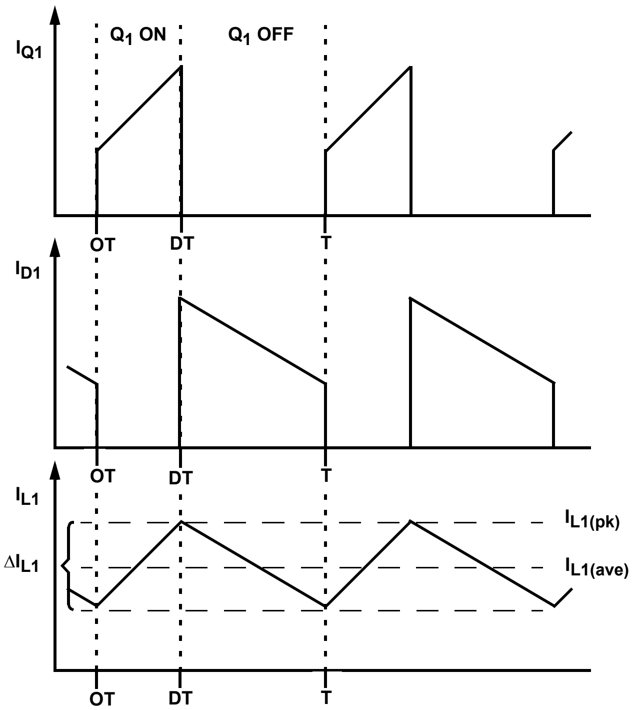

FIGURE 2. INDUCTOR, TRANSISTOR AND DIODE CURRENTS

The duty cycle "D" in Equation 5 is determined by setting the losses in Equation 5 (I_{L1} x R_{L1}, V_{D1}, V_{DS}) to zero because they are within the feedback loop of the ISL97701. The ISL97701 varies the duty cycle continuously to keep V_O constant, regardless of the conduction losses as a function of load current. With the losses set to zero, Equation 5 reduces to Equation 6. This results in the value for the Duty Cycle as shown in Equation 7.

$$\frac{V_O}{V_{IN}} = \frac{1}{1-D} \tag{EQ. 6}$$

$$D = 1 - \frac{V_{IN}}{V_O} \tag{EQ. 7}$$

Inductor Selection

The inductor selection determines the output ripple voltage, transient response, output current capability, and efficiency. Its selection depends on the input voltage, peak inductor current, output voltage, switching frequency, and maximum output current. When choosing an inductor, make sure the saturation current of the inductor is greater than the I_{PEAK} of the circuit. Likewise, the transistor should be able to handle peak current greater than I_{PEAK}. The peak inductor current is shown in Figure 3 and can be calculated using Equation 11.

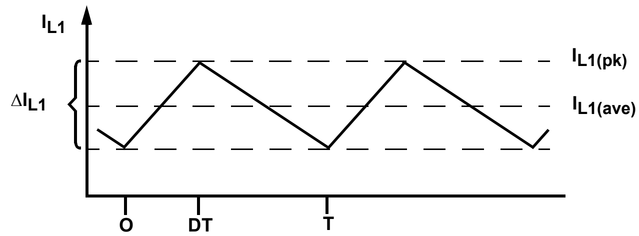

FIGURE 3. INDUCTOR AVERAGE AND PEAK CURRENTS

From Figure 3, it can be seen that the peak inductor current $I_{L1(PK)}$ is equal to the average inductor current $I_{L1(ave)}$ plus one half the ΔI_{L1} current, as shown in Equation 8.

$$I_{L1(PEAK)} = I_{L1(AVE)} + \frac{1}{2}\Delta I_{L1(on)} \tag{EQ. 8}$$

The average power IN is equal to the average power OUT divided by the efficiency of the circuit, as shown in Equation 9.

$$V_{IN} \times I_{L1(AVE)} = \frac{V_O \times I_O}{Eff} \tag{EQ. 9}$$

Where Eff is equal to the efficiency of the ISL97701 boost regulator.

Therefore, the average inductor current is equal to the output current times the gain of the boost regulator as shown in Equation 10.

$$I_{L1(AVE)} = \frac{V_O \times I_O}{V_{IN} \times Eff} \tag{EQ. 10}$$

$\Delta I_{L1(on)}$ was defined in Equation 3 and the duty cycle "D" in Equation 7. Substituting Equation 7 into Equation 3 and adding it to Equation 10 results in Equation 11. Equation 11 gives the inductor's peak current in terms of input voltage, output voltage, switching frequency, and maximum output current (again, the losses due to V_{DS} and I_{L1} x R_{L1} are not included because they are inside the feedback loop of the ISL97701).

$$I_{L(PEAK)} = \frac{V_O \times I_O}{V_{IN} \times Eff} + 1/2 \times \frac{V_{IN} \times (V_O - V_{IN})}{L \times V_O \times FREQ} \tag{EQ. 11}$$

By rearranging the terms in Equations 11, we can solve for the inductor value using Equation 12.

$$L = \frac{V_{IN}^2 Eff(V_O - V_{IN})}{(I_{PK} V_{IN} Eff - I_O V_O) 2 V_O FREQ} \tag{EQ. 12}$$

Equation 12 is useful for determining the minimum value of L the circuit can handle without exceeding the peak current through the inductor, and therefore, the switch Q_1. The maximum peak current (I_{PEAK}) allowed through Q_1 for safe operation is given in the Electrical Specification table of the ISL97701 data sheet as 1.2A.

Minimum Inductor Value Design Example

Given: V_{IN} = 5V, V_O = 25V, I_O = 35mA, I_{PK} = 1.2A, freq = 1MHz, Eff = 0.85 (Efficiency of 85% from Figure 3 in ISL97701 data sheet).

Equation 12 gives us the boundary condition for the smallest inductor we can have to ensure the peak current through Q_1 is less than the max limit of 1.2A. The minimum inductor value for the given conditions is determined to be 2.0µH.

$$L = \frac{(5V)^2(0.85)(25-5)}{(1.2A(5)(0.85)-35mA(25))2(25)1MHz} = 2.0\mu H \quad \text{(EQ. 13)}$$

Maintaining CCM Design Example

For maximum efficiency, the boost converter needs to be operated in continuous conduction mode (CCM). To maintain continuous conduction mode operation of the boost regulator, the value of $I_{L1(ave)}$ needs to be greater than or equal to $\Delta I_{L1}/2$, reference Figure 3.

$$I_{L1(AVE)} \geq \frac{1}{2}\Delta I_{L1}$$

$$\frac{V_O \times I_O}{V_{IN} \times Eff} \geq 1/2 \times \frac{V_{IN} \times (V_O - V_{IN})}{L \times V_O \times FREQ} \quad \text{(EQ. 14)}$$

Rearranging terms and solving for L results in Equation 15.

$$L \geq 1/2 \times \frac{V_{IN} \times (V_O - V_{IN})}{\frac{V_O \times I_O}{V_{IN} \times Eff} \times V_O \times FREQ} \quad \text{(EQ. 15)}$$

To maintain continuous conduction mode operation, for the given circuit design conditions above, the value of L has to be greater than 9.71µH.

$$L \geq 1/2 \times \frac{5V \times (25V - 5V)}{\frac{25V \times 35mA}{5V \times (0.85)} \times 25V \times 1MHz} \geq 9.71\mu H \quad \text{(EQ. 16)}$$

It should be noted that when there is a light load, the circuit can slip into discontinuous conduction mode, where the inductor becomes fully discharged of its current each cycle. This operation will reduce the overall efficiency of the supply. Using Equation 15 and making the value of the inductor large enough for a given minimum output current will insure continuous conduction mode operation.

Output Capacitor

Low ESR capacitors should be used to minimize the output voltage ripple. Multilayer ceramic capacitors (X5R and X7R) are preferred for the output capacitors because of their lower ESR and small packages. Tantalum capacitors with higher ESR can also be used. The output ripple can be calculated in Equation 17:

$$\Delta V_O = \frac{I_{OUT} \times D}{f_{SW} \times C_1} + I_{OUT} \times ESR \quad \text{(EQ. 17)}$$

For noise sensitive applications, a 0.1µF placed in parallel with the larger output capacitor is recommended to reduce the switching noise.

Negative Supply

The operation of the negative supply is best understood by considering Figure 5. We will start our analysis under steady state conditions (the inductor operating in continuous conduction mode and C_1 is equal to the voltage calculated in Equation 1).

When Q_1 turns off, the inductor voltage flies up turning on D_1 and D_3. Diode D_2 is blocking current flow from C_3. The inductor current now charges both capacitors C_1 and C_2 with the polarity as shown in Figure 5. The voltage on C_2 is equal to the voltage on C_1, plus the forward voltage drop of D_1.

When Q_1 turns on, Diodes D_1 and D_3 are blocking and capacitor C_2 is now in parallel with capacitor C_3 through D_2 (which is now on), reference Figure 4. This connection results in a negative voltage being transferred on to C_3. The voltage transferred to C_3 is equal to the voltage on C_1 as shown in Figure 4 and Equation 18.

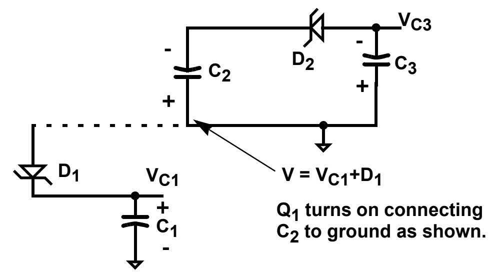

FIGURE 4. CHARGING OF NEGATIVE SUPPLY CAPACITOR C_3

$$(V_{C1} + D_1) - D_2 - V_{C3} = 0$$

$$V_{C1} = V_{C3} \quad \text{(EQ. 18)}$$

The efficiency of the charge transfer between the two capacitors is related to the energy lost during this process. **ENERGY IS LOST ONLY IN THE TRANSFER OF CHARGE BETWEEN CAPACITORS IF A CHANGE IN VOLTAGE OCCURS**. The energy lost is defined in Equation 19:

$$E = \frac{1}{2}C_2({V_1}^2 - {V_2}^2) \quad \text{(EQ. 19)}$$

Where V_1 and V_2 are the voltages on C_2 during the charging and transfer cycles. If the impedances of C_2 and C_3 are relatively high at the 1MHz frequency compared to the value of R_L, there will be substantial difference in the voltages V_1 and V_2. Therefore, it is not only desirable to make C_3 as large as possible to eliminate output voltage ripple, but also to employ a correspondingly large value for C_2 in order to achieve maximum efficiency of operation.

Output Voltage Regulation using Op Amps

The final output voltage regulation is accomplished using two ISL28107 op amps (note: two separate op amps required because of the different supply connections). The voltage developed by the boost converter powers the amplifiers and the output voltage is calculated using Equations 20 and 21.

$$V_{OUT(positive)} = 5V \bullet (R_3 + R_4)/R_3 \quad \text{(EQ. 20)}$$

$$V_{OUT(negative)} = -V_{OUT(positive)} \bullet R_6/R_5 \quad \text{(EQ. 21)}$$

Restriction on Design:

1. For reasonable voltage regulation of the negative supply voltage, the negative supply current needs to be less than or equal to the positive supply current. This is because the control loop for output voltage regulation is around the positive supply voltage only.

$$I_{OUT(positive)} \geq I_{OUT(negative)} \quad \text{(EQ. 22)}$$

2. The maximum output current of the circuit shown in Figure 5 is limited by the maximum output current of the ISL28107 op amps, which is 40mA.
3. The ISL97701 is optimized to work best for a small range of inductors. The slope compensation ramp generator, inside the ISL97701, is optimized for inductor values between the range of 4.7µH to 15µH and output currents between 25mA to 125mA. The circuit will work for inductor values outside this range, as long as the maximum I_{PEAK} current is not exceeded (Equation 12). The only drawback will be a reduction in the efficiency of the circuit. The percent efficiency could drop from the 80's to the 60's as the operation goes from continuous conduction mode to discontinuous conduction mode. Reference the ISL97701 data sheet for additional information on performance of the Boost Regulator.
4. To obtain output currents higher than 40mA, the user could:
   - Operate the circuit without the op amps (at the cost of output voltage regulation) by connecting directly to C_1 and C_3
   - Or replace the op amps with ones with higher output current drive capability
5. The accuracy of the output voltage is highly dependent on the input voltage source. Using a well regulated voltage source is recommended.

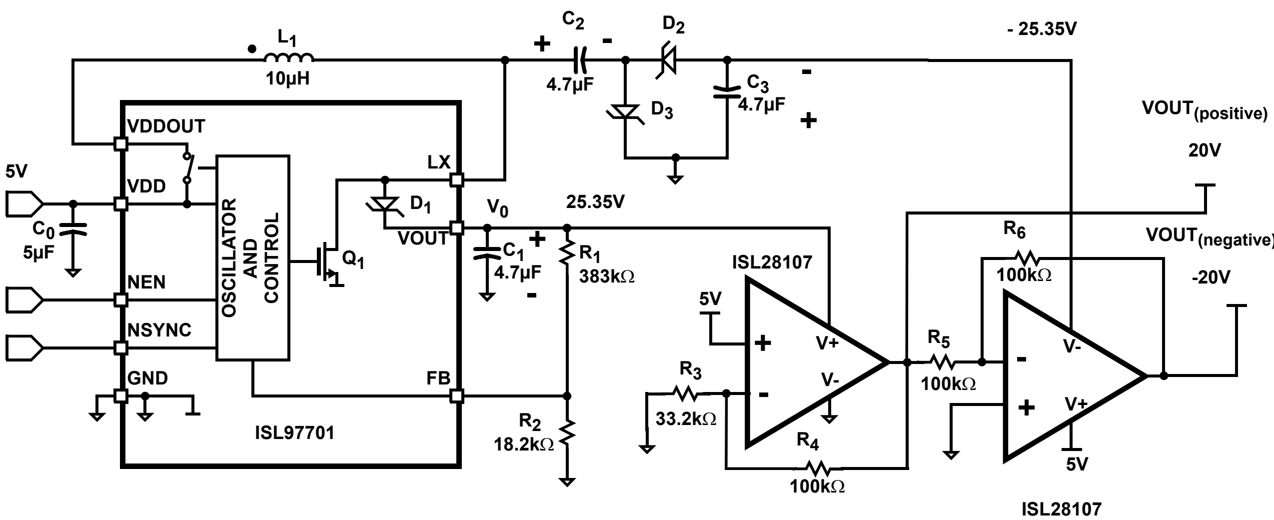

FIGURE 5. REFERENCE DESIGN TO GENERATE A POSITIVE AND NEGATIVE SUPPLY

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