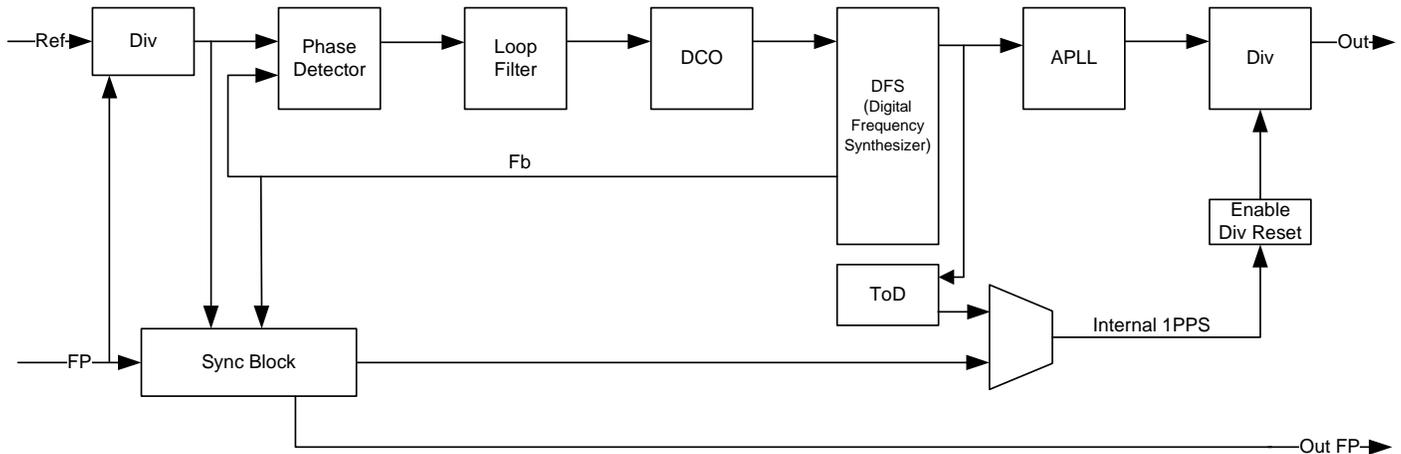


## Introduction

The IDT 82P338XX/9XX Synchronization Management Unit (SMU) for IEEE 1588 and Synchronous Ethernet (SyncE) provides tools to manage timing references. It has several different modes to align the output clocks, to control the skew, clock sources and timing paths for IEEE 1588 / Precision Time Protocol (PTP) and Synchronous Ethernet (SyncE) based clocks. This document focuses on clock alignment with a SYNC input.

Figure 1. 82P338XX/9XX Block Diagram



## SYNC Input Signals

Any of the 82P338XX/9XX clock inputs can be configured as a SYNC input. The SYNC input must be associated with a reference clock(s). The IN{3:14}\_SYNC\_SEL{3:0} bits associates a SYNC input with the applicable reference clock.

There is no specific setting to determination if the SYNC input is a Framing Pulse (FP) or Synchronizing Pulse (SP). It's determined on the overall configuration of the SYNC input, as described in this section, and understanding how the SYNC input is being used to generate the SYNC output and the clock outputs, as described in the following sections.

Support for the SYNC input must be set via the DPLL{1:2}\_EXTSYNC\_EN bit (default b'0, or disabled). All SYNC inputs must have the same frequency (1PPS, 2kHz, 4kHz or 8kHz), matching the setting in the DPLL{1:2}\_SYNC\_FREQ[1:0] bits. If the SYNC input is to be used solely as a SYNC, then the SYNC input should be disabled as a clock source for the DPLL; this is done by setting DPLL{1:2}\_IN{1:14}\_PRIORITY{3:0} to b'0000 (input is disabled for auto reference selection).

By default, the falling edge of the SYNC input is expected to be aligned with the rising edge of the input reference clock (see Figure 2). The rising edge of the SYNC input can be set to align with the rising edge of the input reference clock by setting the DPLL{1:2}\_SYNC\_EDGE bit to b'1 (see Figure 3). The phase relationship of the SYNC input to the reference clock can be in the range of 0.5UI early to 1UI late. How the SYNC input is sampled is described in the next section.

Figure 2. SYNC Input - Falling Edge (Default)

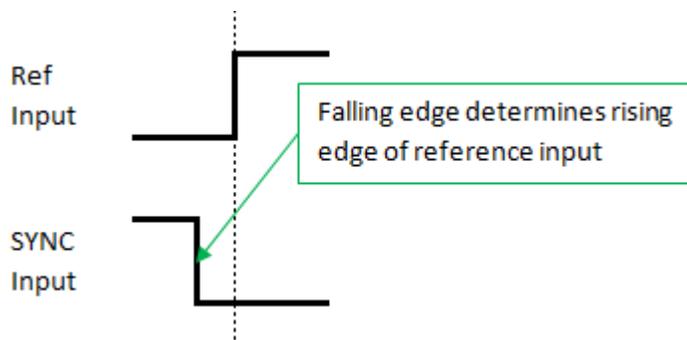
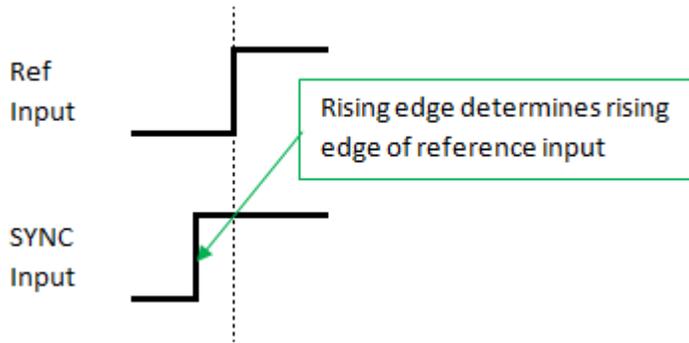


Figure 3. SYNC Input – Rising Edge



The frequency of the output clocks that are synchronous to the SYNC input must be equal to or higher than the associated reference clock (post divided, if applicable). If it is desired to have lower frequency output clocks, then a re-alignment must be triggered on the initial LOCK of the DPLL or when the DPLL comes out of HOLDOVER. Refer to [Alignment of Output Dividers](#) for details.

The SYNC input is also used to generate the FFrame SYNC (FRSYNC) or Multi-FFrame SYNC (MFRSYNC) output signal; refer to [SYNC Output Signals](#) for details.

### Sampling of SYNC input

The sampling of the SYNC input is determined by the phase offset programmed via IN{1:14}\_SYNC\_PHASE[1:0] bits, and illustrated in [Figure 4](#) through [Figure 7](#). Typically, the "On Target" and "1 UI Late" options are used for SP applications; and the "0.5 UI Early" and "0.5UI Late" options are used for FP applications.

Figure 4. SYNC Input Sampling – On Target (Default)

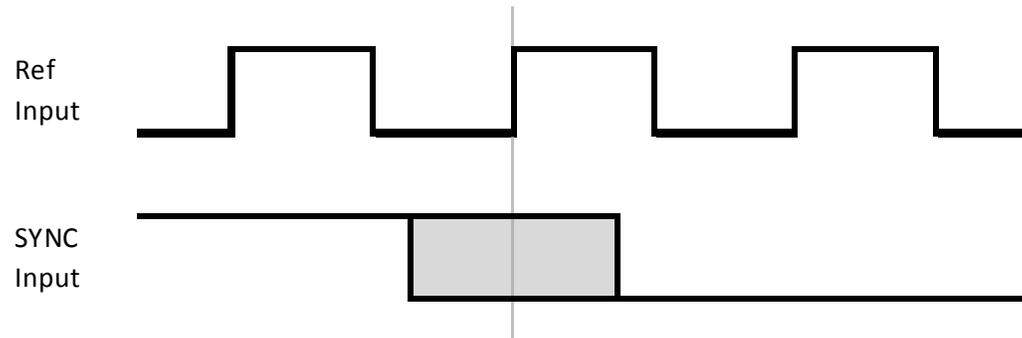


Figure 5. SYNC Input Sampling – 0.5 UI Early

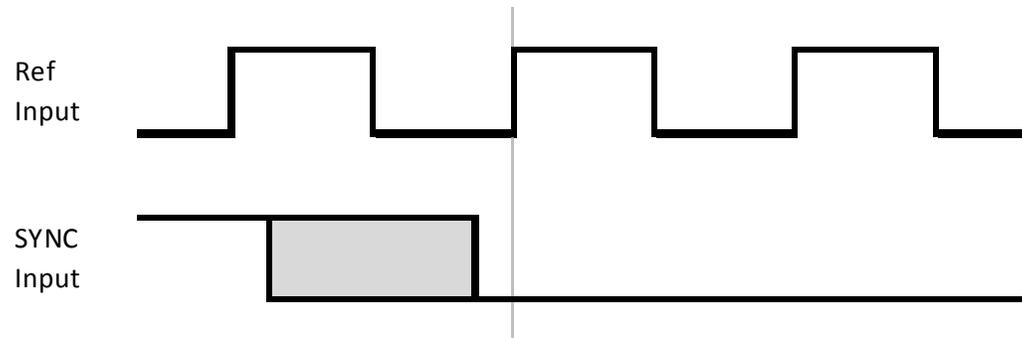


Figure 6. SYNC Input Sampling - 0.5 UI Late

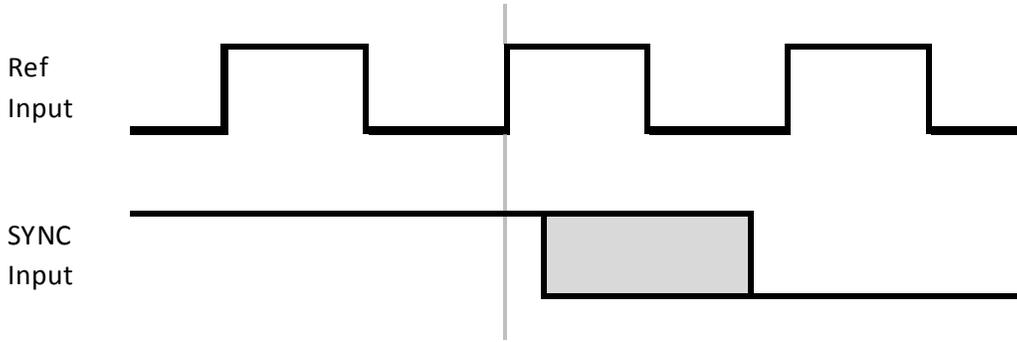
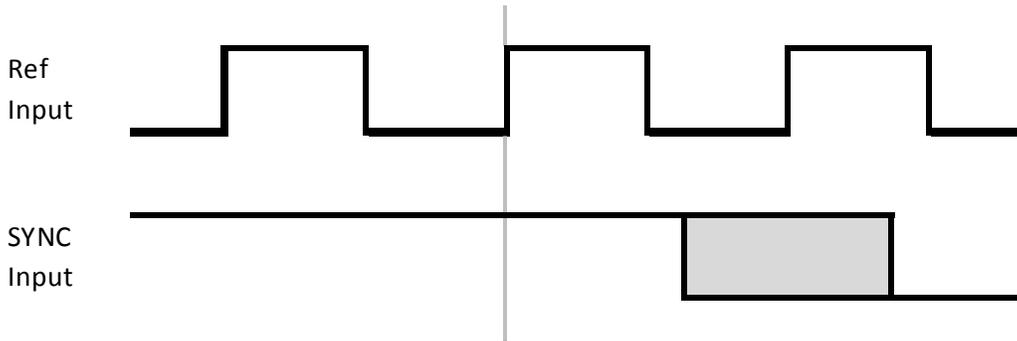


Figure 7. SYNC Input Sampling - 1 UI Late



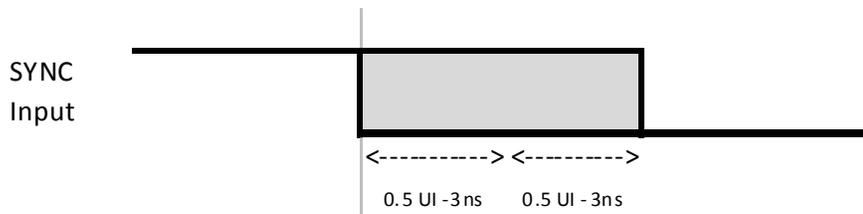
When the SYNC input is sampled by the input reference, the SYNC input must be within a valid window, as illustrated in the figures above. The sampling window size is captured in the table below.

Table 1. SYNC Input Sampling Window Size

Parameter	Description	Minimum	Typical	Maximum
$t_w$	SYNC input sampling window size			$1UI^{[a]} - 6ns$

[a] A UI is in reference to the DPLL's PFD frequency configuration.

Figure 8. SYNC Input Sampling Window Size - Falling Edge (Default)



How the phase offset affects the SYNC output and/or the output clocks is captured in section [SYNC Output Signals](#).

### Alignment of Fractional Input Divider

If an input reference clock has been divided down, then the divided clock edge would be in unknown position with respect to original reference clock. For example, if we divide the clock by 6, then the resulting clock could align to any of 6 input clock cycles. To ensure that the divided down reference clock is always in the same position, the input fractional dividers are synchronized by the SYNC input.

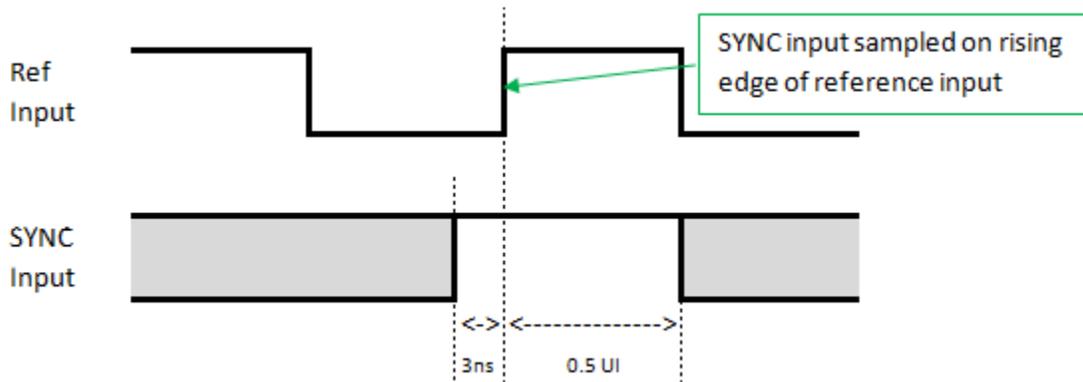
When the input reference is being divided down by the fractional divider, the SYNC input must meet specific setup/hold timing in relationship to the reference input. This setup/hold time is independent of the SYNC input sampling described previously, but does affect the SYNC input sampling with the resulting divided down reference input. The setup and hold times are captured in the table below.

Table 2. Input Fractional Divider SYNC Input Setup & Hold Times

Parameter	Description	Minimum	Typical	Maximum	Units
$t_S$	SYNC input to IN{3:14} Setup time	3			ns
$t_H$	SYNC input to IN{3:14} Hold time	0.5			UI <sup>[a]</sup>

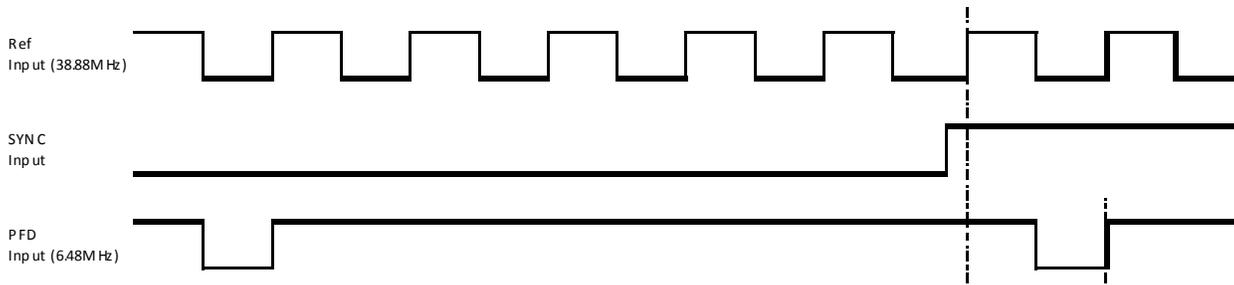
[a] A UI is in reference to the DPLL's PFD frequency configuration.

Figure 9. Input Fractional Divider SYNC Input Setup/Hold



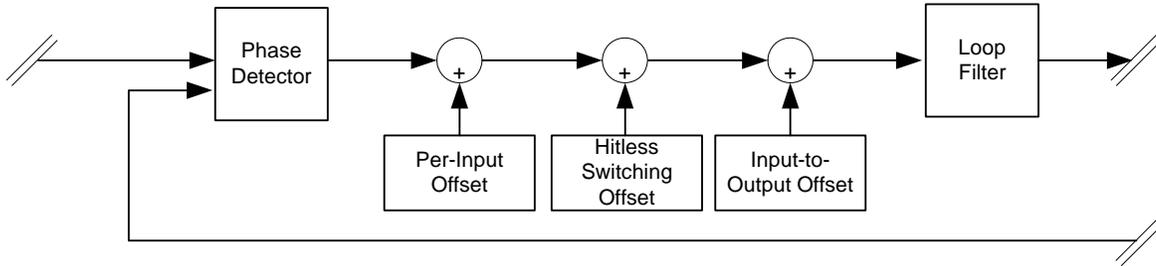
When using the fractional divider, the SYNC input must be configured to use the rising edge, by setting DPLL{1:2}\_SYNC\_EDGE bit to b'1 (as illustrated in Figure 9). The synchronizing of the input fractional dividers will occur on the next cycle of the original input reference clock. This means that a static 1UI offset needs to be accounted for. For example, if a 38.88MHz clock is divided down to 6.48MHz, the static offset would be approximately 25.72ns. This is illustrated in Figure 10 below.

Figure 10. Fractional Input Divider Example – 38.88MHz divided down to 6.48MHz



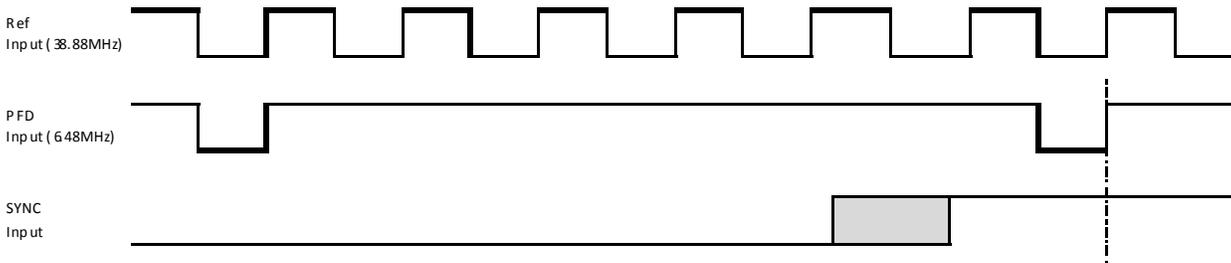
The static 1UI offset can be accounted for using the input skew adjustment registers. This adjustment is done post-phase detector, thus, will affect the alignment of the SYNC output and output clocks.

Figure 11. Input Skew Control



The sampling of the SYNC input will now be based on the divided down clock. However, with the setup/hold requirements for the input divider, the sampling range is limited on the SYNC input, as shown in Figure 12.

Figure 12. Fractional Input Divider - SYNC Input Sampling



As illustrated in Figure 12, the SYNC input will always appear to be 'early' in relationship with the divided down clock. For this reason, it is recommended to set the phase offset for the SYNC input to "0.5UI early" when using the fractional input divider to account for this.

## SYNC Output Signals

From a high level, it can be said that a SYNC output is a re-sampled version of the SYNC input. The SYNC output aligns to the first edge of the associated reference clock that occurs after the edge of the SYNC input.

Both DPLL1 and DPLL2 can generate FFrame SYNC (FRSYNC) and Multi-FFrame SYNC (MFRSYNC) signals. The selection of which signal is assigned to the associated FRSYNC and MFRSYNC output pins is controlled by the FR\_PATH\_SEL bit and MFR\_PATH\_SEL bit, respectively.

Support for the FRSYNC output and MFRSYNC output is controlled via the FR\_PDN bit & MFR\_PDN bit, respectively. By default, the FRSYNC output is 8kHz and the MFRSYNC output is 2kHz. If the FRSYNC output is to be used as a SP (1PPS), then the output should be changed via DPLL{1:2}\_8K\_1PPS\_SEL bit. If the MFRSYNC output is to be used as a SP (1PPS), then the output should be changed via DPLL{1:2}\_2K\_1PPS\_SEL bit.

By default, the falling edge of the [M]FRSYNC output is aligned with the rising edge of the input reference clock (see Figure 13). The [M]FRSYNC output can be inverted by setting the DPLL{1:2}\_8K\_1PPS\_INV bit or DPLL{1:2}\_2K\_1PPS\_INV bit to b'1. The input-to-output delay of the SYNC output to the input reference clock edge is captured in the data sheet.

Figure 13. SYNC Output Alignment – Falling Edge (Default)

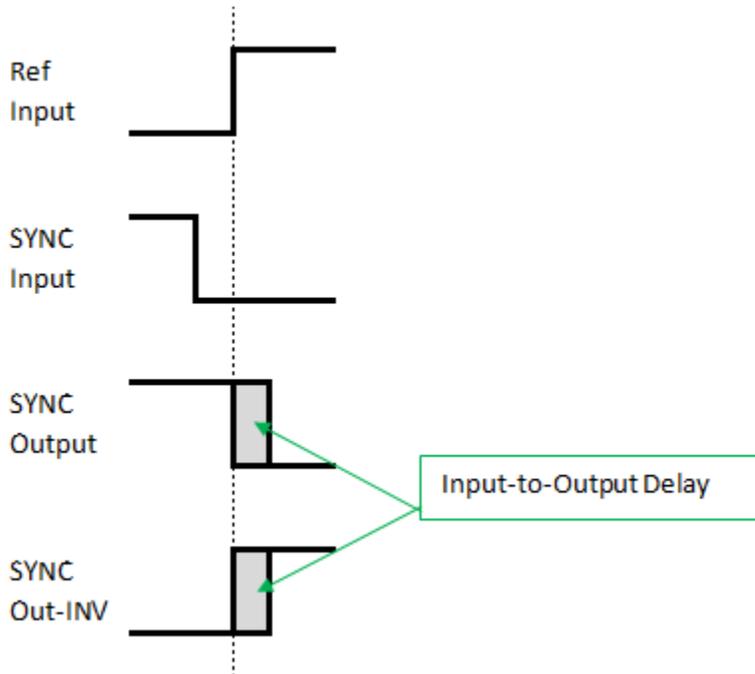
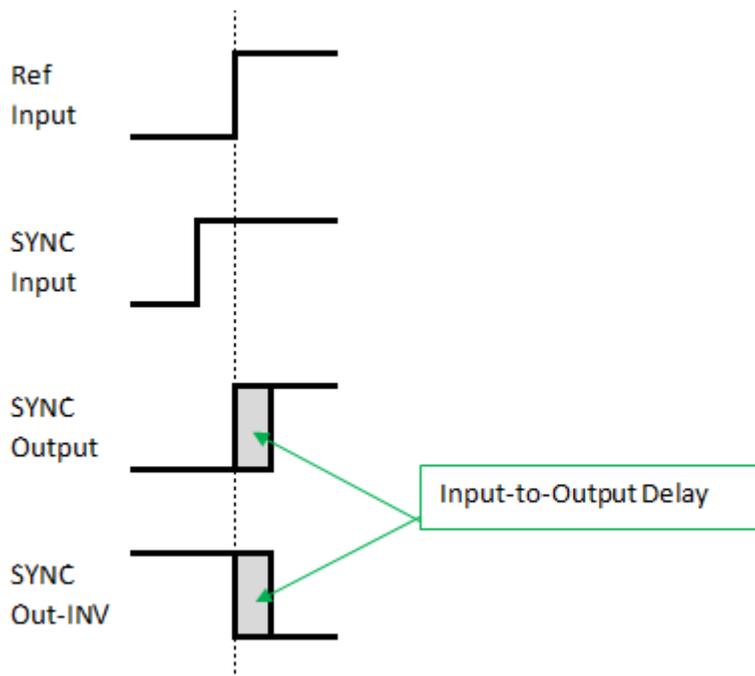


Figure 14. SYNC Output Alignment – Rising Edge



Based on the SYNC input sampling configuration (IN{1:14}\_SYNC\_PHASE[1:0] bits), the SYNC output and clock outputs will have different phase relationships with the rising edge of the reference input, as captured in [Figure 15](#) through [Figure 18](#). The input-to-output delay of the SYNC output and the clock outputs to the input reference clock is captured in the data sheet.

Figure 15. SYNC Output Alignment - On Target (Default)

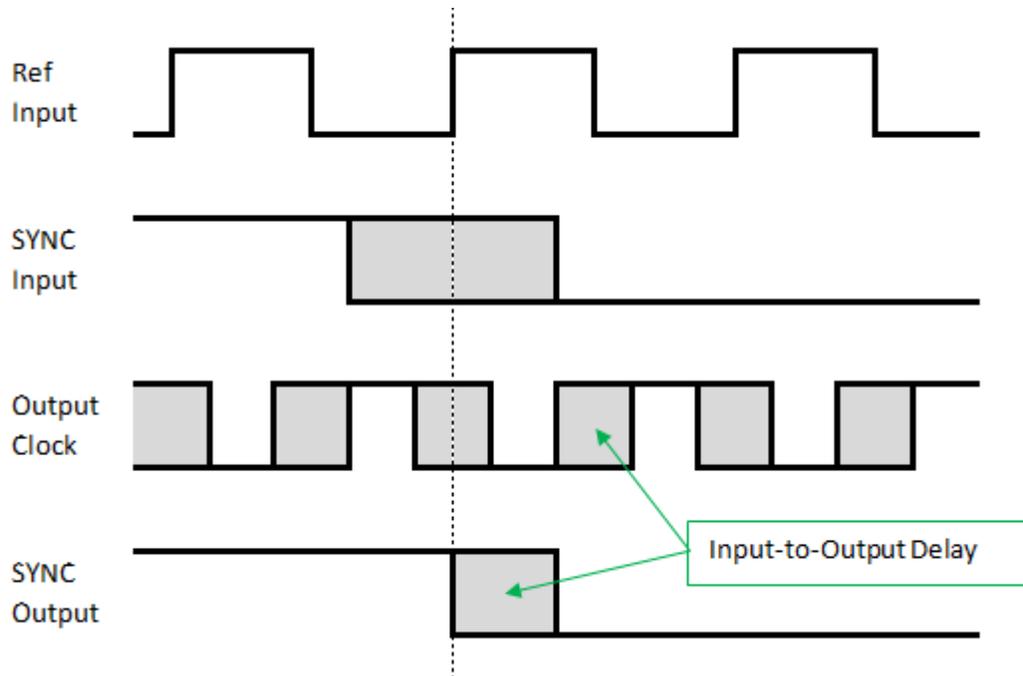


Figure 16. SYNC Output Alignment - 0.5 UI Early

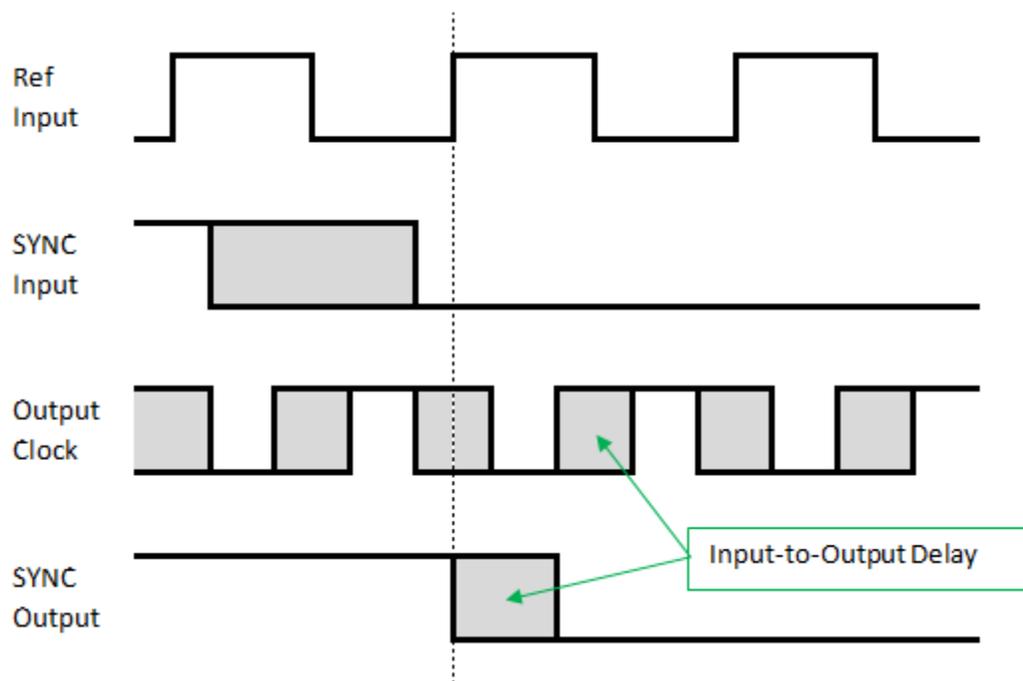


Figure 17. SYNC Output Alignment - 0.5 UI Late

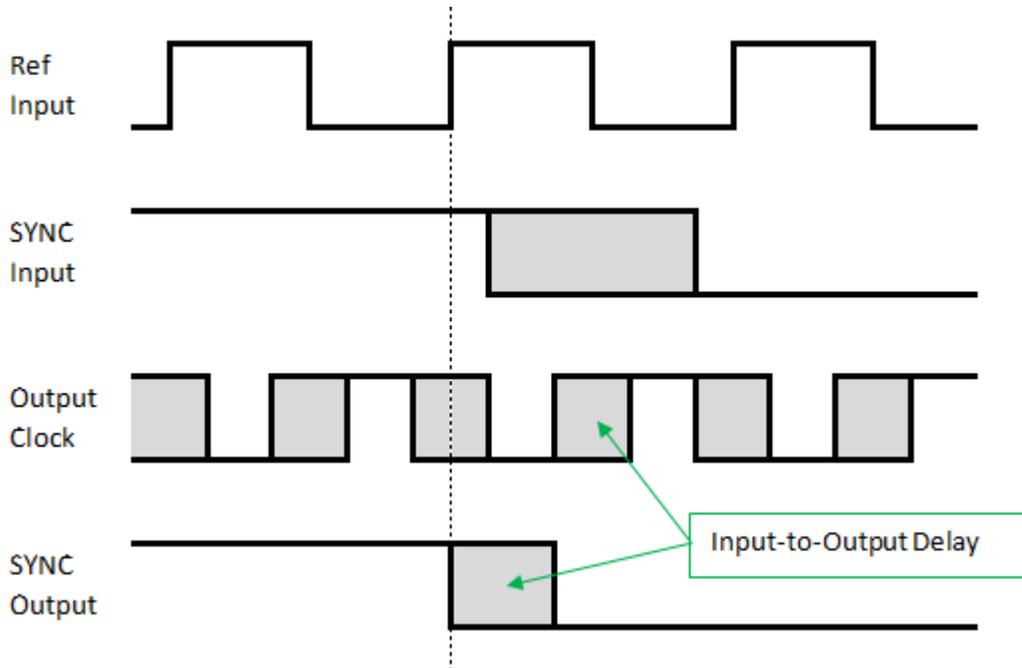
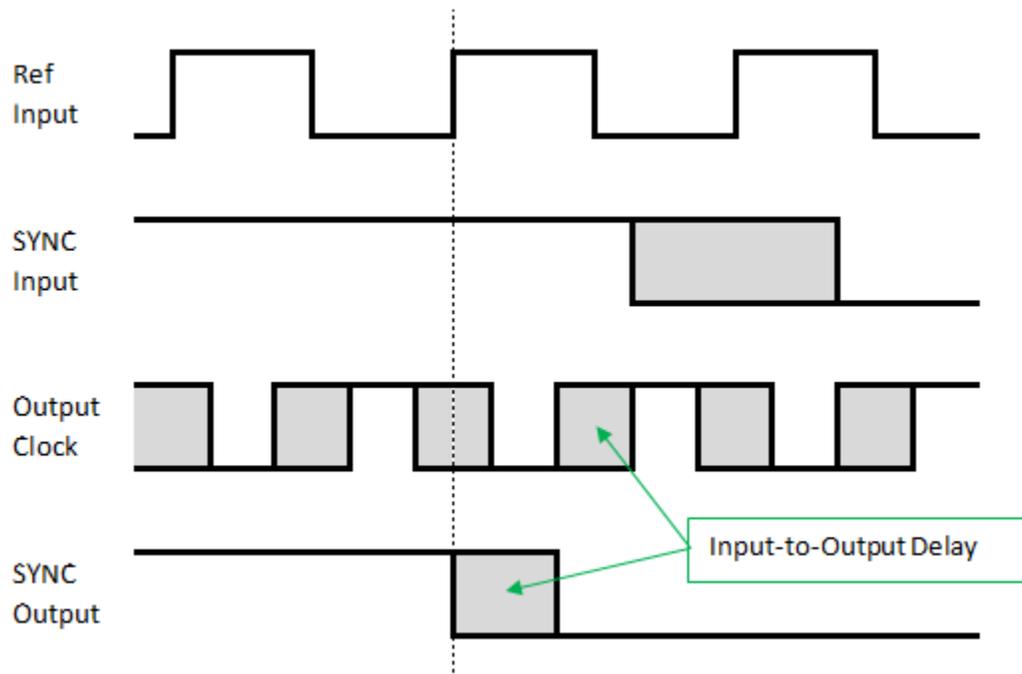


Figure 18. SYNC Output Alignment - 1 UI Late



The SYNC output is a 50/50 clock by default. The FRSYNC output can be changed to a pulse based on the UI of OUT1 via DPLL{1:2}\_FRSYNC\_PULSE bit. In this case, OUT1 must be a clock coming from the same DPLL as the FRSYNC signal. The MFRSYNC output can be changed to a pulse based on the UI of OUT8<sup>[1]</sup> via DPLL{1:2}\_MFRSYNC\_PULSE bit. In this case, OUT8 must be a clock coming from the same DPLL as the MFRSYNC signal.

[1] 82P33x31/x41 devices do not have control of OUT8, as it is internally routed to APLL3. This means that the MFSYNC output cannot be pulsed.

By default, the SYNC output pulse is aligned with the rising edge of OUT1/8 output reference clock. The SYNC output pulse can be set to align with the falling edge of OUT1/8 output reference clock by setting the DPLL{1:2}\_FR\_MFRSYNC\_PUL\_POS bit to b'1.

## Alignment of Output Dividers

The output clocks are aligned with the rising edge of the input reference clock. The output clocks can be inverted by setting the OUT{1:8}\_INV bit. The input-to-output delay of the output clocks to the input reference clock edge is captured in the data sheet.

Although the goal of a SYNC input is to align all output clock edge with a common edge of the input reference clock, it would be undesirable to continuously reset the output dividers. For this reason, the output dividers were designed to only be reset during an input reference clock switch. Each of the clock outputs has the ability to disable the synchronization of the output dividers; controlled via OUT{1:8}\_SYNC\_EN bit. The resetting of the output dividers is automatically controlled by the device; and is triggered within the first 2 seconds of a reference input switch. The alignment of the output clocks to the input reference clock is captured in the previous [Figure 15](#) through [Figure 18](#).

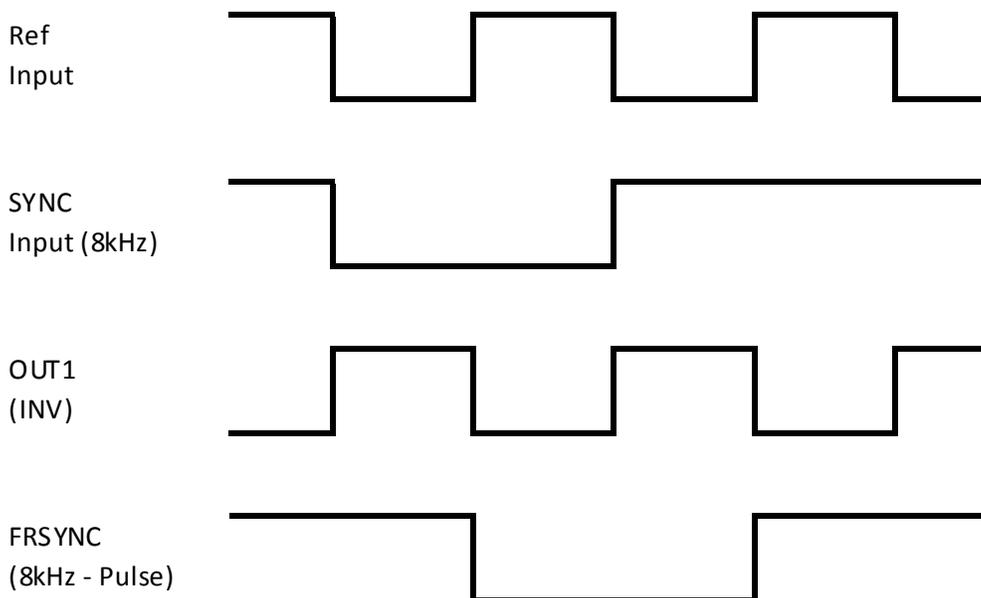
This resetting of the output dividers works for most cases, unless there are output clocks less than the frequency of the input reference clock (post-divided, if applicable). In this case, during initial acquiring of an input reference clock (i.e. coming out of FREERUN or HOLDOVER), the divider reset must be manually triggered to re-align the outputs of the lower frequency clocks. Details of this are captured in the document "Procedure to align output clocks with input Frame Pulse for 82P338xx/9xx".

## Application Examples

### Using SYNC input as a Frame Pulse (FP)

As a FP, the SYNC input is "framing" the input reference clock. This means that the pulse width is typically 1UI of the input reference clock. Because it is a framing pulse, the input reference clock should not be divided down internally (i.e. direct to PFD). The reason is that dividing the clock changes the period from the original reference, which is was used to determine the framing pulse width.

Figure 19. FP Example – 0.5 UI Early

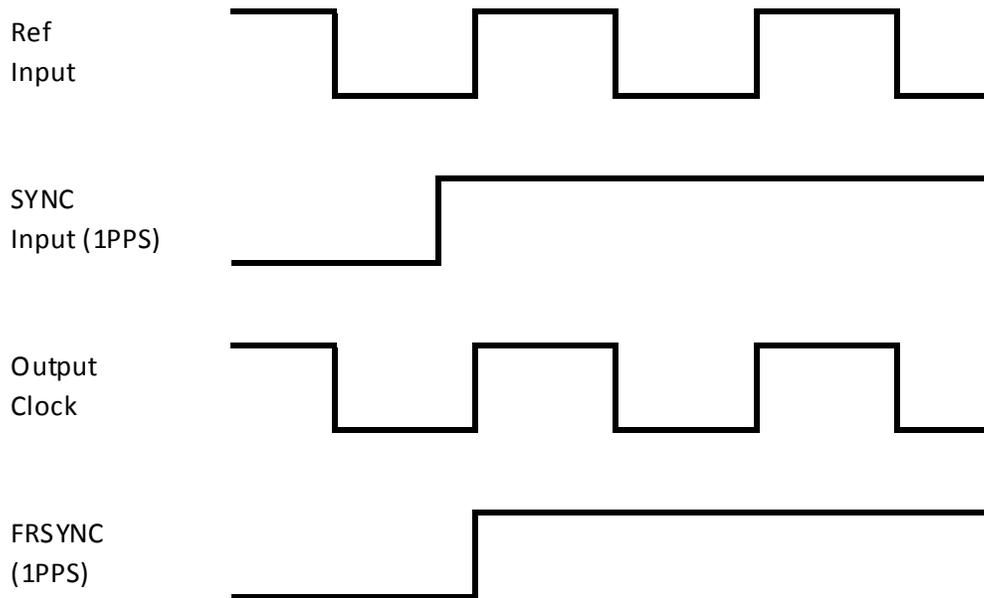


By default, the FP will only be used once the DPLL has locked to the reference input clock. This is controlled by the DPLL{1:2}\_AUTO\_EXTSYNC\_EN bit when DPLL{1:2}\_EXTSYNC\_EN = b'1 (enabled). In a MS/SL configuration, the SLAVE device must set DPLL{1:2}\_SYNC\_BYPASS bit must be set to b'1 for the slave to use the SYNC input.

## Using SYNC input as a Sync Pulse (SP)

As a SP, the SYNC input is identifying an edge of the input reference clock to align all clocks to. Because the SP is synchronous to the reference clock, the input clock can be divided down internally with the fractional input divider<sup>[1]</sup>. The output dividers are also aligned by the SP to the reference input edge. Although 1PPS is the most common SP, 2k/4k/8k can be used as well. In either case, the pulse width must be wide enough to support a divided down reference clock (typically in  $\mu$ s or ms).

Figure 20. SP Example - On Target

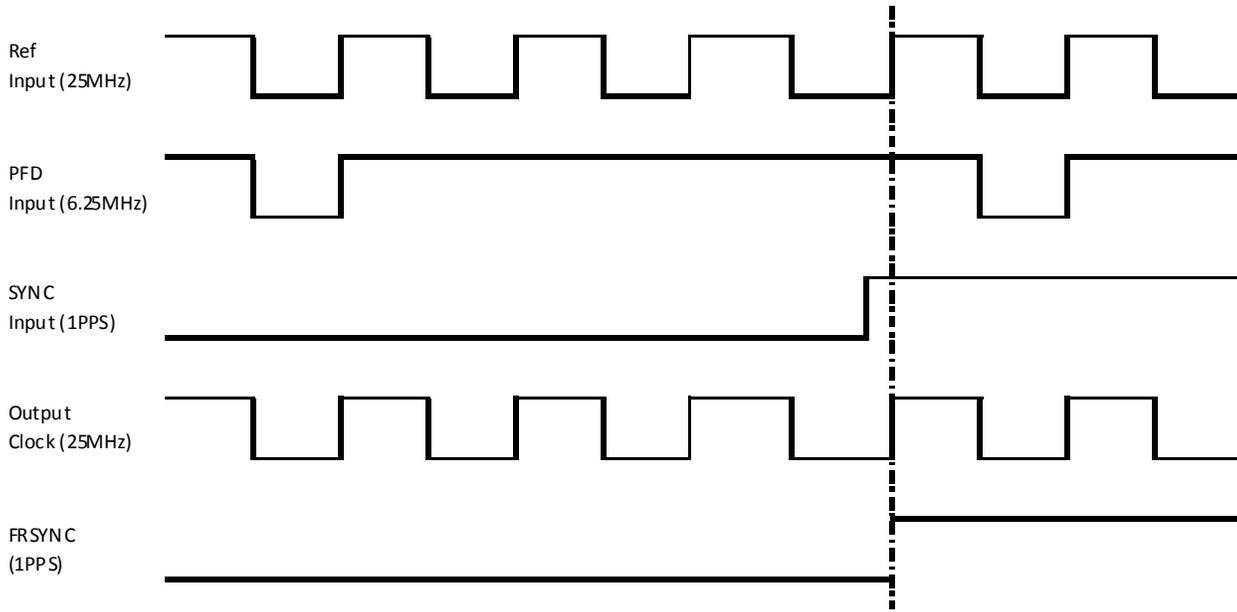


Since the input and output dividers are aligned to the SYNC input, it is recommended to disable `DPLL{1:2}_AUTO_EXTSYNC_EN` by setting to b'0 (always use SYNC input). In a MS/SL configuration, the SLAVE device must set `DPLL{1:2}_SYNC_BYPASS` bit must be set to b'1 for the slave to use the SYNC input.

When using the fractional input divider, it will apply a static 1UI offset to the divided down reference clock (as described in section [Alignment of Fractional Input Divider](#)). It is recommended to apply an input skew offset to the reference input to account for the 1UI static offset. Note that this skew configuration only affects the feedback/output clocks, and does not change the setup/hold times used for the input divider.

[1] The high frequency input divider (`IN{8:3}_HF_DIV[1:0]`) and integer input divider (`IN{3:14}_PRE_DIVN_CNFG[14:0]`) are not aligned by the SYNC input.

Figure 21. Example with Input Divider - 0.5UI Early, -1UI Input Skew



For questions related to device configurations, please contact IDT application support at [support-sync@idt.com](mailto:support-sync@idt.com)

## Revision History

Table 3. Revision History

Revision Date	Description of Change
November 10, 2016	Initial release.

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