

Introduction

The Electrostatic Discharge (ESD) rating of a component can be misleading when the component datasheet does not specify the actual standard the component was tested to. Knowledge of the test standard is important as there are multiple standards in existence that significantly differ in severity.

This tech brief explains the differences between the two, most commonly applied ESD standards, the component level ESD test specified in JEDEC standard JS001-2010, and the system level ESD test, specified in the IEC 61000-4-2 standard.

Component Level ESD

Component level ESD ratings are necessary in the semiconductor manufacturing environment where component assembly, packaging and shipping can cause ESD damage to a single component. Here the test pulse generator creates an ESD pulse that simulates a charged person's discharge through the Device Under Test (DUT) to ground. Hence, the generator interior circuit model is known as the Human Body Model (HBM).

Since component handling is performed in a controlled ESD environment through the application of ESD protective gear, the ESD stress upon a component is drastically reduced. The HBM test, therefore, presents a less severe ESD test, which is sufficient for controlled environments but inadequate for systems in uncontrolled ESD environments.

System Level ESD

System level ESD ratings are required in the uncontrolled field environment where, for example, a charged end-user can subject a hand-held equipment to ESD levels of more than 40kV by touching connector pins when plugging or unplugging cables.

To better rate a system's ESD vulnerability, the IEC 61000-4-2 standard was developed, replicating a charged person discharging into a grounded electrical system via a metal object, such as a screw driver for example.

Differences between HBM and IEC 61000-4-2

The main differences between the HBM and the IEC 61000-4-2 standards are the number of strikes applied during testing and the generator models ([Figure 1](#)), which create differences in the waveforms' rise times and peak currents ([Figure 2](#)).

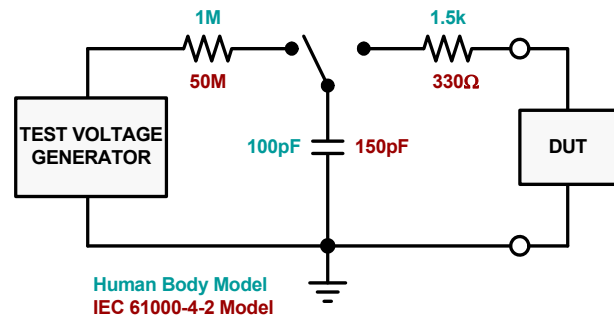


FIGURE 1. ESD GENERATOR MODELS PER HBM AND IEC 61000-4-2 STANDARDS

Pulse Rise Time

The pulse rise times of the two waveforms differ greatly. The rise time of a HBM strike can extend up to 25ns when discharging into a 500Ω resistor, while the rise time of an IEC 61000-4-2 strike is less than 1ns. Hence, an ESD structure designed for an HBM strike might not turn on when exposed to IEC-ESD strikes and the circuit to be protected becomes damaged.

Amount of Peak Current

The amount of peak current is critical to whether a component survives an ESD strike. As shown in the table of Figure 2, the peak current of an 8kV HBM strike is less than the peak current of a 2kV IEC 61000-4-2 strike. It is therefore possible for an IC to survive the 8kV HBM strike, however, fail the much lower, 2kV IEC-ESD strike.

Number of ESD Strikes

The number of ESD strikes in the HBM specification is limited to a single positive and a single negative strike, whereas IEC 61000-4-2 requires a minimum of 10 positive and 10 negative strikes. During an HBM test it is therefore possible for a component to survive the first strike, however, fail on subsequent strikes (if applied) due to damage sustained in the first strike.

Figure 2 shows the normalized waveforms for HBM and IEC 61000-4-2 ESD pulses and also lists various test voltages with their corresponding peak currents.

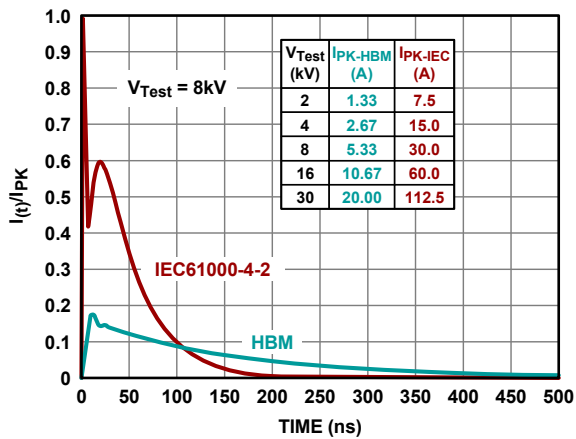


FIGURE 2. HBM AND IEC 61000-4-2 WAVEFORMS FOR 8kV

Conclusion

Since end user applications are subjected to many ESD strikes during their lifetime, system designers should always question generically written ESD specifications in component datasheets.

Devices complying with the IEC 61000-4-2 standard usually indicate this fact, while those that don't are commonly tested to the less severe HBM standard.

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Renesas Electronics America Inc.
1001 Murphy Ranch Road, Milpitas, CA 95035, U.S.A.
Tel: +1-408-432-8888, Fax: +1-408-434-5351

Renesas Electronics Canada Limited
9251 Yonge Street, Suite 8309 Richmond Hill, Ontario Canada L4C 9T3
Tel: +1-905-237-2004

Renesas Electronics Europe Limited
Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, U.K
Tel: +44-1628-651-700, Fax: +44-1628-651-804

Renesas Electronics Europe GmbH
Arcadiastrasse 10, 40472 Düsseldorf, Germany
Tel: +49-211-6503-0, Fax: +49-211-6503-1327

Renesas Electronics (China) Co., Ltd.
Room 1709 Quantum Plaza, No.27 ZhichunLu, Haidian District, Beijing, 100191 P. R. China
Tel: +86-10-8235-1155, Fax: +86-10-8235-7679

Renesas Electronics (Shanghai) Co., Ltd.
Unit 301, Tower A, Central Towers, 555 Langao Road, Putuo District, Shanghai, 200333 P. R. China
Tel: +86-21-2226-0888, Fax: +86-21-2226-0999

Renesas Electronics Hong Kong Limited
Unit 1601-1611, 16/F., Tower 2, Grand Century Place, 193 Prince Edward Road West, Mongkok, Kowloon, Hong Kong
Tel: +852-2265-6688, Fax: +852-2886-9022

Renesas Electronics Taiwan Co., Ltd.
13F, No. 363, Fu Shing North Road, Taipei 10543, Taiwan
Tel: +886-2-8175-9600, Fax: +886-2-8175-9670

Renesas Electronics Singapore Pte. Ltd.
80 Bendemeer Road, Unit #06-02 Hyflux Innovation Centre, Singapore 339949
Tel: +65-6213-0200, Fax: +65-6213-0300

Renesas Electronics Malaysia Sdn.Bhd.
Unit 1207, Block B, Menara Amcorp, Amcorp Trade Centre, No. 18, Jln Persiaran Barat, 46050 Petaling Jaya, Selangor Darul Ehsan, Malaysia
Tel: +60-3-7955-9390, Fax: +60-3-7955-9510

Renesas Electronics India Pvt. Ltd.
No.777C, 100 Feet Road, HAL 2nd Stage, Indiranagar, Bangalore 560 038, India
Tel: +91-80-67208700, Fax: +91-80-67208777

Renesas Electronics Korea Co., Ltd.
17F, KAMCO Yangjae Tower, 262, Gangnam-daero, Gangnam-gu, Seoul, 06265 Korea
Tel: +82-2-558-3737, Fax: +82-2-558-5338