

The Intersil HSP45116 Numerically Controlled Oscillator/Modulator (NCOM) can be combined with a low pass filter to perform down conversion on a digital signal. The NCOM rotates the spectrum of a real or complex signal and outputs a complex data stream. The signal of interest is now at base band, so that the output can be low pass filtered to eliminate unwanted signals (Figure 1).

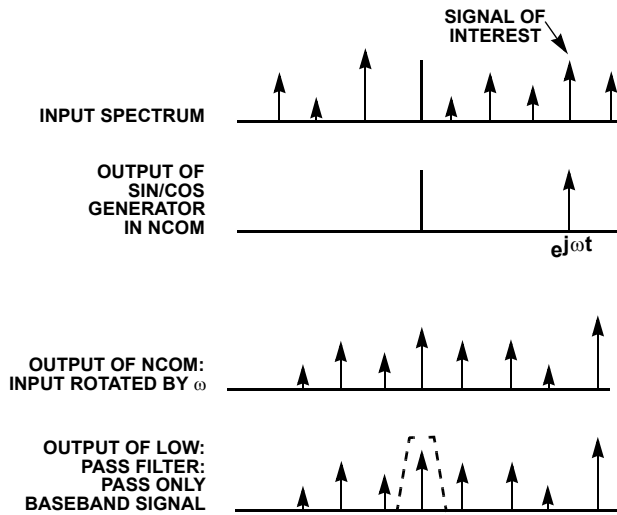


FIGURE 1. DOWN CONVERSION SPECTRAL PLOTS

If the spectrum of the signal of interest is sufficiently narrow, the output sample rate of the filter can be reduced to ease the throughput requirements of the downstream processing. Reducing the sample rate of a signal is commonly known as decimation. The input sample rate divided by the output sample rate is known as the decimation factor, or simply decimation. Note that decimation by one is equivalent to no decimation, and decimation by less than one is undefined. For the purposes of this discussion, base band signals will be divided into two categories: Wide band signals, where the decimation factor is 16 or less, and narrow band signals, where the decimation is greater than 16.

Narrow Band Down Conversion

For narrow band output signals, Intersil has a three chip set with a filter that is capable of decimation by up to 16,384. Figure 2 shows how the NCOM and HSP43220 Decimating Digital Filter (DDF) are connected to perform down conversion and real to quadrature conversion of an input signal. This is a generalized block diagram which can be used as the basis for a specific design.

Several assumptions were made in defining this block diagram. Among these assumptions are:

- Input and output data are sixteen bits. Users requiring less than that should keep bit 15 as the most significant bit, grounding the unused bits on the input of the NCOM. In all cases, bits 0 through 15 on the output of the NCOM should be connected to the sixteen input bits of the DDF. To select the output bits of the DDF, note that if the input is a cosine at frequency A and the NCOM is tuned to frequency B and the phase offset is 0, then the real and imaginary outputs of the NCOM at sample n are:

Real Output:

$$\cos(A_n)\cos(B_n) = [\cos(A_n - B_n) + \cos(A_n + B_n)].$$

Imaginary Output:

$$\cos(A_n)\sin(B_n) = [\sin(A_n + B_n) - \sin(A_n - B_n)].$$

Note that the factor of $1/2$ has been omitted. The output of the Complex Multiplier is shifted left by one bit internally. For this reason, both the real and imaginary outputs have the same magnitude as the input.

- The Phase Register is selected to control the phase of the NCOM (as opposed to MOD0-1) and is initialized along with the center frequency. In this example, the LOAD signal is not exercised, so the initial phase of the NCOM is unknown.
- To shift the positive component of a real input signal to base band, the Center Frequency Register of the NCOM is set to a negative number.
- The Offset Frequency Register, Timer Accumulator and Complex Accumulator of the NCOM are not used.
- The filter clocks of the two DDFs are driven at a higher rate than the input data clocks. For many applications the FIR_CK, CK_IN and CLK signals can all be connected together. In this case the divide by N block is not needed.

The DDFs are reset and started asynchronously with a pulse generator that receives asynchronous commands from an outside source and drives the two DDFs simultaneously. The DDF receiving the asynchronous start pulse performs the synchronization and starts the other part at the proper time.

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Renesas Electronics America Inc.
1001 Murphy Ranch Road, Milpitas, CA 95035, U.S.A.
Tel: +1-408-432-8888, Fax: +1-408-434-5351

Renesas Electronics Canada Limited
9251 Yonge Street, Suite 8309 Richmond Hill, Ontario Canada L4C 9T3
Tel: +1-905-237-2004

Renesas Electronics Europe Limited
Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, U.K
Tel: +44-1628-651-700, Fax: +44-1628-651-804

Renesas Electronics Europe GmbH
Arcadiastrasse 10, 40472 Düsseldorf, Germany
Tel: +49-211-6503-0, Fax: +49-211-6503-1327

Renesas Electronics (China) Co., Ltd.
Room 1709 Quantum Plaza, No.27 ZhichunLu, Haidian District, Beijing, 100191 P. R. China
Tel: +86-10-8235-1155, Fax: +86-10-8235-7679

Renesas Electronics (Shanghai) Co., Ltd.
Unit 301, Tower A, Central Towers, 555 Langao Road, Putuo District, Shanghai, 200333 P. R. China
Tel: +86-21-2226-0888, Fax: +86-21-2226-0999

Renesas Electronics Hong Kong Limited
Unit 1601-1611, 16/F., Tower 2, Grand Century Place, 193 Prince Edward Road West, Mongkok, Kowloon, Hong Kong
Tel: +852-2265-6688, Fax: +852-2886-9022

Renesas Electronics Taiwan Co., Ltd.
13F, No. 363, Fu Shing North Road, Taipei 10543, Taiwan
Tel: +886-2-8175-9600, Fax: +886-2-8175-9670

Renesas Electronics Singapore Pte. Ltd.
80 Bendemeer Road, Unit #06-02 Hyflux Innovation Centre, Singapore 339949
Tel: +65-6213-0200, Fax: +65-6213-0300

Renesas Electronics Malaysia Sdn.Bhd.
Unit 1207, Block B, Menara Amcorp, Amcorp Trade Centre, No. 18, Jln Persiaran Barat, 46050 Petaling Jaya, Selangor Darul Ehsan, Malaysia
Tel: +60-3-7955-9390, Fax: +60-3-7955-9510

Renesas Electronics India Pvt. Ltd.
No.777C, 100 Feet Road, HAL 2nd Stage, Indiranagar, Bangalore 560 038, India
Tel: +91-80-67208700, Fax: +91-80-67208777

Renesas Electronics Korea Co., Ltd.
17F, KAMCO Yangjae Tower, 262, Gangnam-daero, Gangnam-gu, Seoul, 06265 Korea
Tel: +82-2-558-3737, Fax: +82-2-558-5338