The radiation hardened ISL72991RH is a low dropout adjustable negative regulator with an output voltage range of -2.25V to -26V. The device features a 1A output current capability, an adjustable current limit pin (ILIM), and a shutdown pin (SD) for easy on/off control.

The device incorporates unique circuitry that enables precision performance across the -55°C to +125°C temperature range and post-irradiation. Specifications across the full temperature range include an internal reference voltage of -1.25V +40mV/-50mV (maximum), line regulation of ±25mV (maximum), and load regulation of ±15mV (maximum). The reference voltage is the ADJ to GND voltage.

Constructed with the Intersil dielectrically isolated Rad Hard Silicon Gate (RSG) BiCMOS process, these devices are immune to single event latch-up and have been specifically designed to provide highly reliable performance in harsh radiation environments.

Applications
• Post switching power supplies
• DC/DC converters
• Motor controllers

Features
• Electrically screened to DLA SMD # 5962-02503
• QML qualified per MIL-PRF-38535 requirements
• Latch-up immune DI process
• Wide input voltage range ................. -3V to -30V
• Nominal output voltage range ........... -2.25V to -26V
• Line regulation ......................... ±25mV (maximum)
• Load regulation ....................... ±12mV (typ); ±15mV (maximum)
• Dropout voltage (100mA) ........... 0.2V (typ); 0.3V (maximum)
• Dropout voltage (1A) ............. 1V (maximum)
• Minimum load current .................... 3.0mA
• TTL input-level shutdown (SD); low = on
• Operating temperature range .......... -55°C to +125°C
• Radiation environment
  - SEL/SEB LETTH (V_S = -30V) ....... 86.4MeV•cm²/mg
  - Total dose, high dose rate ............ 300krad(Si)

Related Literature
• For a full list of related documents, visit our website
  - ISL72991RH product page
## Ordering Information

<table>
<thead>
<tr>
<th>ORDERING SMD NUMBER</th>
<th>PART NUMBER</th>
<th>TEMP RANGE (°C)</th>
<th>PACKAGE (RoHS COMPLIANT)</th>
<th>PKG. DWG. #</th>
</tr>
</thead>
<tbody>
<tr>
<td>5962F0250301VXC</td>
<td>ISL72991RHVF</td>
<td>-55 to +125</td>
<td>28 Ld Flatpack</td>
<td>K28.A</td>
</tr>
<tr>
<td>5962F0250301QXC</td>
<td>ISL72991RHQF</td>
<td>-55 to +125</td>
<td>28 Ld Flatpack</td>
<td>K28.A</td>
</tr>
<tr>
<td>5962F0250301V9A</td>
<td>ISL72991RHVX</td>
<td>-55 to +125</td>
<td>DIE</td>
<td></td>
</tr>
<tr>
<td>N/A</td>
<td>ISL72991RHF/PROTO (Note 3)</td>
<td>-55 to +125</td>
<td>28 Ld Flatpack</td>
<td>K28.A</td>
</tr>
<tr>
<td>N/A</td>
<td>ISL72991RHX/SAMPLE (Note 3)</td>
<td>-55 to +125</td>
<td>DIE</td>
<td></td>
</tr>
<tr>
<td>N/A</td>
<td>ISL72991RHEVAL22 (Note 4)</td>
<td>Evaluation Board</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**NOTES:**

1. These Intersil Pb-free Hermetic packaged products employ 100% Au plate - e4 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations.

2. Specifications for Rad Hard QML devices are controlled by the Defense Logistics Agency Land and Maritime (DLA). The SMD numbers listed must be used when ordering.

3. The /PROTO and /SAMPLE are not rated or certified for Total Ionizing Dose (TID) or Single Event Effect (SEE) immunity. These parts are intended for engineering evaluation purposes only. The /PROTO parts meet the electrical limits and conditions across the temperature range specified in the DLA SMD and are in the same form and fit as the qualified device. The /SAMPLE die is capable of meeting the electrical limits and conditions specified in the DLA SMD at +25°C only. The /SAMPLE is a die and does not receive 100% screening across the temperature range to the DLA SMD electrical limits. These part types do not come with a certificate of conformance because there is no radiation assurance testing and they are not DLA qualified devices.

4. Evaluation board uses the /PROTO parts. The /PROTO parts are not rated or certified for Total Ionizing Dose (TID) or Single Event Effect (SEE) immunity.

## Pin Configuration

![Pin Configuration Diagram](image-url)
# Pin Descriptions

<table>
<thead>
<tr>
<th>PIN NUMBER</th>
<th>PIN NAME</th>
<th>EQUIVALENT CIRCUIT</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>1, 2, 27, 28</td>
<td>VIN</td>
<td>Circuit 2</td>
<td>Regulator bias and input connection. All 4 pins must be tied together.</td>
</tr>
<tr>
<td>12</td>
<td>ILIM</td>
<td>Circuit 2</td>
<td>Current limiting set input.</td>
</tr>
<tr>
<td>13, 14, 15, 16</td>
<td>VOUT</td>
<td>Circuit 2</td>
<td>Regulator output connection. All 4 pins must be tied together.</td>
</tr>
<tr>
<td>17</td>
<td>SD</td>
<td>Circuit 1</td>
<td>Shut down input, active high.</td>
</tr>
<tr>
<td>18</td>
<td>ADJ</td>
<td>Circuit 2</td>
<td>Output voltage adjust input</td>
</tr>
<tr>
<td>11</td>
<td>GND</td>
<td></td>
<td>Ground connection</td>
</tr>
<tr>
<td>3, 4, 5, 6, 7, 8, 9, 10, 19, 20, 21, 22, 23, 24, 25, 26</td>
<td>NC</td>
<td></td>
<td>No Internal connections. Can be connected to ground or thermal plane.</td>
</tr>
</tbody>
</table>

![Functional Block Diagram](image_url)

**FIGURE 3. FUNCTIONAL BLOCK DIAGRAM**
Typical Application

- VDC TO -VDC VOLTAGE REGULATION CIRCUIT

FIGURE 4. TYPICAL APPLICATION
Absolute Maximum Ratings

- Minimum Supply Voltage: -35V
- Minimum Supply Voltage (Note 7): -30V
- Minimum Output Current: 3mA
- Output Short-Circuit Duration: Indefinite
- ESD Rating:
  - Human Body Model (HBM) (Tested per MIL-PRF-883 3015.7): 3kV
  - Machine Model (MM) (Tested per EIA/JESD22-A115-A): 300V
  - Charged Device Model (CDM) (Tested per JESD22-C101D): 1kV
- Thermal Resistance (Typical):
  - \( \theta_{JA} \) (°C/W): 60
  - \( \theta_{JC} \) (°C/W): 5
- Maximum Storage Temperature Range: -65°C to +150°C
- Maximum Junction Temperature (TJMAX): +150°C

Recommended Operating Conditions

- Ambient Operating Temperature Range: -55°C to +125°C
- Maximum Operating Temperature: +150°C
- Supply Voltage: -3V to -30V

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:
5. \( \theta_{JA} \) is measured with the component mounted on a low-effective thermal conductivity test board in free air. See tech brief TB379 for details.
6. For \( \theta_{JC} \), the “case temp” location is the center of the package underside.
7. The minimum supply limit specified is for operation in a heavy ion environment at an LET = 86.4MeV•cm²/mg.

Electrical Specifications

**DESCRIPTION** | **PARAMETER** | **TEST CONDITIONS** | **MIN (Note 8)** | **TYP** | **MAX (Note 8)** | **UNIT**
---|---|---|---|---|---|---
Reference Voltage (ADJ to GND) | \( V_{REF} \) | \( I_O = 3mA \) to 1A | -1.279 | -1.250 | -1.231 | V
| | | \( -1.300 \) | | \( -1.210 \) | V
Minimum Output Voltage | \( V_{Omin} \) | \( V_{IN} = -3V, I_O = 3mA \) to 100mA | -2.6 | | -2.25 | V
Maximum Output Voltage | \( V_{Omax} \) | \( V_{IN} = -30V, I_O = 3mA \) to 100mA | -12 | 12 | | mV
Output Voltage Load Regulation | \( V_{LDR} \) | \( V_{IN} = -7V, V_O = -5V, I_O = 3mA \) to 1A | -15 | 15 | | mV
Output Voltage Line Regulation | \( V_{LNR} \) | \( V_O \leq V_{IN} -1V \) to \( V_{IN} = -30V, I_O = 100mA \) | -25 | 25 | | mV
0.1A Dropout Voltage | \( V_{DOL} \) | \( dV_O \leq 50mV, I_O = 0.1A \) | 0.2 | | | V
| | | \( 0.3 \) | | | V
1A Dropout Voltage (Pulse Tested) | \( V_{DOH} \) | \( dV_O \leq 50mV, I_O = 1A \) | 1 | | | V
Adjust Current | \( I_{ADJ} \) | \( V_O \leq V_{IN} -1V \) to \( V_{IN} = -30V, I_O = 500mA \) | 1.7 | 5.0 | | \( \mu A \)
Dropout Quiescent Current | \( I_{QDO} \) | \( V_O \cdot V_{IN} = 0.2V, I_O = 500mA \) | 25 | | | mA
| | | \( V_O \cdot V_{IN} = 0.3V, I_O = 500mA \) | 25 | | | mA
SD Input Voltage | \( V_{SD} \) | \( V_O = ON \) | 0.8 | | | V
| | | \( V_O = OFF \) | 2.4 | | | V
SD Input Current | \( I_{SD} \) | \( V_{SD} = 0.8V \) | 50 | | | \( \mu A \)
| | | \( V_{SD} = 2.4V \) | 100 | | | \( \mu A \)
Output Short-Circuit Current Limit | \( I_{SCL} \) | \( V_{IN} = -7V, V_O = 0V, R_{CL} = 3.7k\Omega \) | 0.60 | 0.75 | 0.90 | A
GND Quiescent Current | \( I_{GND} \) | \( -3V \leq V_{IN} \leq -30V, I_O < 1A \) | 6 | | | mA
Power Supply Rejection Ratio | PSRR | Frequency = 1MHz | -49 | | | dB
Thermal Protection | \( OTPROT \) | | | 150 | | °C
Thermal Hysteresis | \( OT_{HYS} \) | | | 20 | | °C
### Post Radiation Electrical Specifications

$V_O \leq V_{IN} - 1.5V, I_O = 100mA, C_O = 47\mu F, SD = 0V, T_A = +25^\circ C$, across a total ionizing dose of 300krad(Si) with exposure at a high dose rate of 50 to 300rad(Si)/s.

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>DESCRIPTION</th>
<th>TEST CONDITIONS</th>
<th>MIN (Note 8)</th>
<th>TYP</th>
<th>MAX (Note 8)</th>
<th>UNITS</th>
</tr>
</thead>
<tbody>
<tr>
<td>V_REF</td>
<td>Reference Voltage</td>
<td>$I_O = 3mA to 1A$</td>
<td>-1.279</td>
<td>-</td>
<td>-1.231</td>
<td>V</td>
</tr>
<tr>
<td>$V_{Omin}$</td>
<td>Minimum Output Voltage</td>
<td>$V_{IN} = -3V, I_O = 3mA to 100mA$</td>
<td>-2.59</td>
<td>-</td>
<td>-2.25</td>
<td>V</td>
</tr>
<tr>
<td>$V_{Omax}$</td>
<td>Maximum Output Voltage</td>
<td>$V_{IN} = -30V, I_O = 3mA to 100mA$</td>
<td>-26</td>
<td>-</td>
<td>12</td>
<td>V</td>
</tr>
<tr>
<td>VLDR</td>
<td>Output Voltage Load Regulation</td>
<td>$V_{IN} = -7V, V_O = -5V I_O = 3mA to 1A$</td>
<td>-12</td>
<td>-</td>
<td>25</td>
<td>mV</td>
</tr>
<tr>
<td>VLINR</td>
<td>Output Voltage Line Regulation</td>
<td>$V_O \leq V_{IN} - 1V$ to $V_{IN} = -30V, I_O = 100mA$</td>
<td>-25</td>
<td>-</td>
<td>25</td>
<td>mV</td>
</tr>
<tr>
<td>$VD_{OL}$</td>
<td>0.1A Dropout Voltage</td>
<td>$dV_O \leq 50mV, I_O = 0.1A$</td>
<td>0.2</td>
<td>-</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>$VD_{OH}$</td>
<td>1A Dropout Voltage (Pulse Tested)</td>
<td>$dV_O \leq 50mV, I_O = 1A$</td>
<td>1</td>
<td>-</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>$I_{ADJ}$</td>
<td>Adjust Current</td>
<td>$V_O \leq V_{IN} - 1V$ to $V_{IN} = -30V, I_O = 500mA$</td>
<td>5.3</td>
<td>-</td>
<td>$25 \mu A$</td>
<td></td>
</tr>
<tr>
<td>$I_{QDO}$</td>
<td>Dropout Quiescent Current</td>
<td>$V_O \cdot V_{IN} = 0.3V, I_O = 500mA$</td>
<td>25</td>
<td>-</td>
<td>mA</td>
<td></td>
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<tr>
<td>V_SD</td>
<td>SD Input Voltage</td>
<td>$V_O = ON$</td>
<td>0.8</td>
<td>-</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V_O = OFF$</td>
<td>2.4</td>
<td>-</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>I_SD</td>
<td>SD Input Current</td>
<td>$V_{SD} = 0.8V$</td>
<td>50</td>
<td>-</td>
<td>$25 \mu A$</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V_{SD} = 2.4V$</td>
<td>100</td>
<td>-</td>
<td>$25 \mu A$</td>
<td></td>
</tr>
<tr>
<td>I_CL</td>
<td>Output Short-Circuit Current Limit</td>
<td>$V_{IN} = - 7V, V_O = 0V, R_{CL} = 3.7k\Omega$</td>
<td>0.6</td>
<td>-</td>
<td>0.9</td>
<td>A</td>
</tr>
</tbody>
</table>

**NOTE:**

8. Compliance to datasheet limits is assured by one or more methods: production test, characterization, and/or design.
Total Dose Radiation Characteristics

This data is typical mean test data post total dose radiation exposure at a high dose rate (HDR) of 50 to 300 rad(Si)/s to 300 krad. This data is intended to show typical parameter shifts due to total dose rate radiation. These are not limits nor are they guaranteed.

FIGURE 5. REFERENCE VOLTAGE CHANGE vs TOTAL DOSE RADIATION

FIGURE 6. 0.1A DROPOUT VOLTAGE CHANGE vs TOTAL DOSE RADIATION

FIGURE 7. 1A DROPOUT VOLTAGE CHANGE vs TOTAL DOSE RADIATION

FIGURE 8. OUTPUT VOLTAGE LINE REGULATION CHANGE vs TOTAL DOSE RADIATION

FIGURE 9. OUTPUT VOLTAGE LOAD REGULATION CHANGE vs TOTAL DOSE RADIATION
Typical Performance Curves

**FIGURE 10. -7V IN, -5VOUT**

![Graph showing CURRENT LIMIT vs RCL for -7V IN, -5VOUT](image)

**FIGURE 11. -12V IN, -5VOUT**

![Graph showing CURRENT LIMIT vs RCL for -12V IN, -5VOUT](image)

**FIGURE 12. -12V IN, -10VOUT**

![Graph showing CURRENT LIMIT vs RCL for -12V IN, -10VOUT](image)

**FIGURE 13. -20V IN, -10VOUT**

![Graph showing CURRENT LIMIT vs RCL for -20V IN, -10VOUT](image)

**FIGURE 14. VREF vs TEMPERATURE**

![Graph showing VREF vs TEMPERATURE for different values of VIN and IOUT](image)

**FIGURE 15. DROPOUT VOLTAGE vs TEMPERATURE**

![Graph showing DROPOUT VOLTAGE vs TEMPERATURE for different values of OUT](image)
Typical Performance Curves (Continued)

**FIGURE 16. LINE REGULATION vs TEMPERATURE**

**FIGURE 17. LOAD REGULATION vs TEMPERATURE**

**FIGURE 18. PSRR vs FREQUENCY (V_{IN} = -20V, V_{OUT} = -18V)**

**FIGURE 19. PSRR vs FREQUENCY (V_{IN} = -7V, V_{OUT} = -5V)**

**FIGURE 20. GAIN/PHASE -12V_{IN}, -5V_{OUT}, 0.5A I_{OUT}**

**FIGURE 21. THERMAL (V_{IN} = -12V, V_{OUT} = -5V, I_{OUT} = 0.74A, T_{A} = +25°C)**
Functional Description

Functional Overview
The radiation hardened ISL72991RH is a low dropout adjustable negative regulator with an output voltage range of -2.25V to -26V. The device features a 1A output current capability, an adjustable current limit pin (ILIM), and a shutdown pin (SD) for easy on/off control. The part is constructed using the Intersil dielectrically isolated, complimentary bipolar RSG process. It is immune to single-event latch-up and has been specifically designed to provide reliable performance in harsh radiation environments.

Application Information

Output Voltage Programming
The output voltage of the regulator can be programmed with two external resistors and is described by Equation 1:

\[ V_{OUT} = -1.25\left(1 + \frac{R_1}{R_2}\right) - \left(I_{ADJ}\times R_1\right) \]  

(EQ. 1)

Output Current Limit Programming
The output current limit threshold of the regulator is set with a single external resistor (RCL) connected from ILIM to ground. The effective current limit at any single RCL value is influenced by the VIN to VOUT difference, temperature, and VIN amplitude. Figures 22 through 24 illustrate these effects.

Figure 22 shows that for a given VOUT (-5V) and temperature (+25°C) the effect of VIN to VOUT differential on the current limit level is significant.

Figure 23 shows the effect of temperature at a single VIN to VOUT voltage condition across the RCL range of 2.1kΩ to 10kΩ.

Figure 24 shows that for a given differential voltage (VIN to VOUT) and temperature, the effect of VIN amplitude is less significant than seen in Figure 22.

Because of these numerous variables, there is no one formula relating RCL to ICL that will suffice for the range of likely possible conditions. Figures 10 through 13 on page 8 provide guidance in setting the RCL value for a limited number of possible conditions. Users are advised to evaluate their specific condition for satisfactory performance.

Capacitor Selection
An input capacitor is required if the regulator is located more than 6 inches from the power supply filter capacitors. A 10μF solid tantalum capacitor is recommended.

An output capacitor of at least 10μF must be used to ensure stability of the regulator. Additional capacitance may be added as required to improve the dynamic response of the regulator. Solid tantalum or ceramic capacitors are recommended.

Loop Compensation
The output capacitor and ESR comprise a zero in the loop transfer function that must be compensated with a pole to ensure loop stability in accordance with Equation 2:

\[ C_C \times R_1 = C_{OUT} \times ESR \]  

(EQ. 2)

The compensating capacitor should be a low ESR ceramic type.

Layout Guidelines

The stability of the regulator is sensitive to layout. It is strongly recommended that a continuous copper ground plane (1oz. or greater) be used. In addition, component lead lengths and interconnects should be minimized, but should not exceed 1/2 inch. Finally, the return lead of the compensation capacitor (C_C) should be connected as close as possible to the GND pin of the IC.
Package Characteristics

Weight of Packaged Device
2.2 Grams (Typical)

Lid Characteristics
Finish: Gold
Potential: Unbiased
Case Isolation to Any Lead: $2 \times 10^9 \, \Omega \text{ (min)}$

Die Characteristics

Die Dimensions
5870µm x 5210µm (231.1 mils x 205.1 mils)
Thickness: 483µm ±25.4µm (19 mils ±1 mil)

Interface Materials

GLASSIVATION
Type: PSG (Phosphorous Silicon Glass)
Thickness: 8.0kÅ ±1.0kÅ

TOP METALLIZATION
Type: AlSiCu (Si 0.75-1%/Cu 0.5%)
Thickness: 16.0kÅ ±2kÅ

BACKSIDE FINISH
Silicon

Assembly Related Information

SUBSTRATE AND LID POTENTIAL
Floating

Additional Information

WORST CASE CURRENT DENSITY
$< 2 \times 10^5 \, \text{A/cm}^2$

PROCESS
Dielectrically Isolated Radiation Hardened Silicon Gate

Metallization Mask Layout
### TABLE 1. DIE PAD COORDINATES

<table>
<thead>
<tr>
<th>PAD NAME</th>
<th>X-COR CENTER</th>
<th>Y-COR CENTER</th>
<th>DX PAD SIZE</th>
<th>DY PAD SIZE</th>
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</thead>
<tbody>
<tr>
<td>ILIM</td>
<td>-1300.5</td>
<td>-4348</td>
<td>258</td>
<td>516</td>
</tr>
<tr>
<td>(15)VOUT</td>
<td>920</td>
<td>-2712</td>
<td>516</td>
<td>516</td>
</tr>
<tr>
<td>SHUTDOWN</td>
<td>3140.5</td>
<td>-4348</td>
<td>258</td>
<td>516</td>
</tr>
<tr>
<td>ADJUST</td>
<td>3473.5</td>
<td>-3658</td>
<td>258</td>
<td>516</td>
</tr>
<tr>
<td>(16)VOUT</td>
<td>2917</td>
<td>-2554</td>
<td>516</td>
<td>516</td>
</tr>
<tr>
<td>(27)VOUT</td>
<td>3580</td>
<td>-156</td>
<td>258</td>
<td>516</td>
</tr>
<tr>
<td>(28)VIN</td>
<td>1840</td>
<td>0</td>
<td>516</td>
<td>516</td>
</tr>
<tr>
<td>(1)VIN</td>
<td>0</td>
<td>0</td>
<td>516</td>
<td>516</td>
</tr>
<tr>
<td>(2)VIN</td>
<td>-1740</td>
<td>-166</td>
<td>258</td>
<td>516</td>
</tr>
<tr>
<td>(14)VOUT</td>
<td>-1077</td>
<td>-2554</td>
<td>516</td>
<td>516</td>
</tr>
<tr>
<td>GND</td>
<td>-1662</td>
<td>-3657</td>
<td>258</td>
<td>516</td>
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**Revision History**  The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to web to make sure you have the latest Revision.

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<th>DATE</th>
<th>REVISION</th>
<th>CHANGE</th>
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<tr>
<td>Apr 14, 2017</td>
<td>FN9054.6</td>
<td>Added Notes 3 and 4 on page 2. Added Table 1 on page 12.</td>
</tr>
<tr>
<td>Aug 17, 2016</td>
<td>FN9054.5</td>
<td>Updated Equation 2 Loop Compensation equation to change R2 to R1.</td>
</tr>
<tr>
<td>May 7, 2015</td>
<td>FN9054.4</td>
<td>Replaced Figures 10, 11, 12 and 13 on page 8. Replaced Figures 22, 23 and 24 on page 10. Updated Equation 1 on page 10: from ( V_{OUT} = -1.25(1+R2/R1) - (I_{ADJ} \times R2) ) to ( V_{OUT} = -1.25(1+R1/R2) - (I_{ADJ} \times R1) ).</td>
</tr>
<tr>
<td>Jan 29, 2015</td>
<td>FN9054.3</td>
<td>“Typical Performance Curves” on page 8: Added Figures 18 and 19.</td>
</tr>
<tr>
<td>Mar 26, 2014</td>
<td>FN9054.2</td>
<td>Added Related Literature on page 1. Added significant relevant content throughout the document, expanding from 3 to 12 pages.</td>
</tr>
<tr>
<td>Jun, 28, 2004</td>
<td>FN9054.1</td>
<td>Updated file.</td>
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<tr>
<td>Jul 9, 2001</td>
<td>FN9054.0</td>
<td>Initial Release.</td>
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**About Intersil**

Intersil Corporation is a leading provider of innovative power management and precision analog solutions. The company’s products address some of the largest markets within the industrial and infrastructure, mobile computing and high-end consumer markets.

For the most updated datasheet, application notes, related documentation and related parts, please see the respective product information page found at [www.intersil.com](http://www.intersil.com).

For a listing of definitions and abbreviations of common terms used in our documents, visit [www.intersil.com/glossary](http://www.intersil.com/glossary).

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Ceramic Metal Seal Flatpack Packages (Flatpack)

NOTES:
1. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer’s identification shall not be used as a pin one identification mark. Alternately, a tab (dimension k) may be used to identify pin one.
2. If a pin one identification mark is used in addition to a tab, the limits of dimension k do not apply.
3. This dimension allows for off-center lid, meniscus, and glass overrun.
4. Dimensions b1 and c1 apply to lead base metal only. Dimension M applies to lead plating and finish thickness. The maximum limits of lead dimensions b and c or M shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.
5. N is the maximum number of terminal positions.
6. Measure dimension S1 at all four corners.
7. For bottom-brazed lead packages, no organic or polymeric materials shall be molded to the bottom of the package to cover the leads.
8. Dimension Q shall be measured at the point of exit (beyond the meniscus) of the lead from the body. Dimension Q minimum shall be reduced by 0.0015 inch (0.038mm) maximum when solder dip lead finish is applied.
10. Controlling dimension: INCH.

### K28.A MIL-STD-1835 CDFP3-F28 (F-11A, CONFIGURATION B) 28 LEAD CERAMIC METAL SEAL FLATPACK PACKAGE

<table>
<thead>
<tr>
<th>SYMBOL</th>
<th>INCHES</th>
<th>MILLIMETERS</th>
<th>NOTES</th>
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<tr>
<td>A</td>
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<tr>
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<td>D</td>
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<tr>
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For the most recent package outline drawing, see [K28.A](#)