ISL71590SEH, ISL73590SEH

Radiation Hardened, 2-Terminal Temperature Transducer

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Rev.3.00
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The ISL71590SEH and ISL73590SEH are temperature-to-current transducers possessing two terminals. They have a high impedance current output that allows them to be insensitive to voltage drops across long lines. When provided a differential voltage between 4V and 33V, the devices act as constant current regulators that generate a current equal to 1µA/Kelvin (K).

These devices are specified across the -55°C to +125°C temperature range and with ±1.7°C accuracy without the need of additional circuitry, and also capable of operating up to +150°C. With power requirements as low as 1.5mW (5V at +25°C), they are an ideal choice for remote sensing applications as any well-insulated twisted pair cable will allow for proper operation. They can be used in several additional applications including temperature compensation networks, flow rate analysis, anemometry, and biasing proportional to absolute temperature.

The high output impedance (>10MΩ) leaves plenty of room for variations in the power supply voltage. The ISL7x590SEH is electrically durable as it can withstand a forward operating voltage of 33V over the full temperature range both under and without ion beam radiation and a reverse voltage of -40V.

The ISL71590SEH and ISL73590SEH are available in 2 Ld flatpacks and die forms. All material applies to both parts except for TID assurance test levels.

Applications

- RF power amplifier bias compensation
- LCD bias compensation
- Laser diode bias compensation
- Sensor bias and linearization
- Data acquisition systems

Features

- 50krad(Si) low dose rate (ELDRS) shift . . . . < 1°C
- Linear output current. 1µA/K
- Wide power supply input range (V+ to V-). . . . . 4V to 33V
- Low power consumption . . . . 1.5mW at 5V
- High output impedance provides excellent rejection to variations in the supply line
- Additional linearization circuitry is not needed for operation
- Operating temperature range. . . . .-55°C to +150°C
- QML qualified per MIL-PRF-38535 requirements
- Radiation environment
  - SEL/SEB LET_{TH} . . . . 86.4MeV•cm^2/mg
  - Total dose, high dose rate. . . . . 300krad(Si)*
  - Total dose, low dose rate . . . . 50krad(Si)

*Applies to the ISL71590SEH only.

- Electrically screened to SMD# 5962-13215

Related Literature

For a full list of related documents, visit our website

- ISL71590SEH and ISL73590SEH product pages

TABLE 1. KEY DIFFERENCES BETWEEN FAMILY OF PARTS

PART NUMBER	HIGH DOSE RATE (HDR) ASSURANCE TEST LEVEL (krad(Si))	LOW DOSE RATE (LDR) ASSURANCE TEST LEVEL (krad(Si))
ISL71590SEH	300	50
ISL73590SEH	N/A	50

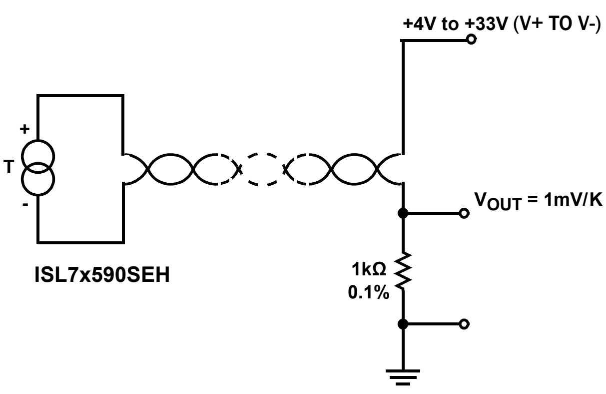


FIGURE 1. TYPICAL APPLICATION

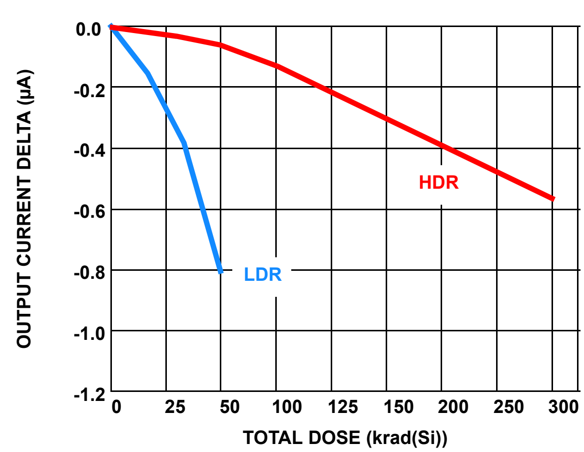


FIGURE 2. I_{OUT} SHIFT vs LOW/HIGH DOSE RATE RADIATION

Ordering Information

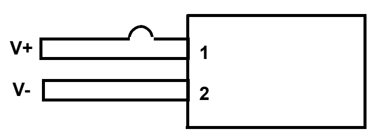
ORDERING SMD NUMBER (Note 2)	PART NUMBER (Note 1)	HIGH DOSE RATE (HDR) krad(Si)	LOW DOSE RATE (LDR) krad(Si)	TEMPERATURE RANGE (°C)	PACKAGE (RoHS COMPLIANT)	PKG. DWG. #
5962F1321501VXC	ISL71590SEHVF	300	50	-55 to +125	2 Ld Flatpack	K2.A
5962F1321501V9A	ISL71590SEHVX	300	50	-55 to +125	Die	
5962L1321502VXC	ISL73590SEHVF	N/A	50	-55 to +125	2 Ld Flatpack	K2.A
5962L1321502V9A	ISL73590SEHVX	N/A	50	-55 to +125	Die	
N/A	ISL71590SEHF/PROTO (Note 3)	N/A	N/A	-55 to +125	2 Ld Flatpack	K2.A
N/A	ISL71590SEHX/SAMPLE (Note 3)	N/A	N/A	-55 to +125	Die	
N/A	ISL71590SEHMF	300	50	-55 to +125	2 Ld Flatpack	K2.A
N/A	ISL71590SEHEV1Z (Note 4)	Evaluation Board				

NOTES:

1. These Pb-free Hermetic packaged products employ 100% Au plate - e4 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations.
2. Specifications for Rad Hard QML devices are controlled by the Defense Logistics Agency Land and Maritime (DLA). The SMD numbers listed must be used when ordering.
3. The /PROTO and /SAMPLE are not rated or certified for Total Ionizing Dose (TID) or Single Event Effect (SEE) immunity. These parts are intended for engineering evaluation purposes only. The /PROTO parts meet the electrical limits and conditions across temperature specified in the DLA SMD and are in the same form and fit as the qualified device. The /SAMPLE parts are capable of meeting the electrical limits and conditions specified in the DLA SMD at +25°C only. The /SAMPLE parts do not receive 100% screening across temperature to the DLA SMD electrical limits. These part types do not come with a Certificate of Conformance because they are not DLA qualified devices.
4. Evaluation board uses the /PROTO parts. The /PROTO parts are not rated or certified for Total Ionizing Dose (TID) or Single Event Effect (SEE) immunity.

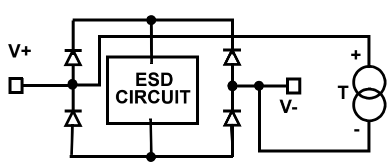
Pin Configuration

2 LD FLATPACK
TOP VIEW



Pin Descriptions

PIN NUMBER	PIN NAME	EQUIVALENT ESD CIRCUIT	DESCRIPTION
1	V+	Circuit 1	Positive voltage lead range 4V to 33V
2	V-	Circuit 1	Negative voltage lead



Circuit 1

Functional Block Diagram

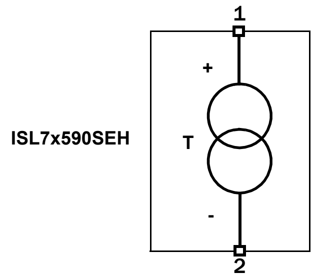


FIGURE 3. BLOCK DIAGRAM

Typical Applications

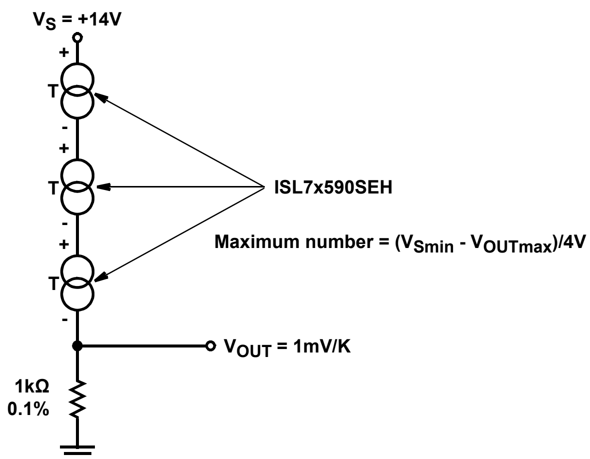
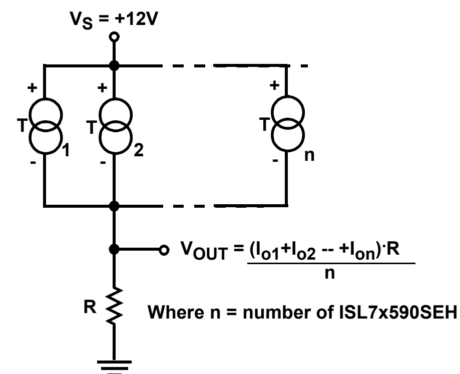


FIGURE 4. LOWEST TEMPERATURE SENSING SCHEME. OUTPUT CURRENT IS THAT OF THE “COLDEST” SENSOR



(e.g., with four sensors and R = 250Ω V_{OUT} = 1mV/K)

FIGURE 5. AVERAGE TEMPERATURE SENSING SCHEME. OUTPUT CURRENT IS THE SUM OF ALL SENSOR CURRENTS

Absolute Maximum Ratings

Maximum Supply Voltage 40V
In-Beam Maximum Supply Voltage (Note 7) 37V
Maximum Reverse Voltage . . . . -40V
Maximum Differential Input Voltage . . . . ±40V
Case to Lead Breakdown Voltage . . . . ±200V
ESD Rating
  Human Body Model (Tested per MIL-STD-883 TM3015.7) 3kV
  Machine Model (Tested per EIA/JESD22-A115-A) 300V
  Charged Device Model (Tested per JESD22-C101D) 750V

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
2 Ld Flatpack (Notes 5, 6)	80	8

Storage Temperature Range . . . . -65°C to +155°C
Maximum Junction Temperature (T_{JMAX}) . . . . +150°C

Recommended Operating Conditions

Ambient Operating Temperature Range . . . . -55°C to +125°C
Maximum Operating Junction Temperature . . . . +150°C
Supply Voltage (V+ to V-) (Notes 7, 8) . . . . 4V to 33V

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

5. θ_{JA} is measured in free air with the component mounted on a high-effective thermal conductivity test board with "direct attach" features. See Tech Brief TB379.
6. For θ_{JC}, the "case temp" location is the center of the ceramic on the package underside.
7. The maximum supply voltage specified is for operation in a heavy ion environment at an LET = 86.4MeV • cm^2/mg.
8. The maximum voltage beyond which output current performance is not to be considered valid (Figure 9).

Electrical Specifications

V_S = 5V, T_A = +25°C, unless otherwise noted. **Boldface limits apply across the operating temperature range, -55°C to +125°C.**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 9)	TYP	MAX (Note 9)	UNIT
Power Supply Voltage Range	V_S	(V+ to V-) (Note 7)	**4**		**31**	V
Nominal Current Output	I_O			298.1		µA
Ambient Error Accuracy	E		**-0.50**	-0.05	**0.50**	°C
Current Output Temperature Coefficient	TCI_O			1		µA/K
Absolute Error without External Calibration	E_A	Over full temperature range	**-2.0**		**2.0**	°C
Nonlinearity	NL	At 5 discrete temperature points	**-0.5**		**0.5**	°C
Repeatability	RPT	After temperature range end point cycling	-0.1		0.1	°C
Long Term Drift	dE/dt	V+ = 31V for 1khr at +125°C	-0.25	-0.05	0.25	°C
Output Current V_S Rejection	PSRR	5V ≥ V_S ≥ 4V		0.05	**0.50**	µA/V
		5V ≤ V_S ≤ 15V		0.03	**0.20**	µA/V
		5V ≤ V_S ≤ 31V		0.04	**0.10**	µA/V
Voltage Noise Density	V_{nd}	f = 100Hz		0.03		µV/√Hz
Current Noise Density	I_{nd}	f = 100Hz		30		pA/√Hz
Case Isolation to Either Lead	Iso	Case to lead voltage = 200V		10^{10}		Ω
Effective Shunt Capacitance	C_S	f = 10Hz		65		pF
Electrical Turn-On Time	t_{ON}	V_S = 4V to I_{OUT} stable		2		µs
-10V Reverse Bias Leakage Current	I_{LEAK}	+125°C = Worst case		50		nA
POST RADIATION						
Post Low Dose Rate Radiation (LDR) Ambient Error 50krad at 0.01rad(Si)/s	E_{RADD} (Figure 19)	Ambient error accuracy plus TID shift (Note 10)	**-2.0**		**0.5**	°C
Post High Dose Rate Radiation (HDR) Ambient Error 300krad at 70rad(Si)/s		Ambient error accuracy plus TID shift (Note 10) (ISL71590SEH only)	**-2.0**		**0.5**	°C

NOTES:

9. Compliance to datasheet limits is assured by one or more methods: production test, characterization, and/or design.
10. The post radiation Ambient Error specs are defined as the absolute temperature error.

TABLE 2. BURN-IN AND LIFE TEST DELTA PARAMETERS

PARAMETER	SYMBOL	BURN-IN END POINT	BURN-IN DELTA	MIL-STD GROUP C END POINT	MIL-STD GROUP C DELTA	UNITS
Ambient Error (+25°C)	E	±0.5	±0.25	±0.5	±0.25	°C

Typical Performance Curves

Unless otherwise specified, V_S = 5V, T_A = +25°C.

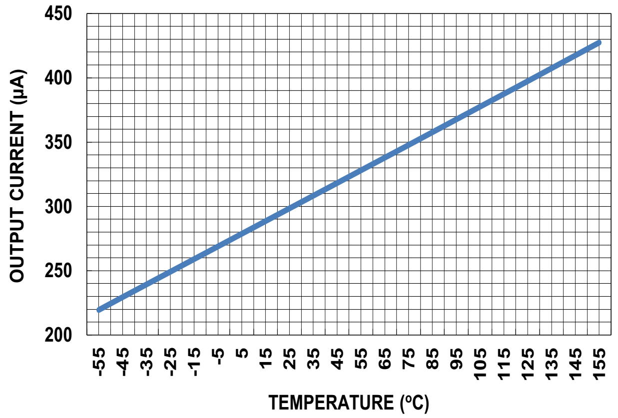


FIGURE 6. OUTPUT CURRENT vs TEMPERATURE

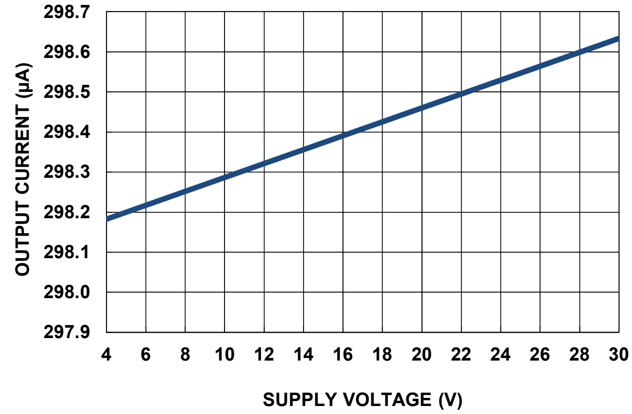


FIGURE 7. OUTPUT CURRENT vs V_S VOLTAGE

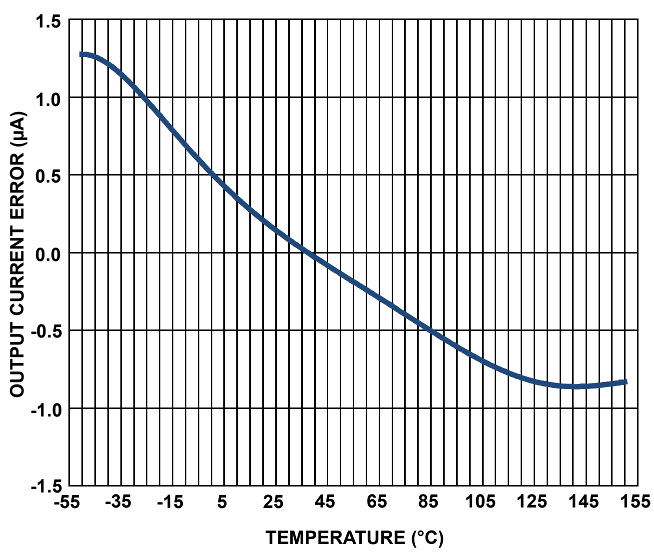


FIGURE 8. TYPICAL ABSOLUTE ERROR WITHOUT EXTERNAL CALIBRATION vs TEMPERATURE

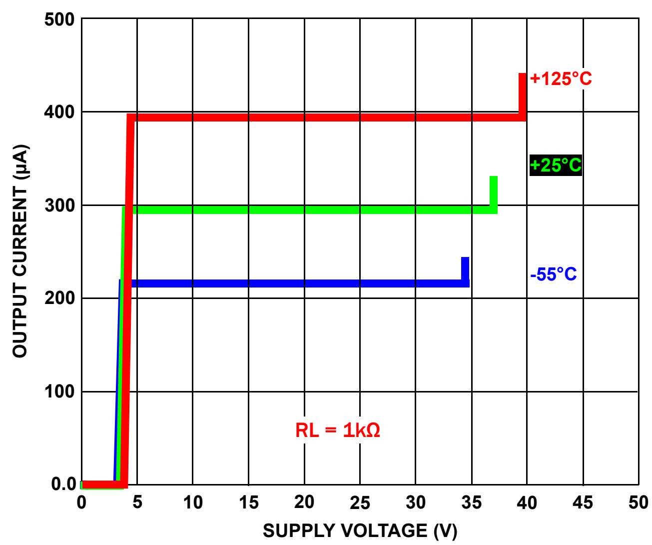


FIGURE 9. VI CURVE OF V_S vs I_{OUT} OVER-TEMPERATURE

Typical Performance Curves

Unless otherwise specified, V_S = 5V, T_A = +25°C. (Continued)

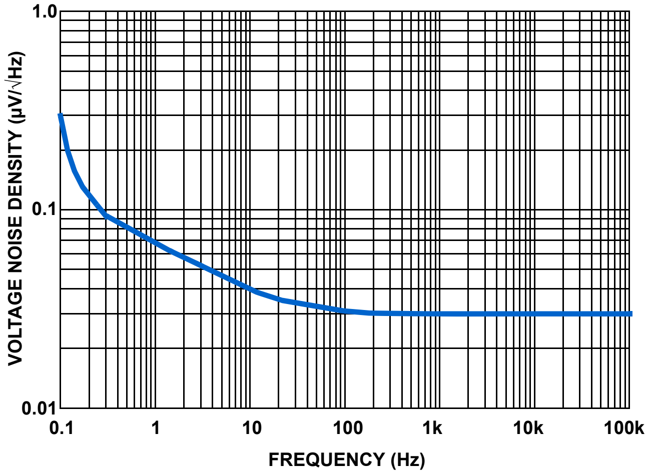


FIGURE 10. VOLTAGE NOISE DENSITY vs FREQUENCY

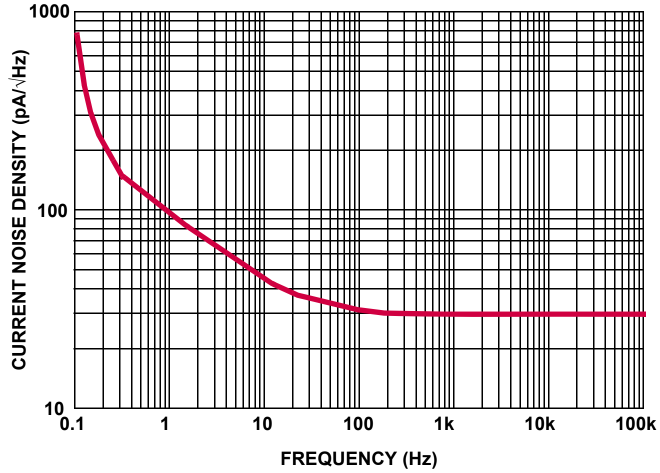


FIGURE 11. CURRENT NOISE DENSITY vs FREQUENCY

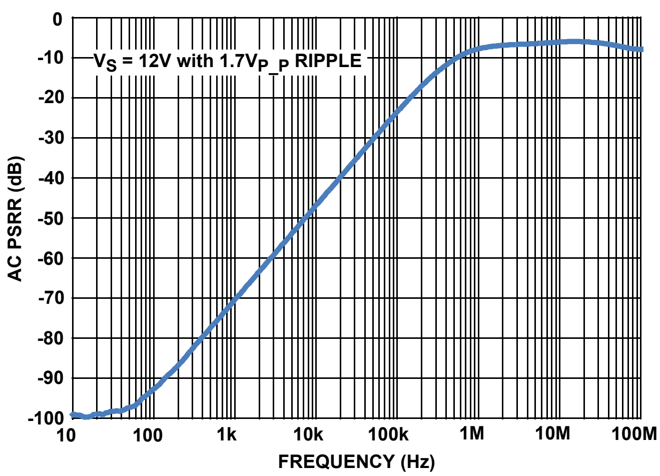


FIGURE 12. AC PSRR vs FREQUENCY

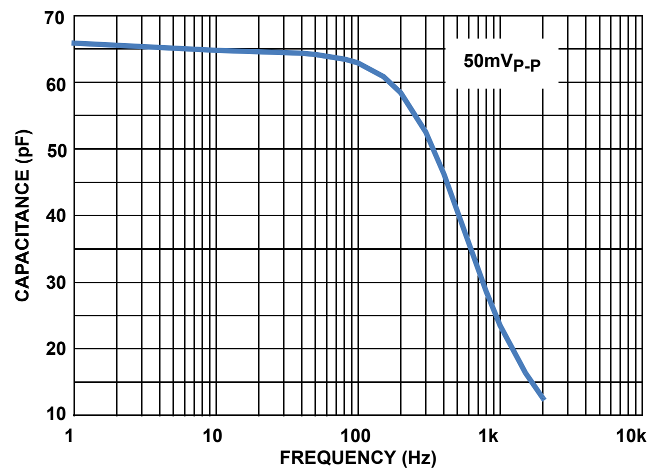


FIGURE 13. SHUNT CAPACITANCE vs FREQUENCY

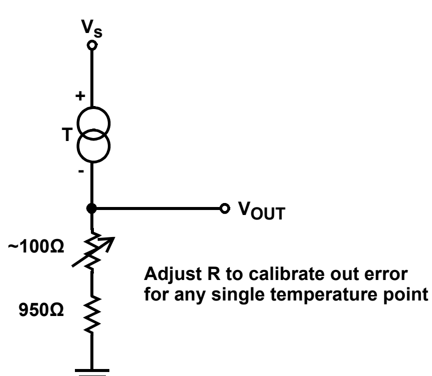


FIGURE 14. SINGLE TEMPERATURE ERROR CALIBRATION

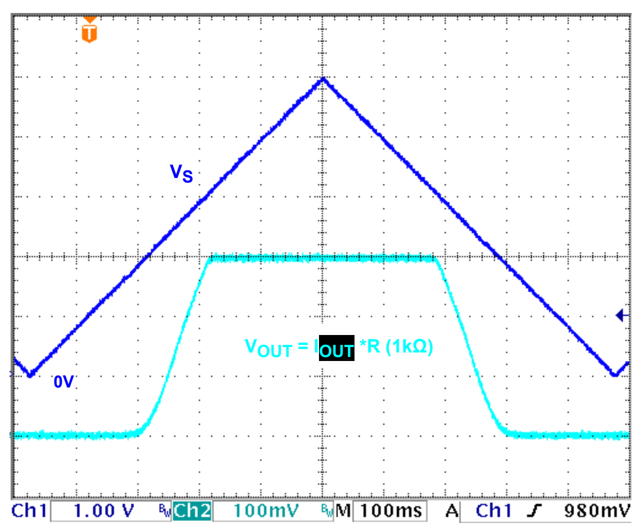


FIGURE 15. TURN-ON/OFF V_S VOLTAGE

Typical Performance Curves
Unless otherwise specified, V_S = 5V, T_A = +25°C. **(Continued)**

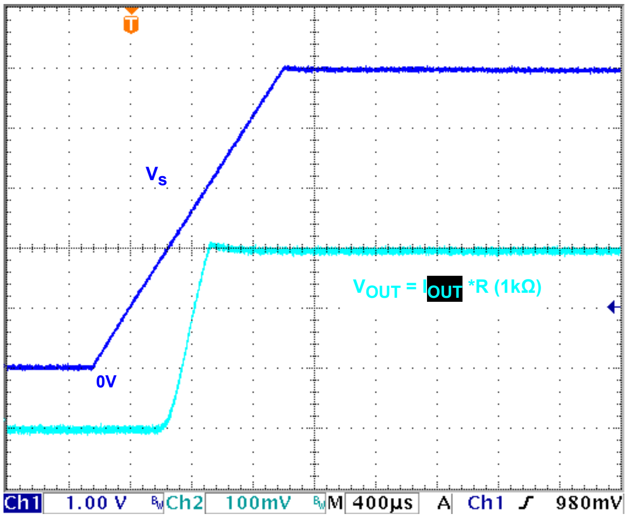


FIGURE 16. V_S RAMP = 3.7V/ms, I_{OUT} TURN-ON

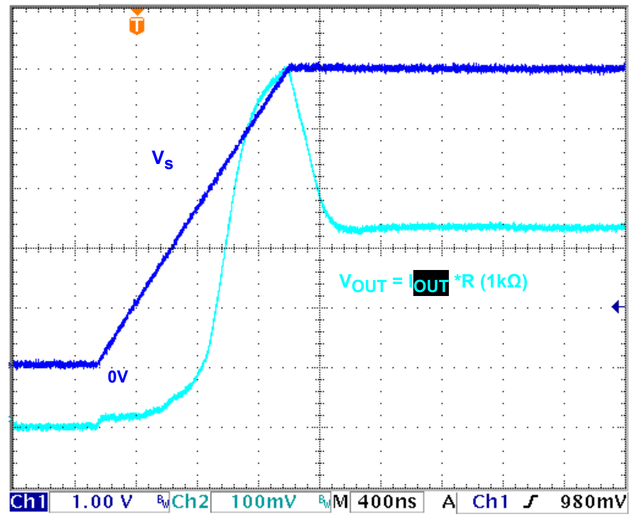


FIGURE 17. V_S RAMP = 5V/µs, I_{OUT} TURN-ON

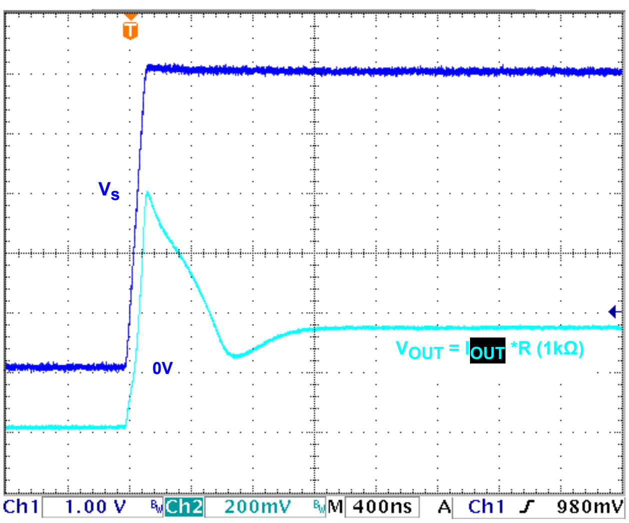


FIGURE 18. V_S RAMP = 50V/µs, I_{OUT} TURN-ON

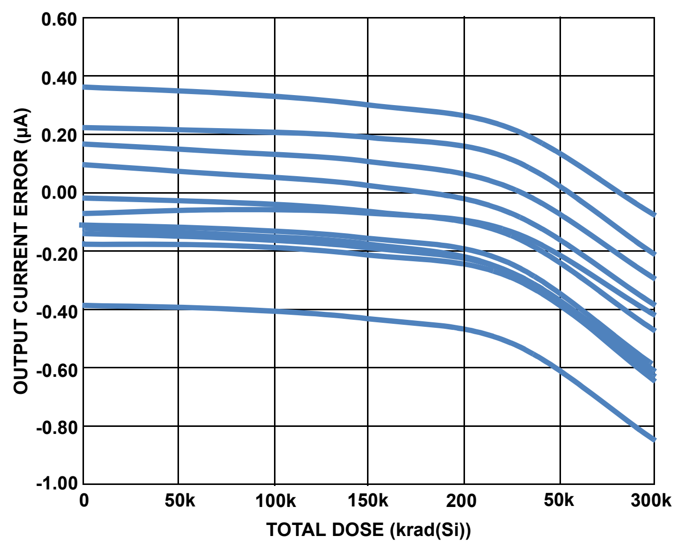


FIGURE 19. TYPICAL ABSOLUTE I_{OUT} ERROR vs TOTAL IONIZING DOSE FOR HIGH DOSE RATE (ISL71590SEH ONLY)

Functional Description

Functional Overview

The ISL71590SEH and ISL73590SEH are integrated-circuit, temperature-to-current transducers, which produce an output current proportional to absolute temperature. The devices act as high impedance constant current regulators passing 1µA/K for supply voltages (V+ to V-) from +4V to +33V.

The ISL71590SEH is assurance tested at low dose rate to 50krad(Si) and high dose rate to 300krad(Si). The ISL73590SEH is only low dose rate assurance tested to 50krad(Si). Both were SEE characterized at an LET = 86.4MeV•cm2/mg.

These devices are manufactured in the Renesas PR40, silicon-on-insulator process, which makes them immune to single event latch-up and provides excellent radiation tolerance. This makes them an ideal choice for high reliability applications in harsh radiation prone environments.

These devices are specified across temperatures of -55°C to +125°C without the need for additional circuitry to produce an output within ±1.7°C accuracy. With power requirements as low as 1.5mW (5V at +25°C), they are an ideal choice for remote sensing as any length of a well-insulated twisted pair cable will allow for proper operation. The high output impedance (>10MΩ) leaves plenty of room for variations in the power supply voltage. They are electrically durable since they can withstand a forward operating voltage of 33V over the full temperature range with and without ion beam radiation and a reverse voltage of -40V.

These devices should be used in any temperature sensing application from -55°C to +150°C in which conventional electrical temperature sensors are currently employed. These devices provide a total temperature sensing solution that is both low in complexity and small in size by eliminating the support circuitry necessary with other thermal sensors such as thermistors, thermocouples, and other discrete-based solutions. External linearization circuitry, precision voltage amplifiers, resistance measuring circuitry, and cold junction compensation are not needed when applying the ISL71590SEH or ISL73590SEH.

In the simplest application, the ISL71590SEH or ISL73590SEH, a resistor, a power source, and any voltmeter can be used to measure temperature. Ideally resistors used should be of a metal film or metal strip type, such resistors having very low thermal coefficient values.

When voltage is initially applied, the circuit becomes active at slightly less than 4V (V+ to V-), with I_{OUT} ramping up typically 2µs after. There will be an initial short period of time for the I_{OUT} to be correctly proportional to the ambient temperature. Depending on the V_S ramp rate and amplitude, this may take a few µs before a reliable temperature reading is available. See Figures 15 through 18 for scope shot examples.

The output characteristics also make the ISL71590SEH or ISL73590SEH easy to multiplex; with either or both the input supply voltage or the output current can be switched by a CMOS multiplexer such as the HS-508 or HS-1840 from Renesas.

When the die product is used, the die substrate should be tied to the more negative of the two terminals for optimum performance.

Parameter Glossary

The parametric specifications provide for an understanding of the temperature sensor performance over-temperature and radiation exposure. Following are critical parameter explanations as they relate to usage and interpretation.

Ambient Error Accuracy refers to the maximum error at an ambient temperature of +25°C and is expressed as ±0.5°C of the **Nominal Current Output** at +25°C (298.15K) of 298.15µA.

The **Absolute Error without External Calibration** describes the temperature accuracy over the entire -55°C to +125°C range. The typical performance is shown in Figure 8 on page 5. Both of these two first specification explanations are to be considered as initial error accuracy specifications.

The **Post Radiation Ambient Error** (E_{RADD}) is the specified accuracy after 50krad(Si) at 0.01rad(Si) per second (LDR) and 300krad(Si) at 70rad(Si) per second (HDR) exposure. This radiation hardness performance is unmatched in the industry for this class of device. This performance is shown in Figure 2 on page 1 as a delta over radiation type and in Figure 19 on page 7 as an absolute measurement.

Nonlinearity, in reference to the these devices, is the maximum allowable deviation of the output current over-temperature for any single part relative to its individual best fit line over five discrete temperature points (-55°C, -15°C, +25°C, +85°C, +125°C). This performance is assured by testing.

Repeatability Errors arise from a strain hysteresis of the package. For the ISL71590SEH and ISL73590SEH this is the maximum deviation between +25°C readings after a single temperature excursion between -55°C and +125°C, and is assured by characterization and is not tested. The magnitude of this error is solely a function of the magnitude of the temperature span and duration over which the device is exposed.

Long Term Drift Errors are related to the average operating temperature and the magnitude of the thermal shocks experienced by the device. Extended use of the ISL7x590SEH temperatures at +125°C typically results in long-term drift of –0.05°C after 1khr with a specification of - 0.25°C to +0.25°C.

Trimming Out Errors

The ideal graph of current versus temperature for the ISL7x590SEH is a straight line, but as Figure 20 on page 9 shows, the actual shape is slightly different (exaggerated greatly for explanation). Since the sensor is limited to the range of -55°C to +150°C, it is possible to optimize the accuracy by trimming. Trimming extracts the maximum performance from the sensor.

The circuit in Figure 21 on page 9 trims the slope of the ISL71590SEH output. The effect of this is shown in Figure 22 on page 9.

The circuit of Figure 23 on page 9 trims both the slope and the offset. Starting in Figure 24 on page 9 with an untrimmed slope, then progressing through to Figure 27 on page 10, each figure shows the effect of adjusting the offset and slope and finally, the offset again, to arrive at an optimized condition.

The diagrams' curvatures are highly are exaggerated to show effects, but it should be clear that these trims can be used to minimize errors over a partial or the entire temperature range.

Trimming Out Errors

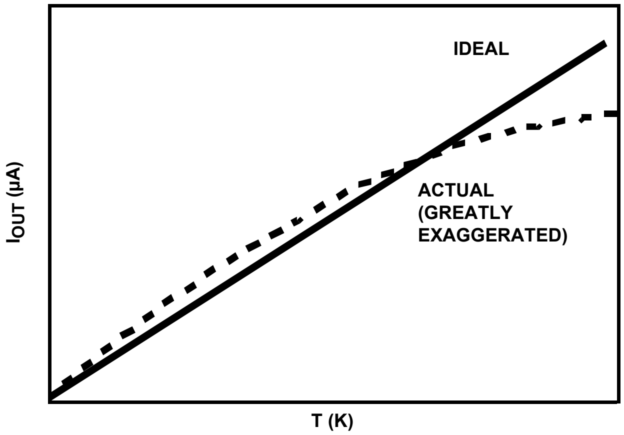


FIGURE 20. TRIMMING OUT ERRORS

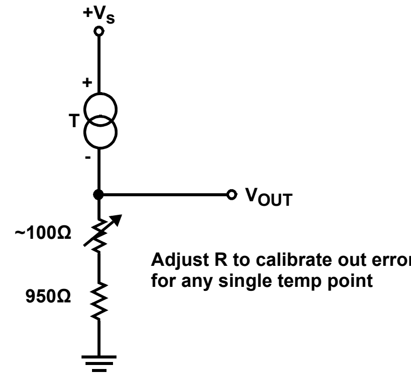


FIGURE 21. SLOPE TRIMMING

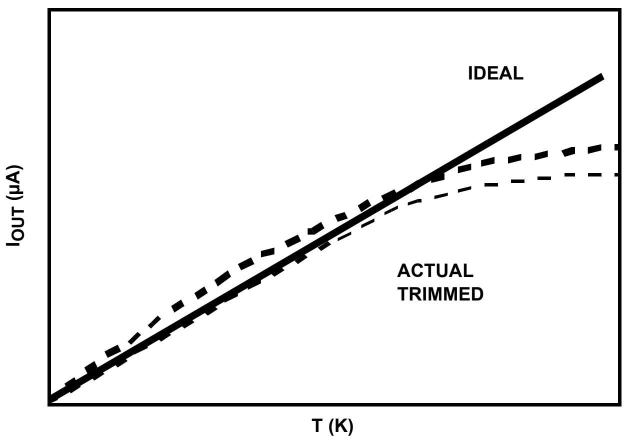


FIGURE 22. EFFECT OF SLOPE TRIM

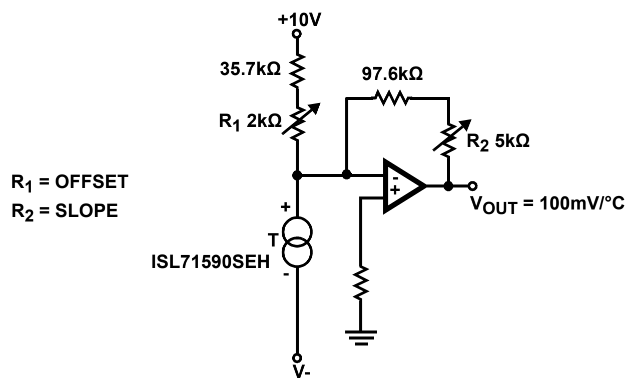


FIGURE 23. SLOPE AND OFFSET TRIMMING

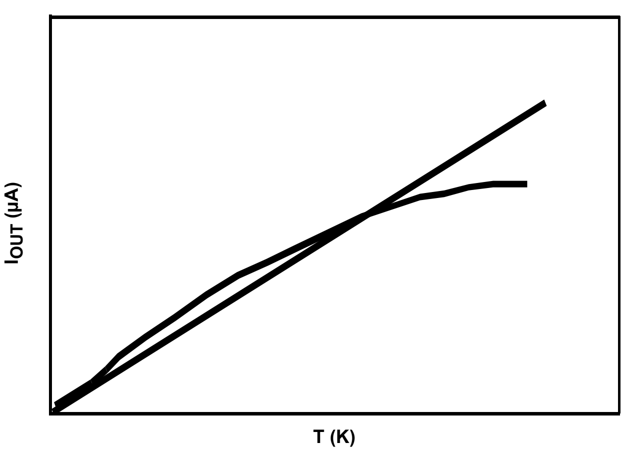


FIGURE 24. UNTRIMMED

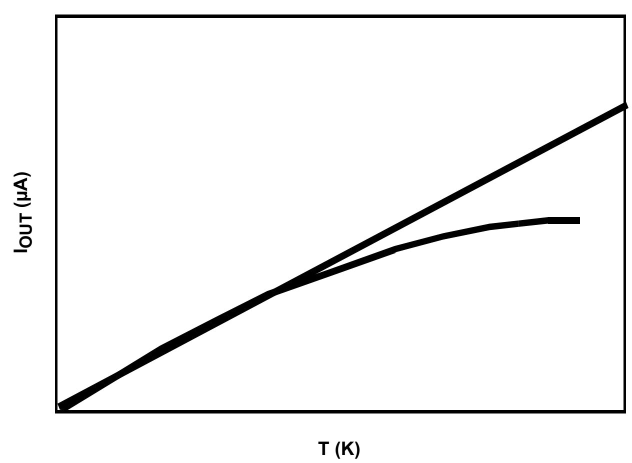


FIGURE 25. TRIM ONE: OFFSET

Trimming Out Errors (Continued)

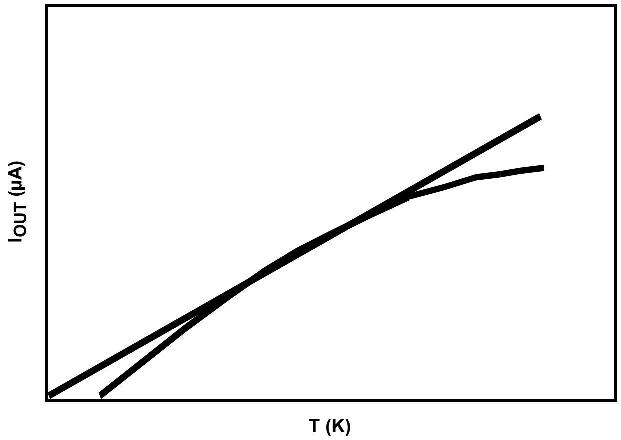


FIGURE 26. TRIM TWO: SLOPE

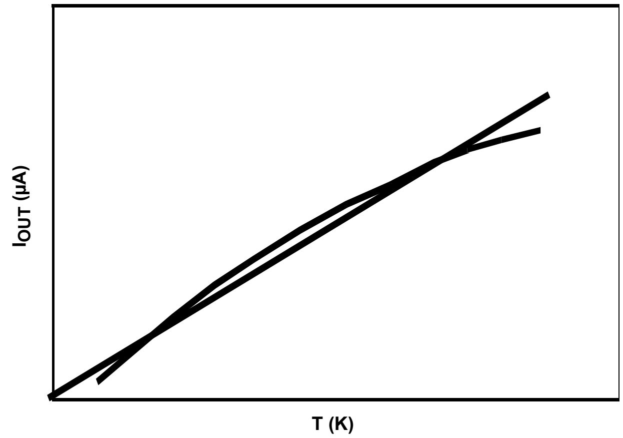


FIGURE 27. TRIM THREE: OFFSET AGAIN

Typical Applications

The following section of the datasheet illustrates several application ideas, touching on each with a short explanation. All of this material is applicable to both the ISL71590SEH and the ISL73590SEH devices.

There is an evaluation board ISL71590SEHEV1Z and accompanying user guide "ISL71590SEH Evaluation Board User's Guide" that details four of the more fundamental implementations of this device.

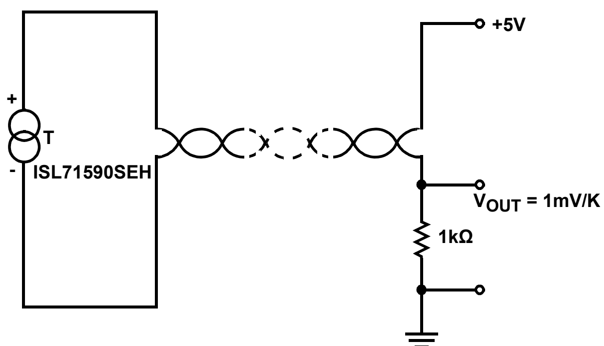


FIGURE 28. TYPICAL APPLICATION

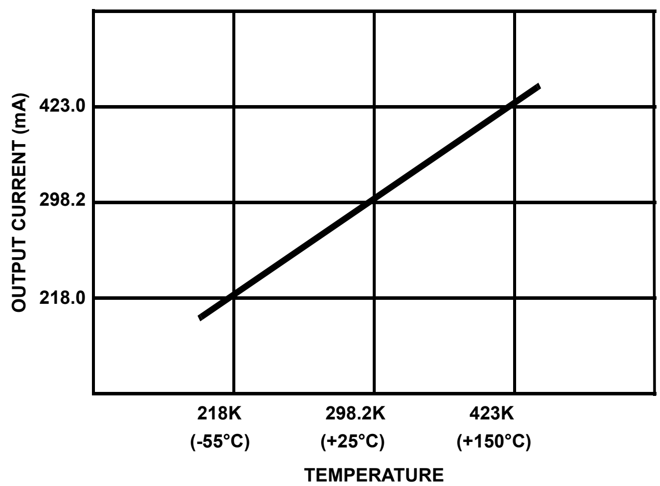


FIGURE 29. SIMPLE CONNECTION. OUTPUT IS PROPORTIONAL TO ABSOLUTE TEMPERATURE

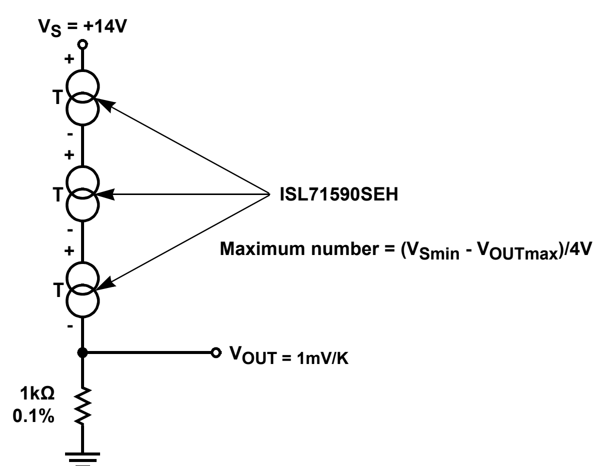
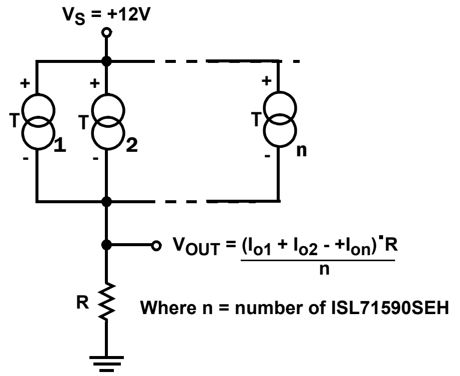


FIGURE 30. LOWEST TEMPERATURE SENSING SCHEME. OUTPUT CURRENT IS THAT OF THE "COLDEST" SENSOR



(e.g., with four sensors and R = 250Ω V_{OUT} = 1mV/K)

FIGURE 31. AVERAGE TEMPERATURE SENSING SCHEME

The sum of the ISL71590SEH currents appears across R, which represents the average temperature in the sensor array (see Figure 31).

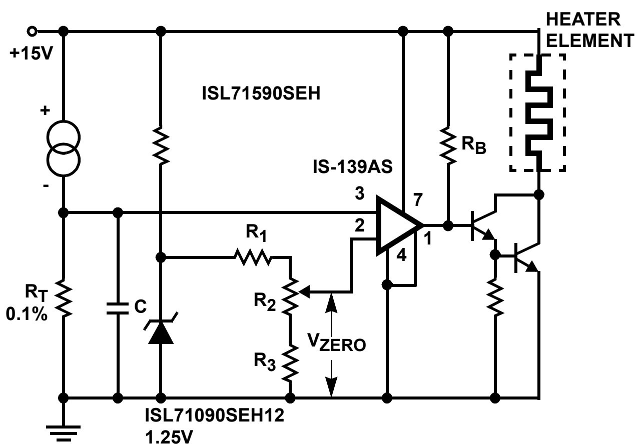


FIGURE 32. SINGLE SETPOINT TEMPERATURE CONTROLLER

In Figure 32, the ISL71590SEH produces a temperature-dependent voltage across R_T (C is for filtering noise). Setting R_2 produces a scale-zero voltage. For the Celsius scale, make R_T = 1kΩ and V_{ZERO} = 0.273V. For Fahrenheit, R_T = 1.8kΩ and V_{ZERO} = 0.460V.

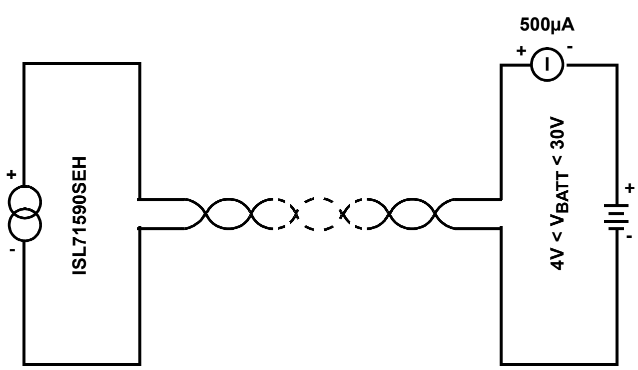


FIGURE 33. SIMPLEST THERMOMETER

Figure 33, illustrates the simplest thermometer displaying current output directly in Kelvin. Using the ISL71590SEH, sensor output is within ±1.7K over the entire range.

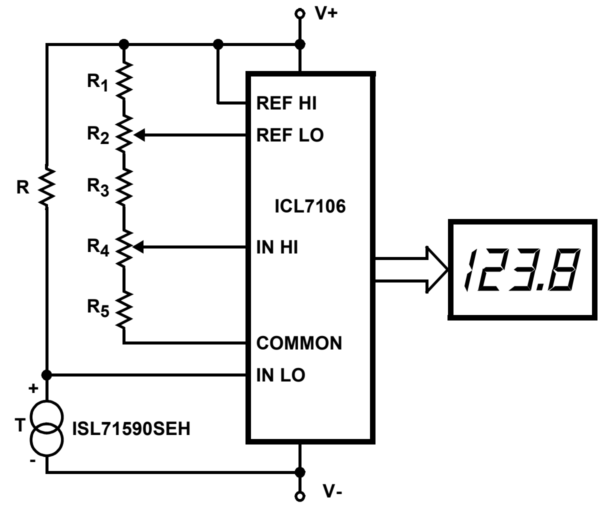


FIGURE 34. BASIC DIGITAL THERMOMETER, CELSIUS, AND FAHRENHEIT SCALES

TABLE 3.

	R	R_1	R_2	R_3	R_4	R_5
°F	9.00	4.02	2.0	12.4	10.0	0
°C	5.00	4.02	2.0	5.11	5.0	11.8

$$\sum_{n=1}^{5} R_n = 28k\Omega \text{ nominal} \quad \text{(EQ. 1)}$$

NOTE: ALL values are in kΩ.

In Figure 34, the ICL7106 has a V_{IN} span of ±2.0V and a V_{CM} range of (V+ - 0.5V) to (V- + 1V). R is scaled to bring each range within V_{CM} while not exceeding V_{IN}. The V_{REF} for both scales is 500mV, maximum reading on the Celsius range is +150°C limited by the maximum allowable sensor temperature. Maximum reading on the Fahrenheit range is +199.9°F (+93.3°C) limited by the number of display digits.

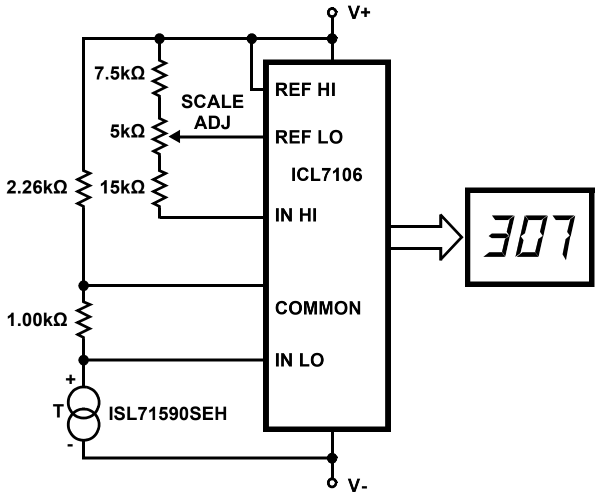


FIGURE 35. BASIC DIGITAL THERMOMETER, KELVIN SCALE

Figure 35, illustrates the Kelvin scale version reading from 0 to 1999K theoretically, and from 223K to 473K actually. The 2.26kΩ resistor brings the input within the ICL7106 V_{CM} range. Two general-purpose silicon diodes or an LED may be substituted.

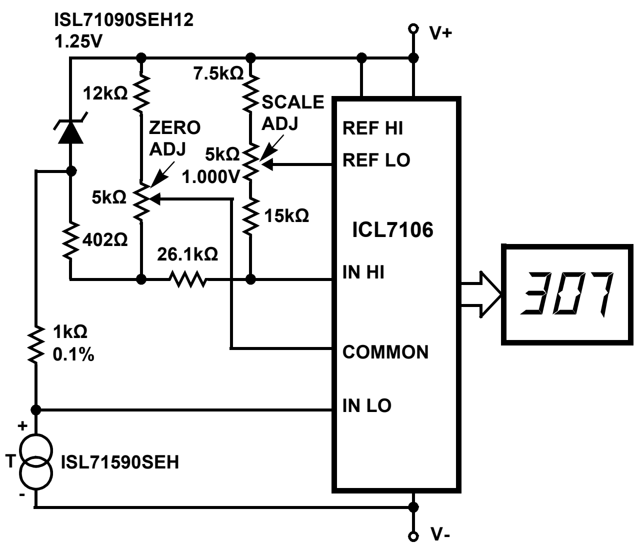


FIGURE 36. BASIC DIGITAL THERMOMETER, KELVIN SCALE WITH ZERO ADJUST

The circuit in Figure 36 allows "zero adjustment" as well as slope adjustment. The ISL71090SEH12 brings the input within the common-mode range, while the 5kΩ pots trim any offset at 218K (-55°C) and set the scale factor.

Since all three scales have narrow V_{IN} spans, some optimization of the ICL7106 components can be made to lower noise and preserve CMR. Table 4 shows the suggested values. Similar scaling can be used with the ICL7126 and ICL7136 (see Figures 34 through 36).

TABLE 4.

SCALE	V_{IN} RANGE (V)	RINT (kΩ)	CAZ (µF)
K	0.223 to 0.473	220	0.47
C	-0.25 to +1.0	220	0.1
F	-0.29 to +0.996	220	0.1

FOR ALL:
C_{REF} = 0.1µF
C_{INT} = 0.22µF
C_{OSC} =100pF
R_{OSC} = 100kΩ

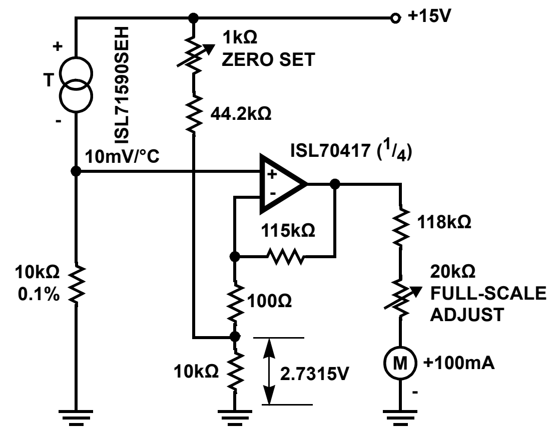


FIGURE 37. CENTIGRADE THERMOMETER (0°C TO +100°C)

Figure 37 illustrates the low bias current of the ISL70417, which allows the use of large value gain resistors and keeps the meter current error under 0.5%, therefore saving the expense of an extra meter driving amplifier.

Figure 38 shows a differential temperature sensing circuit configuration. The 50kΩ pot trims offset in the devices whether internal or external, so it can be used to set the size of the difference interval. This also makes it useful for liquid level detection where there will be a measurable temperature difference.

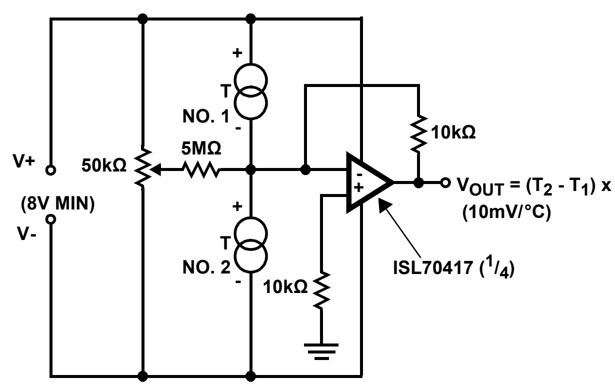


FIGURE 38. DIFFERENTIAL THERMOMETER

In Figure 39 the reference junction(s) should be in close thermal contact with the ISL71590SEH case. V+ must be at least 4V, while ISL71090SEH12 current should be set 1mA to 2mA. Calibration does not require shorting or removal of the thermocouple: set R_1 for V_2 = 10.98mV.
If very precise measurements are needed, adjust R_2 to the exact Seebeck coefficient for the thermocouple used (measured or from table) note V_1, and set R_1 to buck out this voltage (i.e., set $V_2 = V_1$).

For other thermocouple types, adjust values to the appropriate Seebeck coefficient.

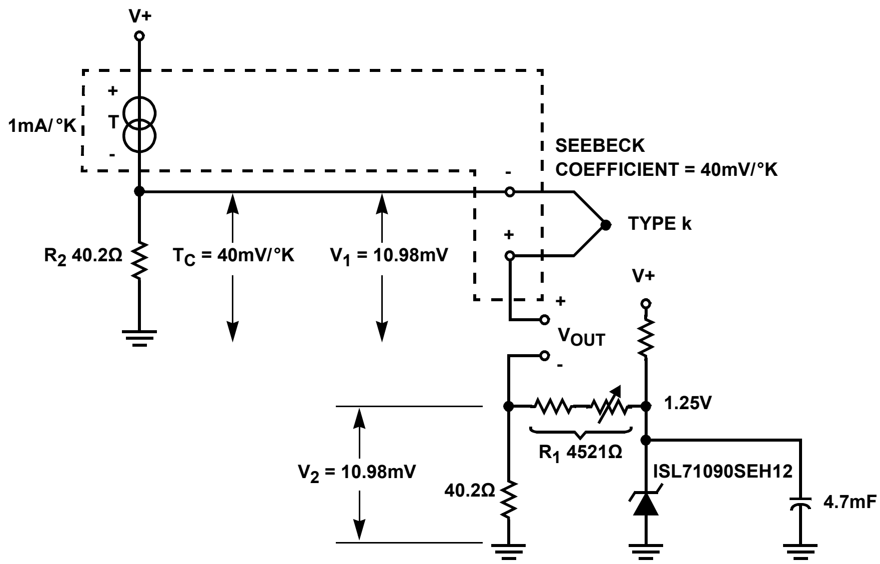


FIGURE 39. COLD JUNCTION COMPENSATION FOR TYPE K THERMOCOUPLE

Package Characteristics

Weight of Packaged Device

0. 07Grams (typical)

Lid Characteristics

Finish: Gold
Potential: Floating
Case Isolation to Any Lead: 10 x $10^9\Omega$ (minimum)

Die Characteristics

Die Dimensions

1185µm x 1695µm (46.7 mils x 66.7 mils)
Thickness: 254µm ±25.4µm (10 mils ±1 mil)

Interface Materials

GLASSIVATION

Type: Nitrox
Thickness: 15kÅ

TOP METALLIZATION

Type: AlCu (99.5%/0.5%)
Thickness: 30kÅ

BACKSIDE FINISH

Silicon

ASSEMBLY RELATED INFORMATION

SUBSTRATE POTENTIAL

Tied to V- pin

ADDITIONAL INFORMATION

WORST CASE CURRENT DENSITY

$<5 \times 10^3 A/cm^2$

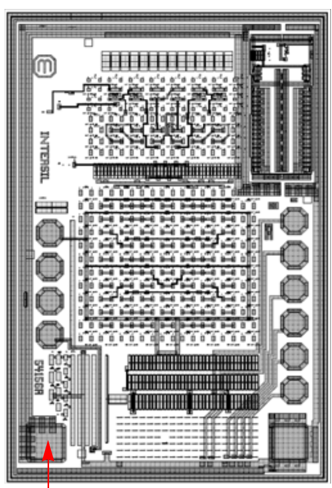
PROCESS

Dielectrically Isolated Bipolar SOI - PR40

TRANSISTOR COUNT

92

Metallization Mask Layout



V+ (1)   V- (2)

TABLE 5.

PAD NAME	PIN NUMBER	X (µm)	Y (µm)	ΔX (µm)	ΔY (µm)	BOND WIRES PER PAD
V+	1	0	0	110	110	1
V-	2	823	0	110	110	1

NOTES:

11. Origin of coordinates is the centroid of pad 1.
12. Bond wire size is 1.25 mil.

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please visit our website to make sure you have the latest revision.

DATE	REVISION	CHANGE
Sep 14, 2018	FN8376.3	Added Table 1 on page 1. Updated Related Literature section. Added ISL73590SEH information throughout document. Added Notes 3 and 4. Applied new Header/Footer. Removed About Intersil. Updated Disclaimer.
Jun 3, 2016	FN8376.2	Clarified minimum differential voltage throughout document. Replaced figures 5 and 6.
Jan 19, 2016	FN8376.1	Removed Pb-Free Reflow reference from “Thermal Information” on page 4 as it is not applicable to hermetic packages. In “Electrical Specifications” on page 4: -Updated EA maximum and minimum limits. -Updated ERADD Low Dose minimum limits. -Updated ERADD High Dose minimum limits. Updated About Intersil Section.
Sep 26, 2013	FN8376.0	Initial Release

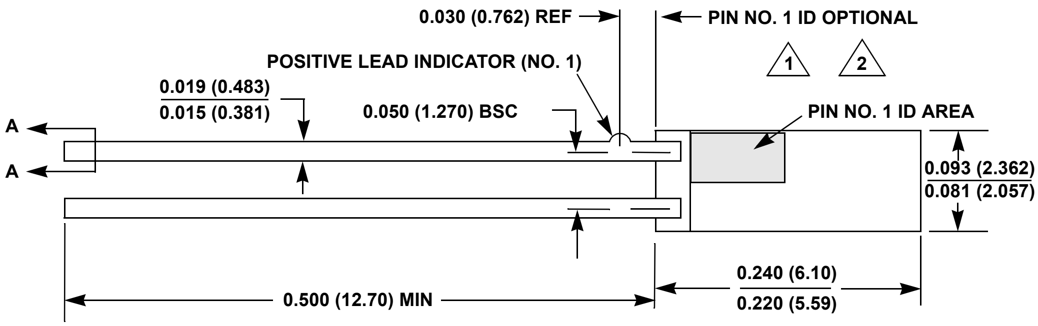
Package Outline Drawing

For the most recent package outline drawing, see K2.A.

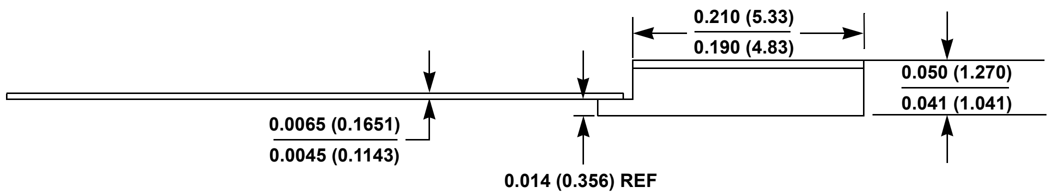
K2.A

2 LEAD CERAMIC METAL SEAL FLATPACK PACKAGE

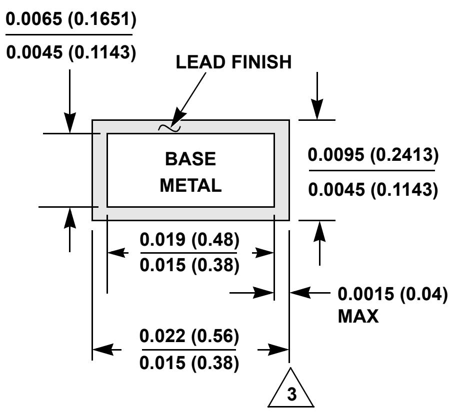
Rev 1, 4/12



TOP VIEW



SIDE VIEW



SECTION A-A

NOTES:

1. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark. Alternately, a tab may be used to identify pin one.
2. If a pin one identification mark is used in addition to a tab, the limits of the tab dimension do not apply.
3. The maximum limits of lead dimensions (section A-A) shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.
4. Dimensioning and tolerancing conform to ANSI Y14.5M-1982.
5. Dimensions: Inch (mm). Controlling dimension: Inch.

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