ISL70023SEH, ISL73023SEH

100V, 60A Enhancement Mode GaN Power Transistor

FN8975
Rev.3.00
Aug 16, 2019

The ISL70023SEH and ISL73023SEH are 100V N-channel enhancement mode GaN power transistors. These GaN FETs have been characterized for destructive Single Event Effects (SEE) and tested for Total Ionizing Dose (TID) radiation. Applications for these devices include commercial aerospace, medical, and nuclear power generation.

GaN's exceptionally high electron mobility and low temperature coefficient allows for very low $r_{DS(ON)}$, while its lateral device structure and majority carrier diode provide exceptionally low Q_G and zero Q_{RR}. The end result is a device that can operate at a higher switching frequency with more efficiency while reducing the overall solution size.

By combining the exceptional performance of the GaN FET in a hermetically sealed Surface Mount Device (SMD) package with manufacturing in a MIL-PRF-38535 like flow results in best-in-class power transistors that are ideally suited for high reliability applications.

Applications

- Switching regulation
- Motor drives
- Relay drives
- Inrush protection
- Down hole drilling
- High reliability industrial

Features

- **Very low $r_{DS(ON)}$ 5mΩ (typical)**
- **Ultra low total gate charge 14nC (typical)**
- SEE hardness (see SEE report for details)
  - SEL/SEB LET_{TH} (V_{DS} = 100V, V_{GS} = 0V): 86MeV•cm^2/mg
- ISL70023SEH radiation accepting testing
  - High dose rate (50-300rad(Si)/s): 100krad(Si)
  - Low dose rate (0.01rad(Si)/s): 75krad(Si)
- ISL73023SEH radiation accepting testing
  - Low dose rate (0.01rad(Si)/s): 75krad(Si)
- Ultra small hermetically sealed 4 Ld Surface Mount Device (SMD) package
  - Package area: 42mm^2
- Full military-temperature range operation
  - T_A = -55°C to +125°C
  - T_J = -55°C to +150°C

Related Literature

For a full list of related documents, visit our website

- ISL70023SEH, ISL73023SEH product pages

Figure 1. ISL70023SEH 4 Ld SMD Package

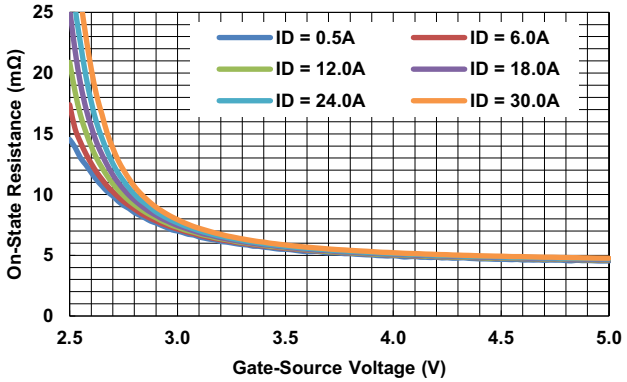


Figure 2. On-State Resistance (+25°C)

1. Overview

1.1 Ordering Information

Ordering Part Number (Note 1)	Radiation Hardness (Total Ionizing Dose)	Temperature Range (°C)	Package (RoHS Compliant)	Package Drawing
ISL70023SEHML	HDR to 100krad(Si) LDR to 75krad(Si)	-55 to +125	4 Ld SMD	J4.A
ISL73023SEHML	LDR to 75krad(Si)	-55 to +125	4 Ld SMD	J4.A
ISL70023SEHMX	HDR to 100krad(Si) LDR to 75krad(Si)	-55 to +125	Die	-
ISL73023SEHMX	LDR to 75krad(Si)	-55 to +125	Die	-
ISL70023SEHX/SAMPLE (Note 2)	N/A	+25	Die	-
ISL73023SEHX/SAMPLE (Note 2)	N/A	+25	Die	-
ISL70023SEHL/PROTO (Note 2)	N/A	-55 to +125	4 Ld SMD	J4.A
ISL73023SEHL/PROTO (Note 2)	N/A	-55 to +125	4 Ld SMD	J4.A

Notes:

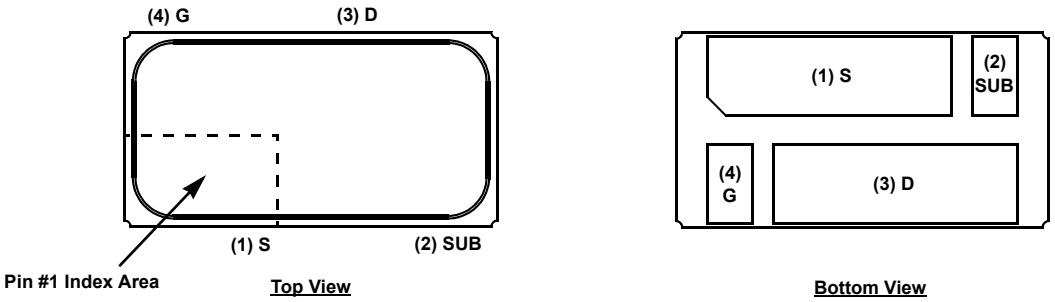
1. These Pb-free Hermetic packaged products employ 100% Au plate - e4 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations.
2. The /PROTO and /SAMPLE parts are not rated or certified for Total Ionizing Dose (TID) or Single Event Effect (SEE) immunity. These parts are intended for engineering evaluation purposes only. The /PROTO and /SAMPLE parts meet the electrical limits and conditions across the temperature range specified in this datasheet and are of the same form and fit as the ISL70023SEHML/ISL73023SEHML devices. The /PROTO and /SAMPLE parts do not come with a Certificate of Conformance (C of C) and have no accompanying data or documentation.

Table 1. Key Differences Between Family of Parts

Part Number	I_D (A)	$r_{DS(ON)}$ Typical (mΩ)	Breakdown Voltage	Radiation Assurance
ISL70023SEH	60	5	100V	HDR to 100krad(Si) LDR to 75krad(Si)
ISL73023SEH	60	5	100V	LDR to 75krad(Si)
ISL70024SEH	7.5	45	200V	HDR to 100krad(Si) LDR to 75krad(Si)
ISL73024SEH	7.5	45	200V	LDR to 75krad(Si)

1.2 Pin Configuration

ISL70023SEH, ISL73023SEH
(4 Ld SMD)



Note: The ESD triangular mark indicates Pin #1. It is a part of the device marking and is placed on the lid in the quadrant where Pin #1 is located.

1.3 Pin Descriptions

Pin Number	Pin Name	Description
1	S	Source connection for the GaN FET.
2	SUB	Substrate connection for the GaN FET which is internally shorted in to source. Tie this pin to source on the PCB.
3	D	Drain connection for the GaN FET
4	G	Gate connection for the GaN FET. Minimize trace inductance from driver to reduce over-stressing the gate.
NA	Lid	Internally tied to the source pin.

2. Specifications

2.1 Absolute Maximum Ratings

Parameter	Minimum	Maximum	Unit
V_{DS} (Note 3)	0	100	V
V_{GS}	-4	6	V
ESD Rating (Drain-to-Source)	**Value**		**Unit**
Human Body Model (Tested per MIL-STD-883 TM3015)	2		kV
Machine Model (Tested per JESD22-A115C)	200		V
Charged Device Model (Tested per JS-002-2014)	750		V
ESD Rating (Gate-to-Source)	**Value**		**Unit**
Human Body Model (Tested per MIL-STD-883 TM3015)	500		V
Machine Model (Tested per JESD22-A115C)	200		V
Charged Device Model (Tested per JS-002-2014)	750		V

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

Note:

3. Tested in a heavy ion environment at LET = 86.4MeV•cm^2/mg at +125°C (T_C)

2.2 Thermal Information

ISL70023SEH, ISL70023SEH in SMD Package J4.A			
Thermal Resistance	**Typical**	**Maximum**	**Unit**
θ_{JA} (Note 4)	23.0		°C/W
θ_{JC} (Note 5)	3.1	3.9	°C/W

Notes:

4. θ_{JA} is measured in free air with the component mounted on a high-effective thermal conductivity test board with “direct attach” features. See TB379.
5. For θ_{JC}, the “case temp” location is on the solder terminations adjacent to the center of the package underside.

Parameter	Minimum	Maximum	Unit
Maximum Junction Temperature	-	+150	°C
Storage Temperature Range	-65	+150	°C

2.3 Recommended Operating Conditions

Parameter	Minimum	Maximum	Unit
Temperature	-55	+125	°C
V_{DS}	0	80	V
I_D (V_{GS} = 5.0V, T_C = +25°C) (Note 6)	0	60	A
I_D (V_{GS} = 5.0V, T_C = +105°C) (Note 6)	0	35	A

Note:

6. T_J = +150°C. Current limited by package constraints.

2.4 Electrical Specifications

Unless otherwise noted, V_{DS} = 80V. **Boldface limits apply across the operating temperature range, -55°C to +125°C; over a total ionizing dose of 100krad(Si) with exposure at a high dose rate of 50-300rad(Si)/s (ISL70023SEH only); or over a total ionizing dose of 75krad(Si) with exposure at a low dose rate of <10mrad(Si)/s.**

Parameter	Symbol	Test Conditions	Min (Note 8)	Typ (Note 7)	Max (Note 8)	Unit
Static Characteristics						
Drain-to-Source Breakdown Voltage	BV_{DSS}	V_{GS} = 0V, I_D = 1.2mA	**100**	-	-	V
Drain-to-Source Leakage Current	I_{DSS}	V_{DS} = 80V, V_{GS} = 0V	-	0.1	**1.1**	mA
Drain-to-Gate Leakage Current	I_{GSX}	V_{DS} = 80V, V_{GS} = 0V	-	0.1	**0.7**	mA
Gate-to-Source Forward Leakage	I_{GSS}	V_{GS} = 5V	-	1	**9**	mA
Gate-to-Source Reverse Leakage		V_{GS} = -4V	**-0.7**	-0.1	-	mA
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 12mA	**0.7**	1.5	**2.5**	V
Drain-to-Source On-Resistance	$r_{DS(ON)}$	V_{GS} = 5V, I_D = 25A	-	5	**12**	mΩ
Source-to-Drain Forward Voltage	V_{SD}	I_S = 0.5A, V_{GS} = 0V,	**0.7**	1.8	**3.0**	V
Dynamic Characteristics						
Input Capacitance	C_{ISS}	V_{DS} = 50V, V_{GS} = 0V (Note 9)	-	1500	-	pF
Output Capacitance	C_{OSS}	V_{DS} = 50V, V_{GS} = 0V, T_A=+25°C	-	960	1250	pF
Gate Resistance	r_G	T_A = +25°C, (Note 9)	-	5	-	mΩ
Reverse Transfer Capacitance	C_{RSS}	V_{DS} = 50V, V_{GS} = 0V (Note 9)	-	18	-	pF
Total Gate Charge	Q_G	V_{DS} = 50V, I_D = 25A, V_{GS} = 5V, T_A = +25°C	-	14	25	nC
Gate Charge at Threshold	$Q_{G(th)}$	V_{DS} = 50V, I_D = 25A (Note 9)	-	2.6	-	nC
Gate-to-Drain Charge	Q_{GD}	V_{DS} = 50V, I_D = 25A, T_A = +25°C	-	5.5	12	nC
Gate-to-Source Charge	Q_{GS}	V_{DS} = 50V, I_D = 25A, T_A = +25°C	-	2.0	5	nC
Output Charge	Q_{OSS}	V_{DS} = 50V, V_{GS} = 0V (Note 9)	-	71	-	nC

Notes:

7. Typical values shown are not guaranteed.
8. Parameters with MIN and/or MAX limits are 100% tested at -55°C, +25°C, and +125°C, unless otherwise specified.
9. Limits are established by characterization and/or design, not tested.

3. Typical Performance Curves

Unless otherwise noted, V_{DS} = 80V; T_A = +25°C.

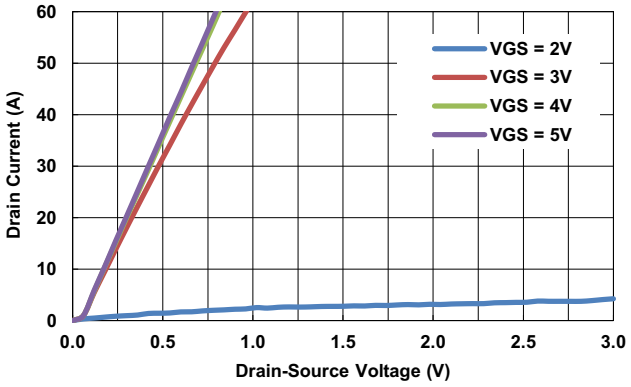


Figure 3. Output Characteristics (+25°C)

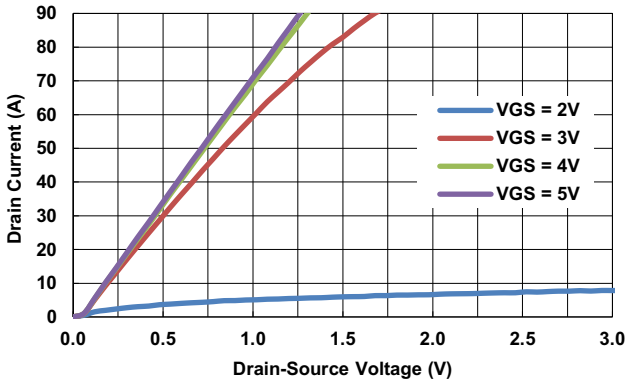


Figure 4. Output Characteristics (+125°C)

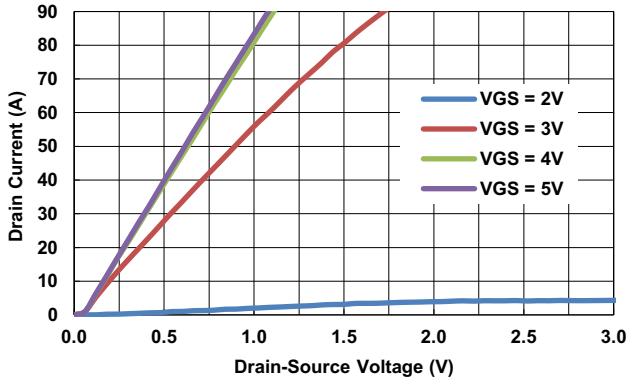


Figure 5. Output Characteristics (-55°C)

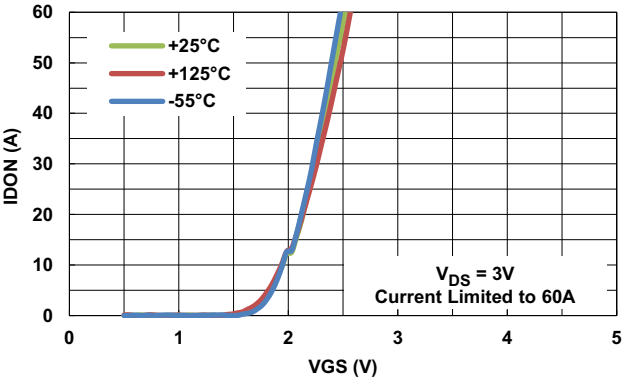


Figure 6. Transfer Characteristics

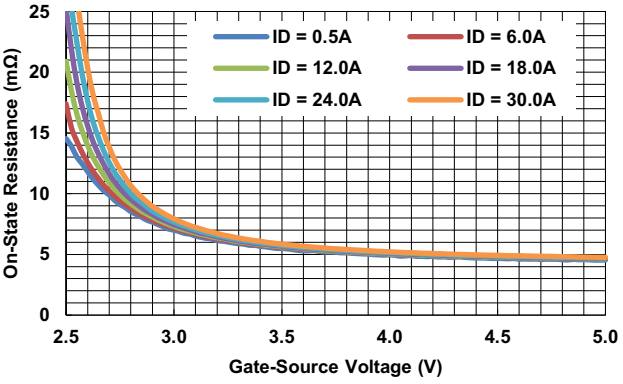


Figure 7. On-State Resistance (+25°C)

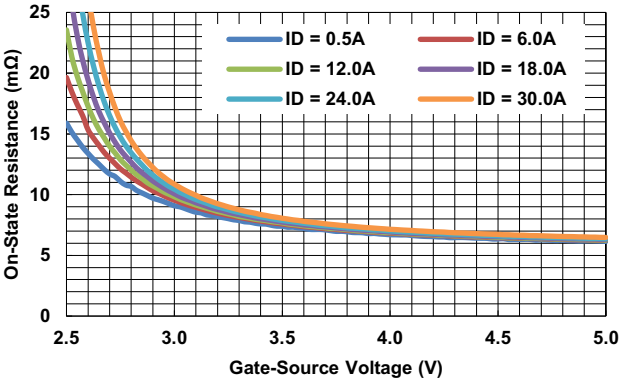


Figure 8. On-State Resistance (+125°C)

Unless otherwise noted, V_{DS} = 80V; T_A = +25°C. **(Continued)**

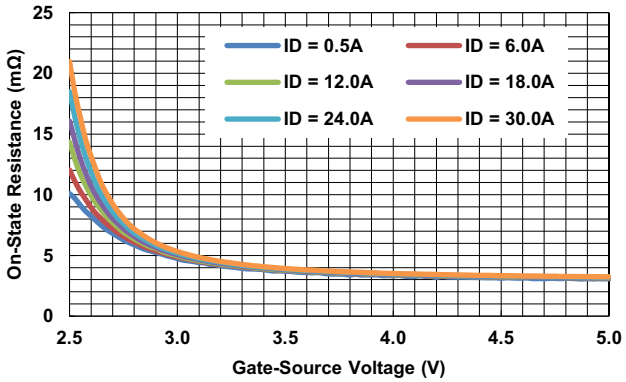


Figure 9. On-State Resistance (-55°C)

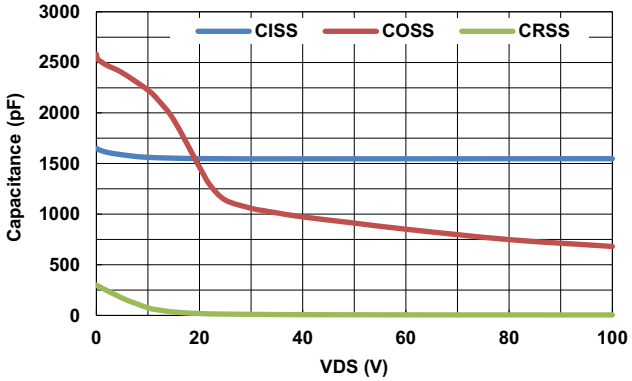


Figure 10. Capacitance (Linear Scale)

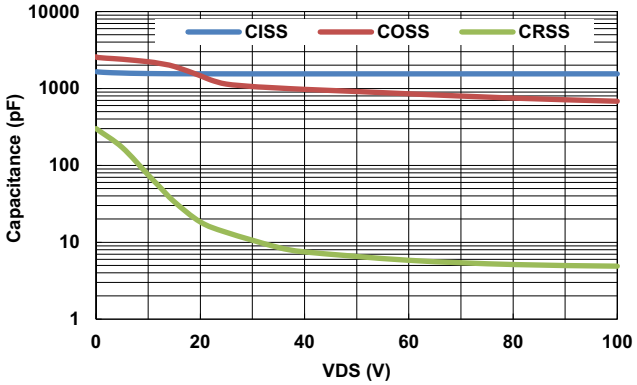


Figure 11. Capacitance (Log Scale)

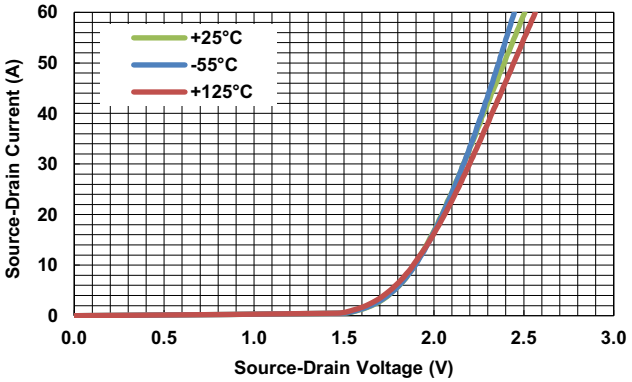


Figure 12. Reverse Drain-Source Characteristics

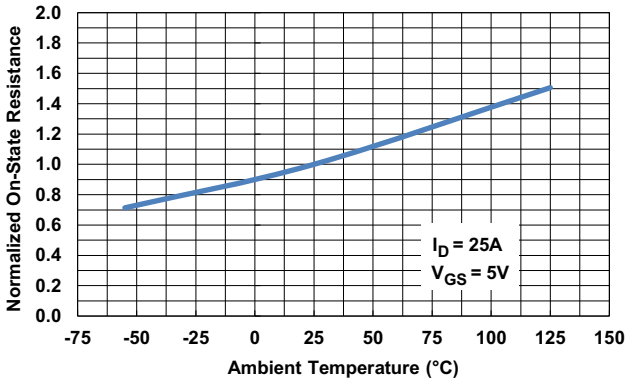


Figure 13. Normalized On-State Resistance

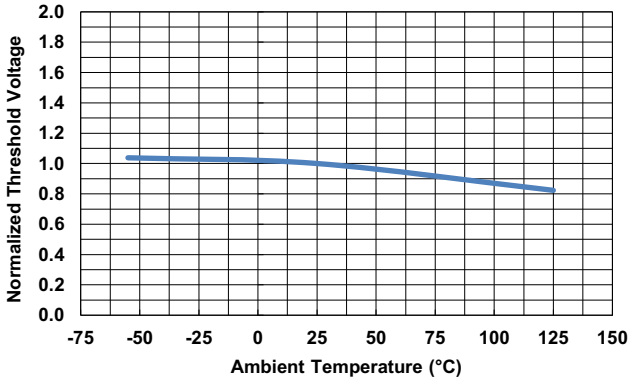


Figure 14. Normalized Threshold Voltage

Unless otherwise noted, V_{DS} = 80V; T_A = +25°C. **(Continued)**

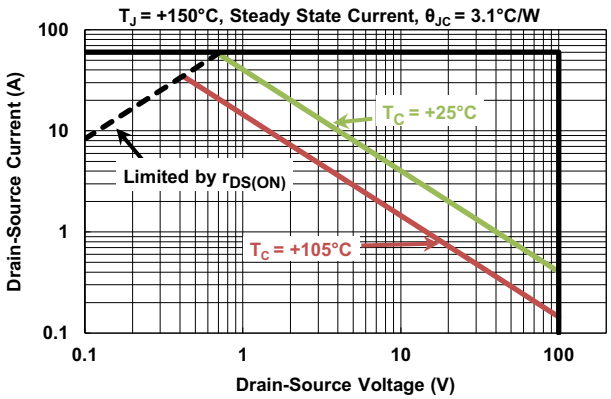


Figure 15. Safe Operating Area

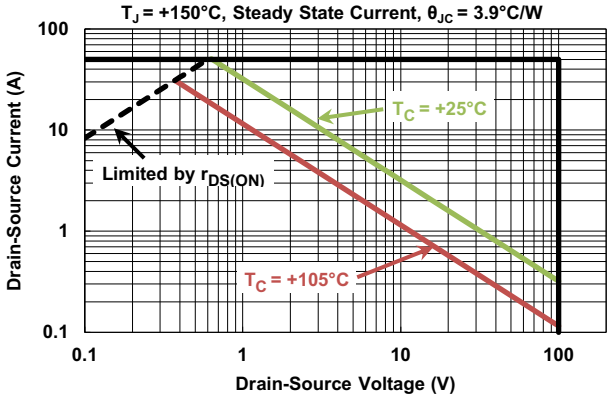


Figure 16. Safe Operating Area (Derated)

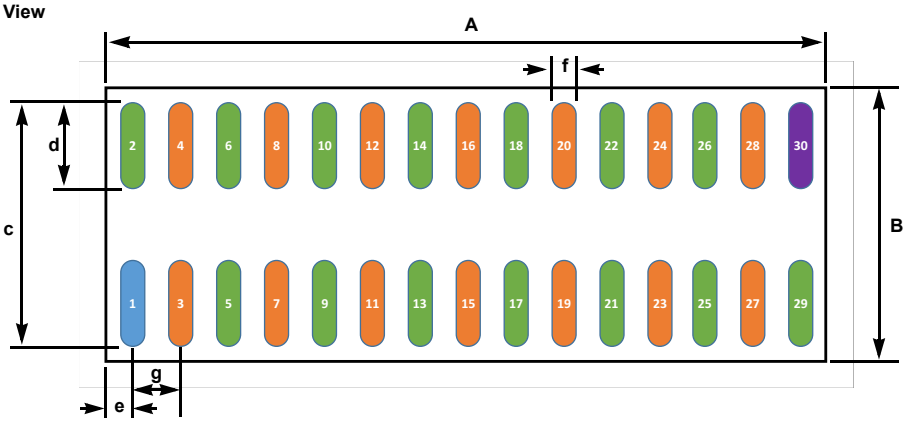
4. Die Characteristics

Table 2. Die and Assembly Related Information

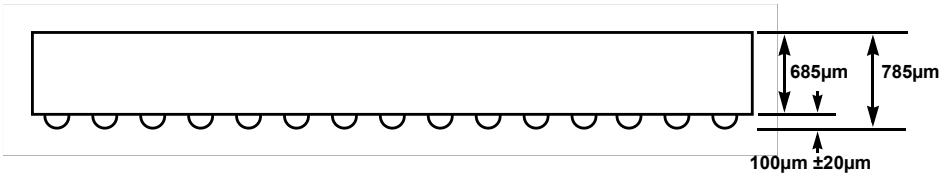
Die Information	
Dimensions	6050µm x 2300µm (238.19 mils x 90.55 mils) Thickness: 685µm (26.97 mils)

ISL70023SEH, ISL73023SEH

Solder Bump View



Side View



Color Key:

Pads in Green are the Source

Pads in Orange are the Drain

Pad in Blue is the Gate

Pad in Purple is the Substrate

Table 3. Dimensions

Dimension	Min (µm)	Nominal (µm)	Max (µm)
A	6020	6050	6080
B	2270	2300	2330
c	2047	2050	2053
d	717	720	723
e	210	225	240
f	195	200	205
g	400	400	400

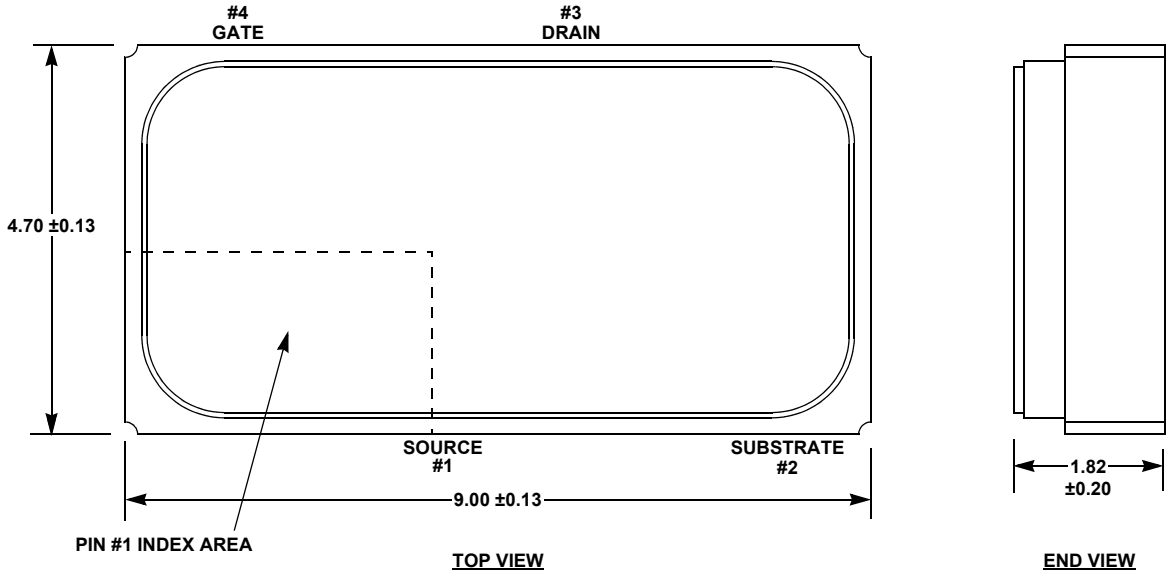
5. Revision History

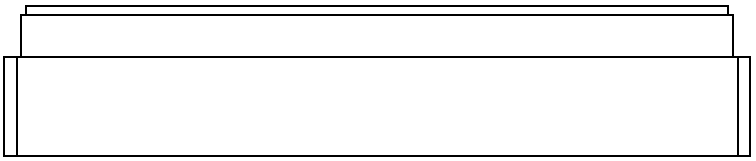
Rev.	Date	Description
3.00	Aug 16, 2019	Updated features section to include new radiation acceptance tolerance and SEE testing formatting. Updated Table 1. Updated disclaimer.
2.00	Mar 8, 2018	Updated ordering information table by correcting /SAMPLE part numbers and adding Die where applicable. Updated Section 4 heading from “Die and Assembly Characteristics” to “Die Characteristics”.
1.00	Jan 12, 2018	Updated Figure 1. Added ISL73023SEH part information throughout datasheet. Updated ordering information table. Updated Notes 2 and 9. Added Table 1 on page 3. Added Die and Assembly Characteristics section on page 10. Removed About Intersil section. Updated Disclaimer.
0.00	Oct 5, 2017	Initial release

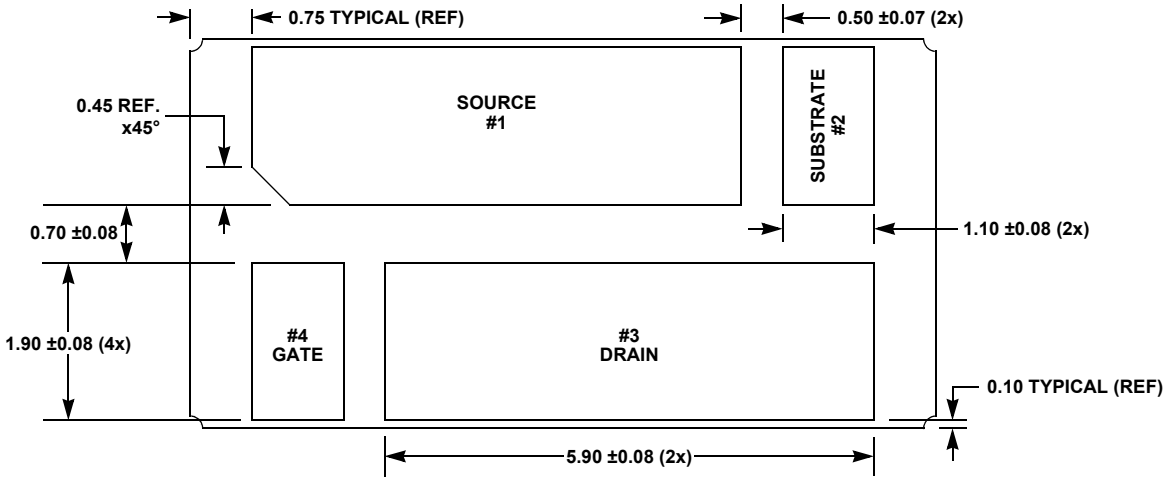
6. Package Outline Drawing

For the most recent package outline drawing, see J4.A.

J4.A
4 PIN 9.0mmx4.7mm HERMETIC SURFACE MOUNT PACKAGE
Rev 0, 2/16

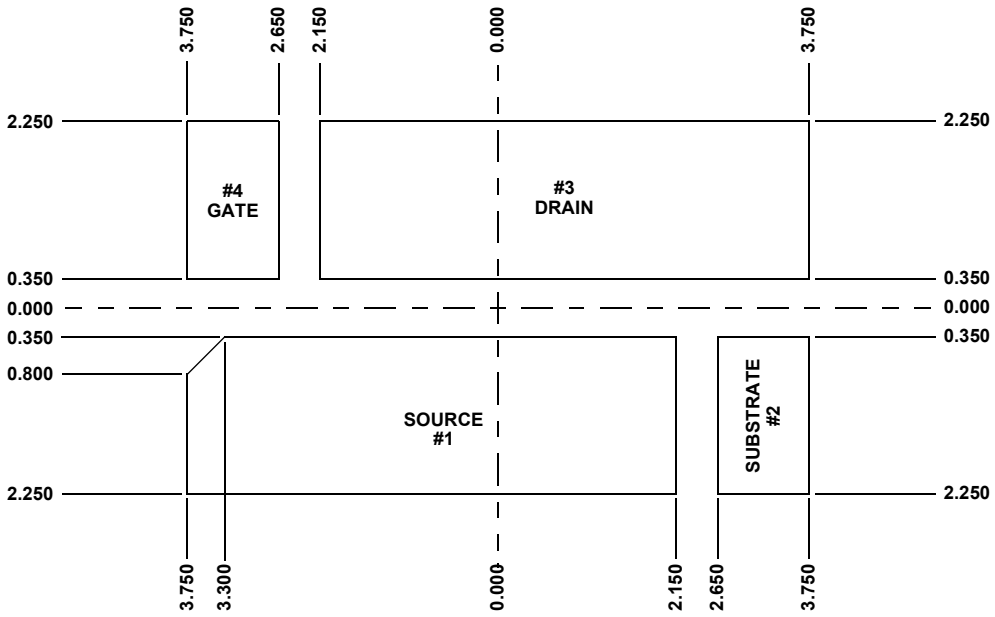






NOTES:

1. The corner shape (radius, chamfer, etc.) may vary at the manufacturers option from that shown on the drawing.
2. The package thickness dimension is the package height before being solder dipped.
3. Dimensions are in millimeters.



TYPICAL RECOMMENDED LAND PATTERN

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