

ISL59115

Triple Channel Video Driver with LPF

FN6185

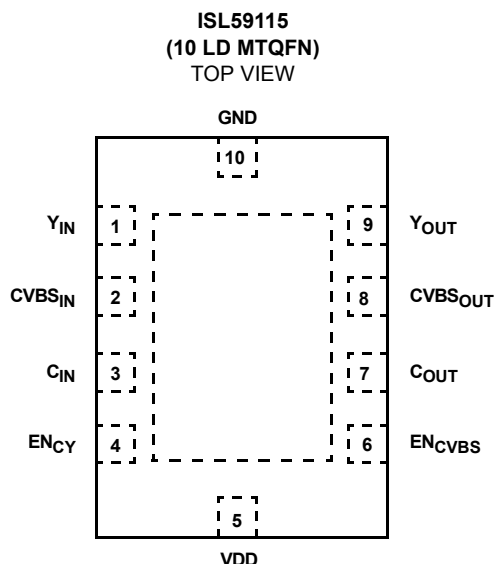
Rev 2.00

September 21, 2006

The ISL59115 is a triple channel reconstruction filter with a -3dB roll-off frequency of 9MHz. Operating from a single supply ranging from +2.5V to +3.6V and drawing only 4.5mA quiescent current, the ISL59115 is ideally suited for low power, battery-operated applications. Additionally, enable pins shut the part down in under 14ns.

The ISL59115 is designed to meet the bandwidth and very low power requirements of battery-operated communication, instrumentation, and modern industrial applications such as video on demand, cable set-top boxes, MP3 players, and HDTV. The ISL59115 is offered in a space-saving  $\mu$ TQFN Pb-free package guaranteed to a 0.6mm maximum height constraint and specified for operation from -40°C to +85°C temperature range.

**Pinout**



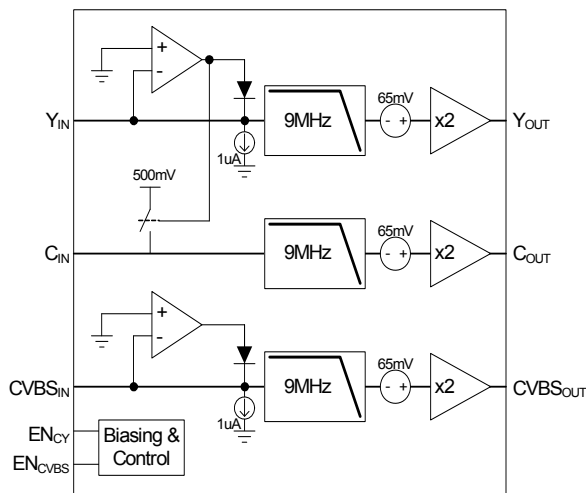
**Features**

- 3rd order 9MHz reconstruction filter
- 40V/ $\mu$ s slew rate
- Low supply current = 4.5mA
- Maximum Power-down current <0.5 $\mu$ A
- Supplies from 2.5V to 3.6V
- Rail-to-rail output
- $\mu$ TQFN package
- Pb-free plus anneal available (RoHS compliant)

**Applications**

- Video amplifiers
- Portable and handheld products
- Communications devices
- Video on demand
- Cable set-top boxes
- Satellite set-top boxes
- MP3 players
- HDTV
- Personal video recorder

**Block Diagram**



**Ordering Information**

PART NUMBER (Note)	PART MARKING	TAPE AND REEL	TEMP. RANGE (°C)	PACKAGE (Pb-Free)	PKG. DWG. #
ISL59115IRUZ-T7	FK	7"	-40 to +85	10 Ld $\mu$ TQFN	L10.2.1x1.6A

NOTE: Intersil Pb-free plus anneal products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

**Absolute Maximum Ratings** ( $T_A = +25^\circ\text{C}$ )

Supply Voltage from  $V_{DD}$  to GND ..... 4.2V  
 Input Voltage .....  $V_{DD} + 0.3\text{V}$  to GND  $-0.3\text{V}$   
 Continuous Output Current ..... 40mA  
 Power Dissipation ..... See Curves  
 Operating Junction Temperature .....  $+125^\circ\text{C}$

ESD Classification  
 Human Body Model ..... 2500V  
 Machine Model ..... 300V  
 Storage Temperature .....  $-65^\circ\text{C}$  to  $+125^\circ\text{C}$   
 Ambient Operating Temperature .....  $-40^\circ\text{C}$  to  $+85^\circ\text{C}$

*CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.*

*IMPORTANT NOTE: All parameters having Min/Max specifications are guaranteed. Typ values are for information purposes only. Unless otherwise noted, all tests are at the specified temperature and are pulsed tests, therefore:  $T_J = T_C = T_A$*

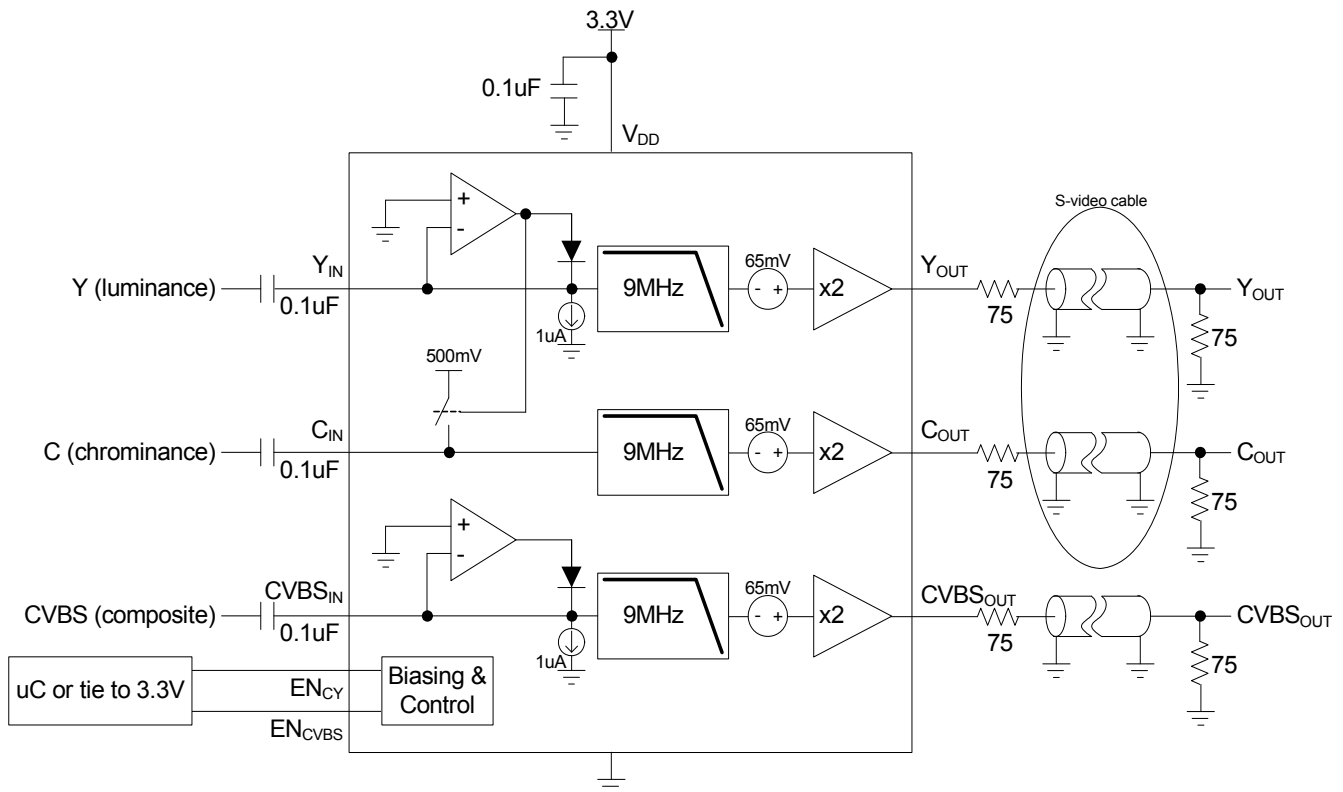
Electrical Specifications  $V_{DD} = 3.3\text{V}$ ,  $T_A = +25^\circ\text{C}$ ,  $R_L = 150\Omega$  to GND, unless otherwise specified.

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNIT
<b>INPUT CHARACTERISTICS</b>						
$V_{DD}$	Supply Voltage Range		2.5		3.6	V
$I_{DD\_CY}$	Quiescent Supply Current - CY Amps Enabled	$V_{IN} = 500\text{mV}$ , $EN_{CY} = V_{DD}$ , no load		3.1	4.0	mA
$I_{DD\_CVBS}$	Quiescent Supply Current - CVBS Amp Enabled	$V_{IN} = 500\text{mV}$ , $EN_{CVBS} = V_{DD}$ , no load		1.4	2.0	mA
$I_{DD}$	Quiescent Supply Current	$V_{IN} = 500\text{mV}$ , $EN_{CY} = EN_{CVBS} = V_{DD}$ , no load		4.5	6.0	mA
$I_{DD\_OFF}$	Shutdown Supply Current	$EN_{CY} = EN_{CVBS} = 0\text{V}$		0.1	0.5	$\mu\text{A}$
$V_{Y\_CLAMP}$	Y Input Clamp Voltage	$I_Y = -100\mu\text{A}$	-30	-15	10	mV
$I_{Y\_DOWN}$	Y Input Clamp Discharge Current	$V_Y = 0.5\text{V}$	0.6	1.1	1.6	$\mu\text{A}$
$I_{Y\_UP}$	Y Input Clamp Charge Current	$V_Y = -0.1\text{V}$		-3.6	-3.0	mA
$R_Y$	Y Input Resistance	$0.5\text{V} < V_Y < 1\text{V}$	10			$\text{M}\Omega$
$V_{CVBS\_CLAMP}$	CVBS Input Clamp Voltage	$I_{CVBS} = -100\mu\text{A}$	-30	-15	10	mV
$I_{CVBS\_DOWN}$	CVBS Input Clamp Discharge current	$V_{CVBS} = 0.5\text{V}$	0.6	1.1	1.6	$\mu\text{A}$
$I_{CVBS\_UP}$	CVBS Input Clamp Charge current	$V_{CVBS} = -0.1\text{V}$		-3.6	-3.0	mA
$R_{CVBS}$	CVBS Input Resistance	$0.5\text{V} < V_{CVBS} < 1\text{V}$	10			$\text{M}\Omega$
$V_{C\_CLAMP}$	C Input Clamp Voltage	$V_Y = 0.05\text{V}$ , $I_C = 0\text{A}$	500	550	700	mV
$R_C$	C Input Resistance	$V_Y = 0.05\text{V}$ , $0.25\text{V} \leq V_C \leq 0.75\text{V}$	2.0	2.5	3.0	$\text{k}\Omega$
$I_C$	C Input Bias Current	$V_Y = 0.3\text{V}$	-200	-2	200	nA
$V_{Y\_SYNC}$	Y Input Sync Detect Voltage		100	150	200	mV
$V_{OLS}$	Output Level Shift Voltage	$V_{IN} = 0\text{V}$ , no load	60	130	200	mV
$A_V$	Voltage Gain	$R_L = 150\Omega$	1.95	1.99	2.04	V/V
$\Delta A_{V\_CY}$	C-Y Channel Gain Mismatch		-1.75	$\pm 0.5$	1.75	%
$\Delta A_{V\_CVBS}$	C/Y-CVBS Channel Gain Mismatch		-2	$\pm 0.5$	2	%
PSRR	DC Power Supply Rejection	$V_{DD} = 2.5\text{V}$ to $3.6\text{V}$	40	60		dB
$V_{OH}$	Output Voltage High Swing	$V_{IN} = 2\text{V}$ , $R_L = 150\Omega$ to GND	2.85	3.2		V
$I_{SC}$	Output Short-Circuit Current	$V_{IN} = 2\text{V}$ , to GND through $10\Omega$	100	145		mA
$I_{ENABLE}$	$EN_{CY}$ , $EN_{CVBS}$ Input Current	$0\text{V} < V_{EN} < 3.3\text{V}$	-0.2	0.001	+0.2	$\mu\text{A}$
$V_{IL}$	Disable Threshold				0.8	V
$V_{IH}$	Enable Threshold		2.0			V
$R_{OUT}$	Shutdown Output Impedance	$EN = 0\text{V}$ , DC	5.0		7.5	$\text{k}\Omega$
		$EN = 0\text{V}$ , $f = 4.5\text{MHz}$		3.4		$\text{k}\Omega$

Electrical Specifications  $V_{DD} = 3.3V$ ,  $T_A = +25^\circ C$ ,  $R_L = 150\Omega$  to GND, unless otherwise specified. (Continued)

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNIT
<b>AC PERFORMANCE</b>						
BW <sub>0.1dB</sub>	±0.1dB Bandwidth	R <sub>SOURCE</sub> = 75Ω, R <sub>L</sub> = 150Ω, C <sub>L</sub> = 5pF		5.6		MHz
		R <sub>SOURCE</sub> = 500Ω, R <sub>L</sub> = 150Ω, C <sub>L</sub> = 5pF		3.9		MHz
BW <sub>3dB</sub>	-3dB Bandwidth	R <sub>SOURCE</sub> = 75Ω, R <sub>L</sub> = 150Ω, C <sub>L</sub> = 5pF		8.8		MHz
		R <sub>SOURCE</sub> = 500Ω, R <sub>L</sub> = 150Ω, C <sub>L</sub> = 5pF		7.8		MHz
	Normalized Stopband Gain	f = 27MHz, R <sub>SOURCE</sub> = 75Ω		-28.5		dB
		f = 27MHz, R <sub>SOURCE</sub> = 500Ω		-30.6		dB
dG	Differential Gain	NTSC and PAL		0.10		%
dP	Differential Phase	NTSC and PAL		0.5		°
D/DT	Group Delay Variation	f = 100kHz, 5MHz		5.4		ns
SNR	Signal to Noise Ratio	100% white signal		65		dB
T <sub>ON</sub>	Enable Time	V <sub>IN</sub> = 500mV, V <sub>OUT</sub> to 1%		200		ns
T <sub>OFF</sub>	Disable Time	V <sub>IN</sub> = 500mV, V <sub>OUT</sub> to 1%		14		ns
+SR	Positive Slew Rate	20% to 80%, V <sub>IN</sub> = 1V step	30	40	50	V/μs
-SR	Negative Slew Rate	80% to 20%, V <sub>IN</sub> = 1V step	-30	-40	-50	V/μs
t <sub>F</sub>	Fall Time	2.5V <sub>STEP</sub> 80% - 20%		25		ns
t <sub>R</sub>	Rise Time	2.5V <sub>STEP</sub> 20% - 80%		22		ns

**Connection Diagram**



**Pin Descriptions**

PIN NUMBER	PIN NAME	DESCRIPTION
1	Y <sub>IN</sub>	Luminance input
2	CVBS <sub>IN</sub>	Composite video input
3	C <sub>IN</sub>	Chrominance input
4	EN <sub>CY</sub>	Enable chrominance and luminance outputs
5	V <sub>DD</sub>	Positive power supply
6	EN <sub>CVBS</sub>	Enable composite video output
7	C <sub>OUT</sub>	Chrominance output
8	CVBS <sub>OUT</sub>	Composite video output
9	Y <sub>OUT</sub>	Luminance output
10	GND	Ground

**Typical Performance Curves**

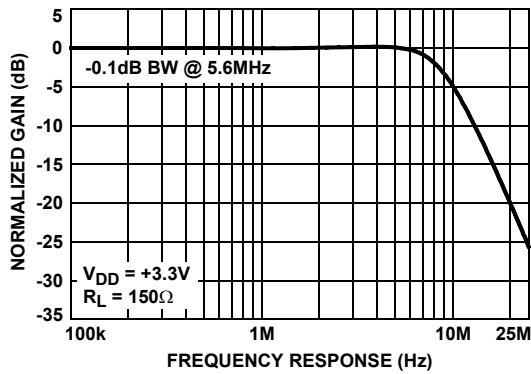


FIGURE 1. GAIN vs FREQUENCY -0.1dB

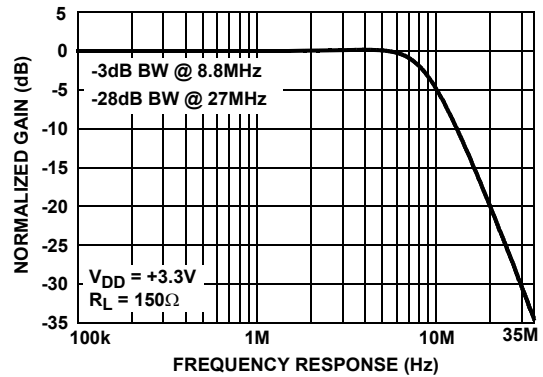


FIGURE 2. GAIN vs FREQUENCY -3dB POINT

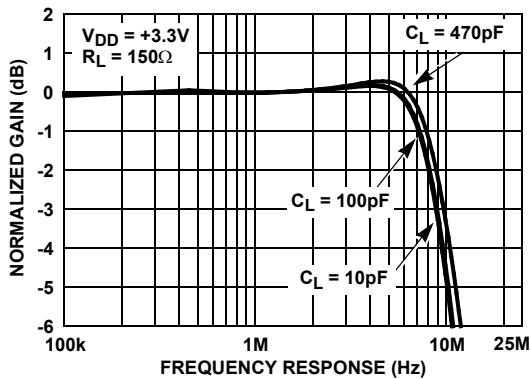


FIGURE 3. GAIN vs FREQUENCY FOR VARIOUS C<sub>LOAD</sub>

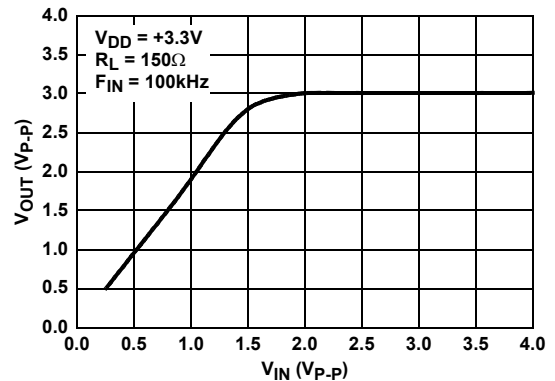


FIGURE 4. MAXIMUM OUTPUT MAGNITUDE vs INPUT MAGNITUDE

Typical Performance Curves (Continued)

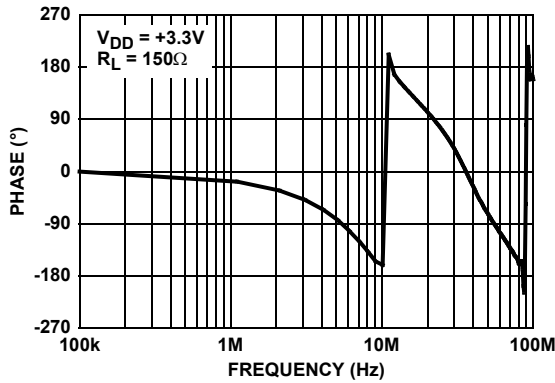


FIGURE 5. PHASE vs FREQUENCY

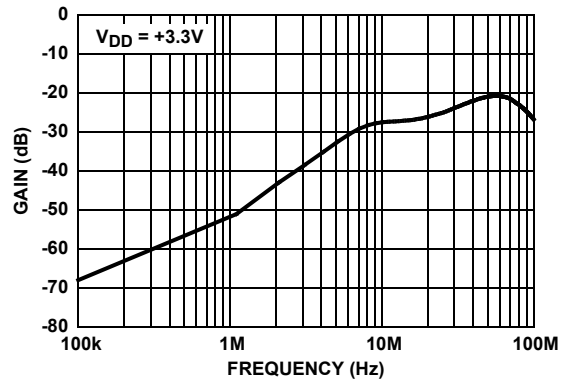


FIGURE 6. PSRR vs FREQUENCY

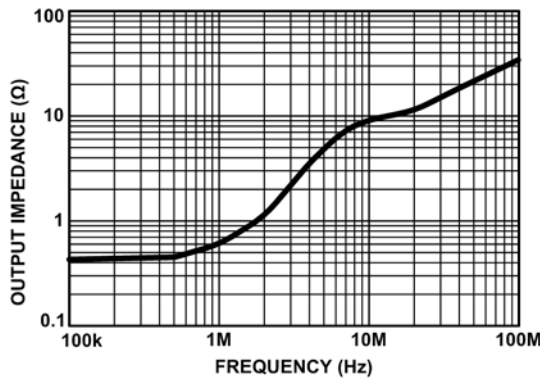


FIGURE 7. OUTPUT IMPEDANCE vs FREQUENCY

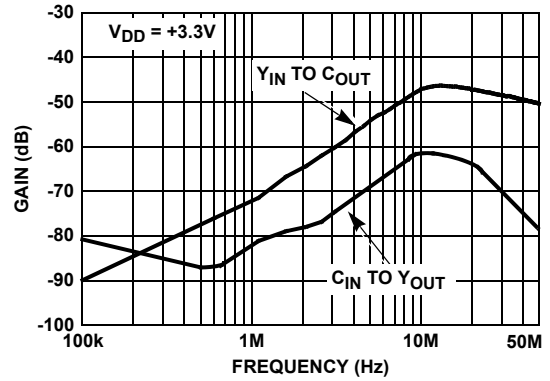


FIGURE 8. ISOLATION vs FREQUENCY

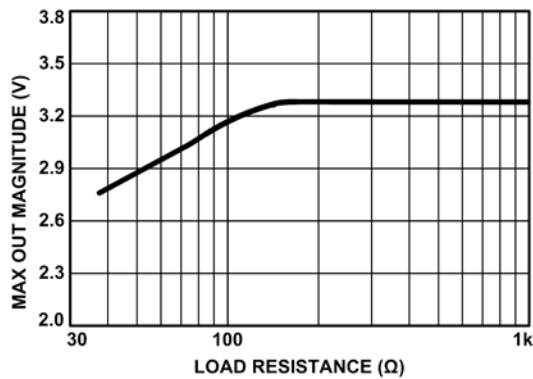


FIGURE 9. MAXIMUM OUTPUT vs LOAD RESISTANCE

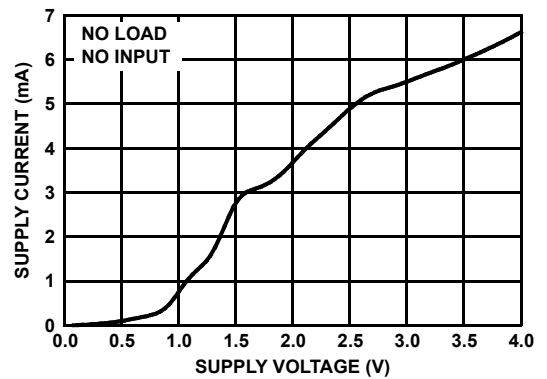


FIGURE 10. SUPPLY CURRENT vs SUPPLY VOLTAGE

Typical Performance Curves (Continued)

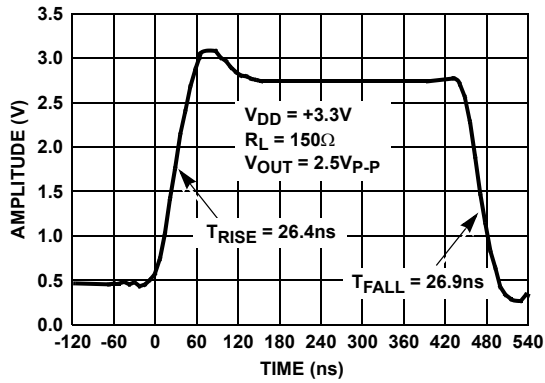


FIGURE 11. LARGE SIGNAL STEP RESPONSE

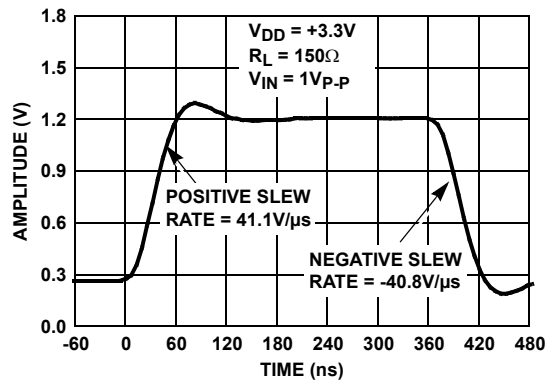


FIGURE 12. SLEW RATE

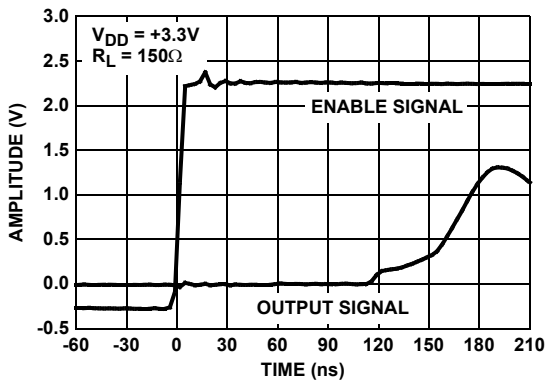


FIGURE 13. ENABLE TIME

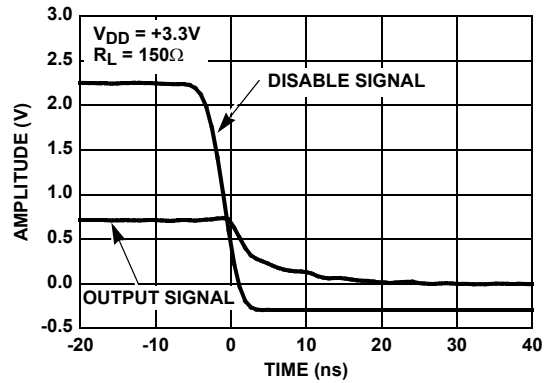


FIGURE 14. DISABLE TIME

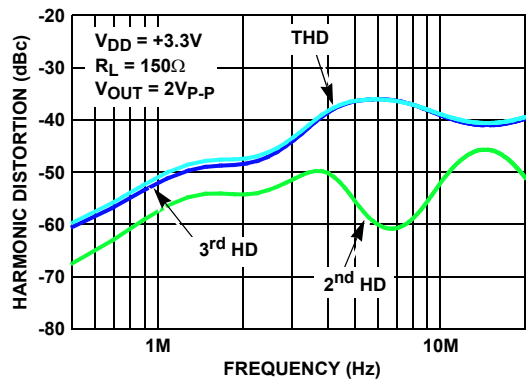


FIGURE 15. HARMONIC DISTORTION vs FREQUENCY

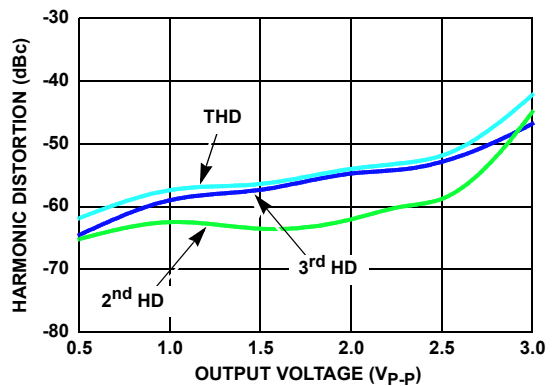


FIGURE 16. HARMONIC DISTORTION vs OUTPUT VOLTAGE

Typical Performance Curves (Continued)

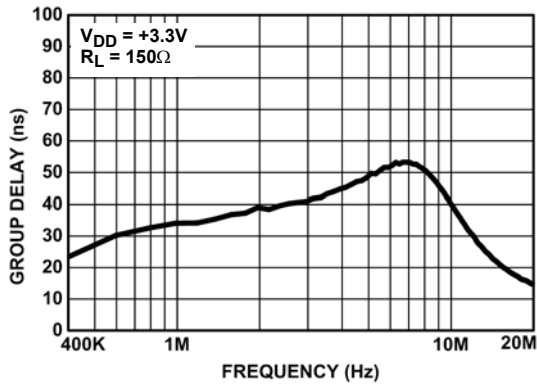


FIGURE 17. GROUP DELAY vs FREQUENCY

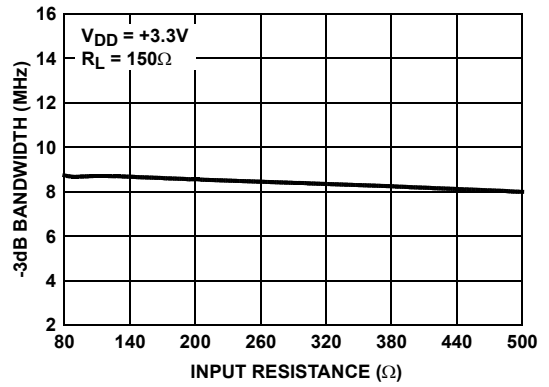


FIGURE 18. -3dB BANDWIDTH vs INPUT RESISTANCE

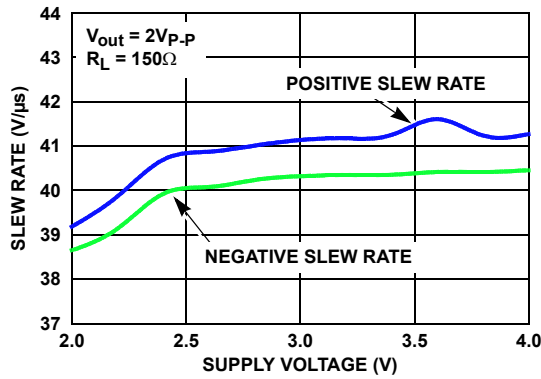


FIGURE 19. SLEW RATE vs SUPPLY VOLTAGE

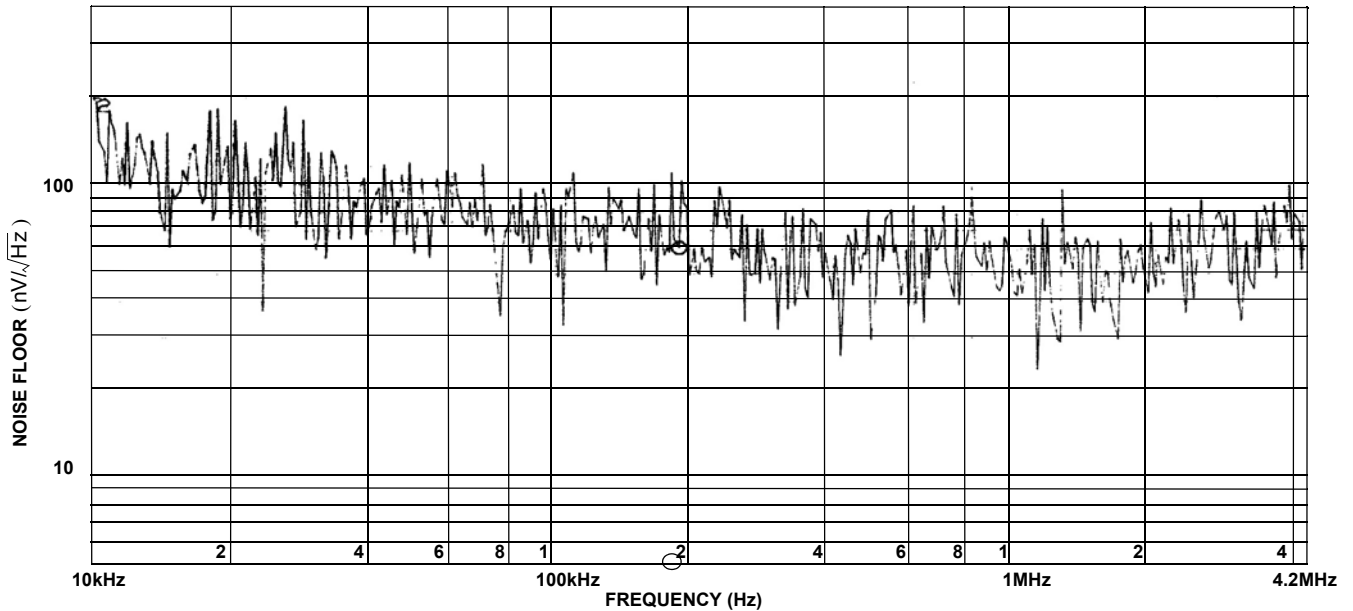


FIGURE 20. UNWEIGHTED NOISE FLOOR

## Typical Performance Curves (Continued)

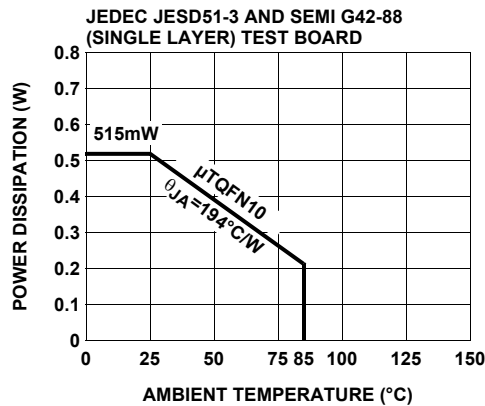


FIGURE 21. PACKAGE POWER DISSIPATION vs AMBIENT TEMPERATURE

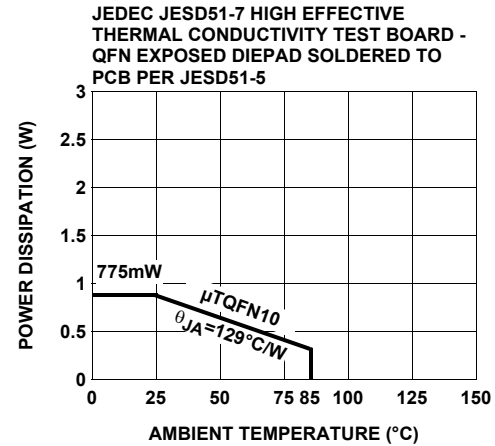


FIGURE 22. PACKAGE POWER DISSIPATION vs AMBIENT TEMPERATURE

### Application Information

The ISL59115 is a single-supply rail-to-rail triple (one s-video channel and one composite channel) video amplifier with internal sync tip clamps, a typical -3dB bandwidth of 9MHz and slew rate of about 40V/μs. This part is ideally suited for applications requiring high composite and s-video performance with very low power consumption. As the performance characteristics and features illustrate, the ISL59115 is optimized for portable video applications.

#### Internal Sync Clamp

Embedded video DACs typically use ground as their most negative supply. This places the sync tip voltage at a minimum of 0V. Presenting a 0V input to most single supply amplifiers will saturate the output stage of the amplifier resulting in a clipped sync tip and degraded video image.

The ISL59115 features an internal sync clamp and offset function that level shifts the entire video signal to the optimum level before it reaches the amplifiers' input stage. These features also help avoid saturation of the output stage of the amplifier by setting the signal closer to the best voltage range.

The simplified block diagram on the front page shows the basic operation of the ISL59115's sync clamp. The Y and CVBS inputs' AC-coupled video sync signal is pulled negative by a current source at the input. When the sync tip goes below the comparator threshold, the comparator output goes high, pulling up on the input through the diode, forcing current into the coupling capacitor until the voltage at the input is again 0V, and the comparator turns off. This forces the sync tip clamp to always be 0V, setting the offset for the entire video signal. The C channel is slaved to the Y channel and clamped to a 500mV level.

### The Sallen Key Low Pass Filter

The Sallen Key is a classic low pass configuration. This provides a very stable low pass function, and in the case of the ISL59115, a three-pole roll-off at 9MHz. The three-pole function is accomplished with an RC low pass network placed in series with and before the Sallen Key. One pole provided by the RC network and poles two and three provided by the Sallen Key for a nice three-pole roll-off at 9MHz.

#### Output Coupling

The ISL59115 can be AC or DC coupled to its output. When AC coupling, a 220μF coupling capacitor is recommended to ensure that low frequencies are passed, preventing video "tilt" or "droop" across a line.

The ISL59115's internal sync clamp makes it possible to DC couple the output to a video load, eliminating the need for any AC coupling capacitors, saving board space, cost, and eliminating any "tilt" or offset shift in the output signal. The trade off is larger supply current draw, since the DC component of the signal is now dissipated in the load resistor. Typical load current for AC coupled signals is 5mA compared to 10mA for DC coupling.

#### Output Drive Capability

The ISL59115 does not have internal short circuit protection circuitry. If the output is shorted indefinitely, the power dissipation could easily overheat the die or the current could eventually compromise metal integrity. Maximum reliability is maintained if the output current never exceeds ±40mA. This limit is set by the design of the internal metal interconnect. Note that for transient short circuits, the part is robust.

Short circuit protection can be provided externally with a back match resistor in series with the output placed close as possible to the output pin. In video applications this would be a 75Ω resistor and will provide adequate short circuit protection to the device. Care should still be taken not to stress the device with a short at the output.



### Power Dissipation

With the high output drive capability of the ISL59115, it is possible to exceed the +125°C absolute maximum junction temperature under certain load current conditions. Therefore, it is important to calculate the maximum junction temperature for an application to determine if load conditions or package types need to be modified to assure operation of the amplifier in a safe operating area.

The maximum power dissipation allowed in a package is determined according to:

$$PD_{MAX} = \frac{T_{JMAX} - T_{AMAX}}{\Theta_{JA}}$$

Where:

$T_{JMAX}$  = Maximum junction temperature

$T_{AMAX}$  = Maximum ambient temperature

$\Theta_{JA}$  = Thermal resistance of the package

The maximum power dissipation actually produced by an IC is the total quiescent supply current times the total power supply voltage, plus the power in the IC due to the load, or:

for sourcing:

$$PD_{MAX} = V_S \times I_{SMAX} + (V_S - V_{OUT}) \times \frac{V_{OUT}}{R_L}$$

for sinking:

$$PD_{MAX} = V_S \times I_{SMAX} + (V_{OUT} - V_S) \times I_{LOAD}$$

Where:

$V_S$  = Supply voltage

$I_{SMAX}$  = Maximum quiescent supply current

$V_{OUT}$  = Maximum output voltage of the application

$R_{LOAD}$  = Load resistance tied to ground

$I_{LOAD}$  = Load current

### Power Supply Bypassing Printed Circuit Board Layout

As with any modern operational amplifier, a good printed circuit board layout is necessary for optimum performance. Lead lengths should be as short as possible. The power supply pin must be well bypassed to reduce the risk of oscillation. For normal single supply operation, a single 4.7µF tantalum capacitor in parallel with a 0.1µF ceramic capacitor from  $V_S+$  to GND will suffice.

### Printed Circuit Board Layout

For good AC performance, parasitic capacitance should be kept to minimum. Use of wire wound resistors should be avoided because of their additional series inductance. Use of sockets should also be avoided if possible. Sockets add parasitic inductance and capacitance that can result in compromised performance.

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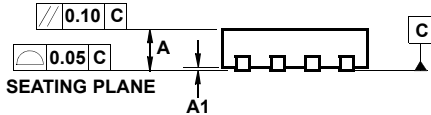
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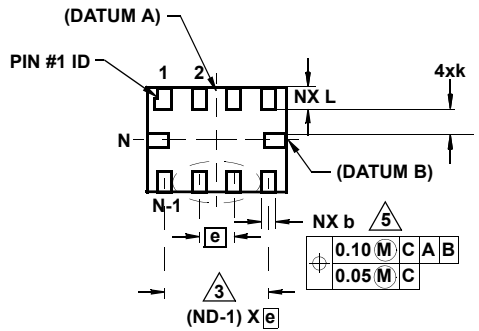
**Ultra Thin Quad Flat No-Lead Plastic Package (UTQFN)**



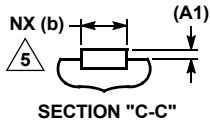
TOP VIEW



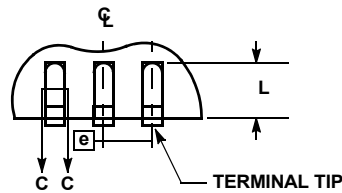
SIDE VIEW



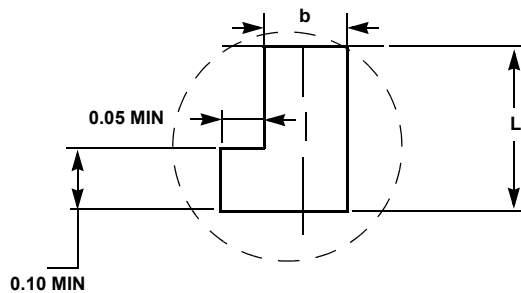
BOTTOM VIEW



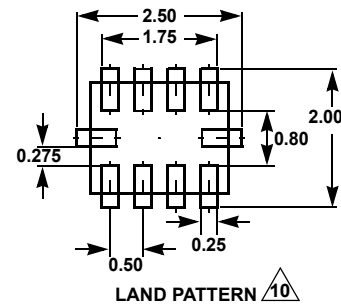
SECTION "C-C"



FOR ODD TERMINAL/SIDE



DETAIL "A" PIN 1 ID



LAND PATTERN  $\triangle 10$

**L10.2.1x1.6A**

**10 LEAD ULTRA THIN QUAD FLAT NO-LEAD PLASTIC PACKAGE**

SYMBOL	MILLIMETERS			NOTES
	MIN	NOMINAL	MAX	
A	0.45	0.50	0.55	-
A1	-	-	0.05	-
A3	0.127 REF			-
b	0.15	0.20	0.25	5
D	2.05	2.10	2.15	-
E	1.55	1.60	1.65	-
e	0.50 BSC			-
k	0.20	-	-	-
L	0.35	0.40	0.45	-
N	10			2
Nd	4			3
Ne	1			3
$\theta$	0	-	12	4

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NOTES:

1. Dimensioning and tolerancing conform to ASME Y14.5-1994.
2. N is the number of terminals.
3. Nd and Ne refer to the number of terminals on D and E side, respectively.
4. All dimensions are in millimeters. Angles are in degrees.
5. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.
7. Maximum package warpage is 0.05mm.
8. Maximum allowable burrs is 0.076mm in all directions.
9. Same as JEDEC MO-255UABD except:  
No lead-pull-back, "A" MIN dimension = 0.45 not 0.50mm  
"L" MAX dimension = 0.45 not 0.42mm.
10. For additional information, to assist with the PCB Land Pattern Design effort, see Intersil Technical Brief TB389.