# ISL15102

Single Port, PLC Differential Line Driver

The ISL15102 is a single port differential line driver developed for Power Line Communication (PLC) applications. The device is designed to drive heavy line loads while maintaining a high level of linearity required in Orthogonal Frequency Division Multiplexing (OFDM) PLC modem links.

The ISL15102 has a disable control pin (DIS). In Disable mode, the line driver goes into Low Power mode and the outputs maintain a high impedance in the presence of high receive signal amplitude, improving TDM receive signal integrity.

The ISL15102 has built-in thermal protection. When the internal temperature reaches +150°C (typical) the driver shuts down to prevent damage to the device.

An internal input CM buffer maximizes the dynamic range and reduces the number of external components in the application circuit.

The ISL15102 is supplied in a thermally-enhanced small footprint (4mm x 5mm) 24 Ld QFN package. The ISL15102 is specified for operation across the -40°C to +105°C operating ambient temperature range.

## Features

- Single differential driver
- Internal $V_{CM}$
- 90MHz signal bandwidth
- 900V/µs slew rate
- Single +8V to +28V supply, absolute maximum 30V
- Supports narrowband and broadband DMT PLC
- -86dB THD at 200kHz in to 50Ω line load
- -70dB THD at 3MHz in to 50Ω line load
- Control pin for enable/disable for TDM operation
- Thermal shutdown

## Applications

- Power line communication differential driver

**Table 1. Alternate Solutions**

| Part # | Nominal ±$V_S$ (V) | Bandwidth (MHz) | Applications |
|---|---|---|---|
| ISL15100 | ±6, +12 | 180 | Broadband PLC |
| ISL1571 | ±6, +12 | 250 | Broadband PLC |

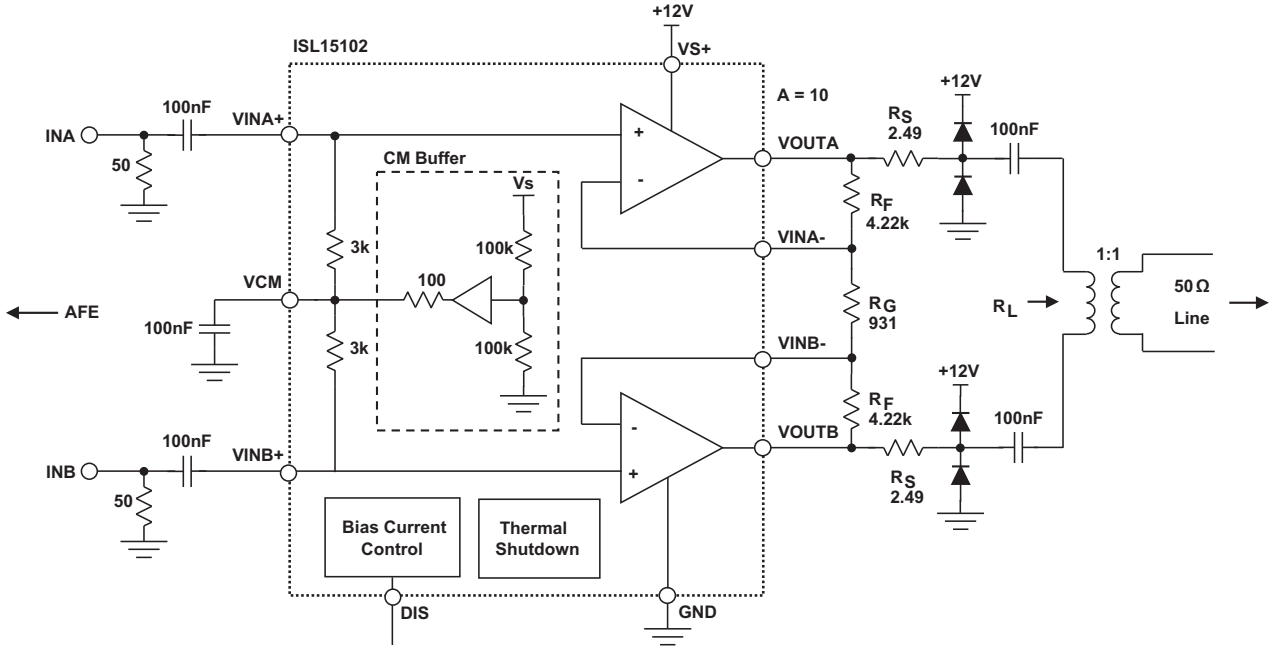



**Figure 1. Typical Application Circuit**

# 1. Overview

## 1.1 Ordering Information

| Part Number (Notes 2, 3) | Part Marking | Operating Ambient Temp Range (°C) | Tape and Reel (Units) (Note 1) | Package (RoHS Compliant) | Pkg. Dwg. # |
|---|---|---|---|---|---|
| ISL15102IRZ | 15102IRZ | -40 to +105 | - | 24 Ld QFN | L24.4x5F |
| ISL15102IRZ-T13 | 15102IRZ | -40 to +105 | 2.5k | 24 Ld QFN | L24.4x5F |
| ISL15102IRZ-EVALZ | Evaluation Board | | | | |

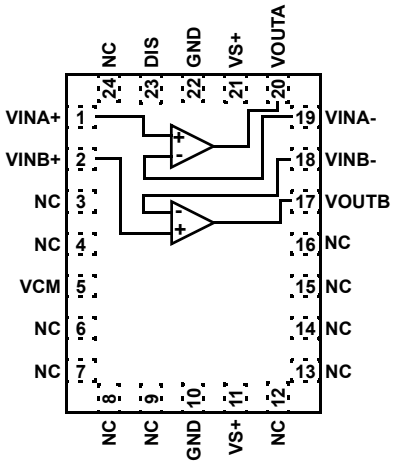
**Notes:**

1. See TB347 for details about reel specifications.
2. These Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J-STD-020.
3. For Moisture Sensitivity Level (MSL), see the ISL15102 device page. For more information about MSL, see TB363.

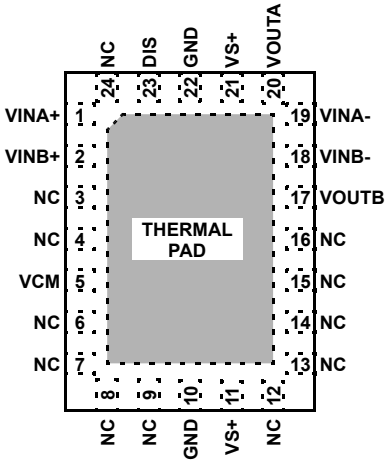
## 1.2 Pin Configuration

ISL15102
(24 Ld QFN)

Internal View

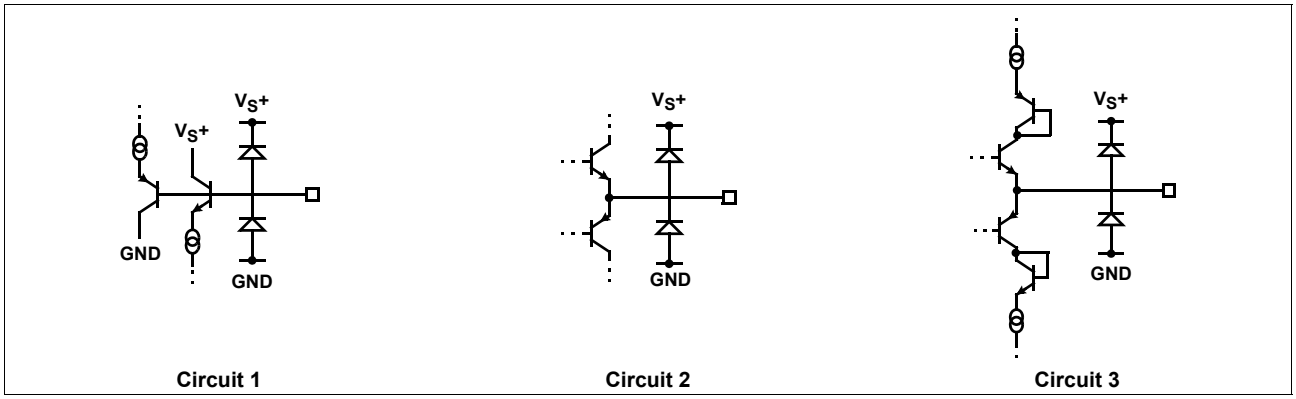



Top View



## 1.3 Pin Descriptions

| Pin Number | Pin Name | Function | Circuit |
|---|---|---|---|
| 1 | VINA+ | Amplifier A non-inverting input | See Circuit 1 |
| 2 | VINB+ | Amplifier B non-inverting input | See Circuit 1 |
| 3, 4, 6, 7, 8, 9, 12, 13, 14, 15, 16, 24 | NC | No internal connection | |
| 10, 22 | GND | Ground connection | |
| 5 | VCM | Output common-mode bias | |
| 11, 21 | VS+ | Positive supply voltage | |
| 17 | VOUTB | Amplifier B output | See Circuit 2 |
| 18 | VINB- | Amplifier B inverting input | See Circuit 3 |
| 19 | VINA- | Amplifier A inverting input | See Circuit 3 |
| 20 | VOUTA | Amplifier A output | See Circuit 2 |
| 23 | DIS | Disable control pin | |
| - | Thermal Pad | Connects to GND | |




Circuit 1 Circuit 2 Circuit 3

# 2. Specifications

## 2.1 Absolute Maximum Ratings

$T_A$ = +25°C

| Parameter | Minimum | Maximum | Unit |
|---|---|---|---|
| $V_S$+ Voltage to GND | -0.3 | 30 | V |
| Driver $V_{IN}$+ Voltage | GND | $V_S$+ | V |
| DIS Voltage to GND | -0.3 | 6 | V |
| $V_{CM}$ Voltage to GND | GND | $V_S$+ | |
| **ESD Rating** | **Value** | | **Unit** |
| Human Body Model (Tested per JS-001-2014) | 2 | | kV |
| Charged Device Model (Tested per JS-002-2014) | 750 | | V |

**CAUTION:** Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions can adversely impact product reliability and result in failures not covered by warranty.

## 2.2 Thermal Information

| Thermal Resistance (Typical) | $\theta_{JA}$ (°C/W) | $\theta_{JC}$ (°C/W) |
|---|---|---|
| 24 Ld QFN Package (Notes 4, 5) | 38 | 4 |

**Notes:**

4. $\theta_{JA}$ is measured in free air with the component mounted on a high-effective thermal conductivity test board with direct attach features. See TB379.
5. For $\theta_{JC}$, the case temperature location is the center of the exposed metal pad on the package underside.

| Parameter | Minimum | Maximum | Unit |
|---|---|---|---|
| Storage Temperature Range | -65 | +150 | °C |
| Power Dissipation | See Figure 14 | | |
| Pb-Free Reflow Profile | See TB493 | | |

## 2.3 Recommended Operation Conditions

| Parameter | Minimum | Maximum | Unit |
|---|---|---|---|
| Temperature Range | -40 | +105 | °C |
| Junction Temperature | -40 | +150 | °C |

## 2.4 Electrical Specifications

Unless otherwise noted, all tests are at the specified temperature $T_A$ = +25°C, $V_S$+ = +12V, $A_V$ = 10V/V, $R_F$ = 4.22kΩ, $R_L$ = 50Ω differential, DIS = 0V.

| Parameter | | Symbol | Test Conditions | Min (Note 6) | Typ (Note 7) | Max (Note 6) | Unit |
|---|---|---|---|---|---|---|---|
| **AC Performance** | | | | | | | |
| -3dB Small Signal Bandwidth | | BW | $V_O < 2V_{P-P-DIFF}$ | | 90 | | MHz |
| -3dB Large Signal Bandwidth | | | $V_O = 10V_{P-P-DIFF}$ | | 60 | | MHz |
| 20% to 80% | | SR | $V_O = 10V_{P-P-DIFF}$ | | 900 | | V/µs |
| 200kHz Harmonic Distortion | 2nd Harmonic | | $V_{OUT} = 2V_{P-P-DIFF}$ | | -88 | | dBc |
| | 3rd Harmonic | | $V_{OUT} = 2V_{P-P-DIFF}$ | | -92 | | dBc |
| | THD | | $V_{OUT} = 2V_{P-P-DIFF}$ | | -86 | | dBc |
| 3MHz Harmonic Distortion | 2nd Harmonic | | $V_{OUT} = 2V_{P-P-DIFF}$ | | -83 | | dBc |
| | 3rd Harmonic | | $V_{OUT} = 2V_{P-P-DIFF}$ | | -70 | | dBc |
| | THD | | $V_{OUT} = 2V_{P-P-DIFF}$ | | -70 | | dBc |
| 6MHz Harmonic Distortion | 2nd Harmonic | | $V_{OUT} = 2V_{P-P-DIFF}$ | | -76 | | dBc |
| | 3rd Harmonic | | $V_{OUT} = 2V_{P-P-DIFF}$ | | -66 | | dBc |
| | THD | | $V_{OUT} = 2V_{P-P-DIFF}$ | | -65 | | dBc |
| Non-Inverting Input Voltage Noise at each of the Two Inputs | | $e_N$ | f = 1MHz | | 8.5 | | nV/√Hz |
| Non-Inverting Input Current Noise at each of the Two Inputs | | $+i_N$ | f = 1MHz | | 1.5 | | pA/√Hz |
| Inverting Input Current Noise at each of the Two Inputs | | $-i_N$ | f = 1MHz | | 38 | | pA/√Hz |
| Common-Mode Output Noise | | $e_{N-CM}$ | f = 1MHz | | 128 | | nV/√Hz |
| **Power Control Features** | | | | | | | |
| Logic High Voltage | | $V_{IH}$ | DIS input | 2.0 | | | V |
| Logic Low Voltage | | $V_{IL}$ | DIS input | | | 0.8 | V |
| Logic High Current for DIS | | $I_{IH}$ | DIS = 3.3V | | 0.3 | | µA |
| Logic Low Current for DIS | | $I_{IL}$ | DIS = 0V | | -0.4 | | µA |
| **Supply Characteristics** | | | | | | | |
| Maximum Operating Supply Voltage | | | | | 28 | | V |
| Minimum Operating Supply Voltage | | | | | 8 | | V |
| GND Pin Current | | $I_{GND}$ | All outputs at 0V, DIS = 3.3V | | 0.4 | | mA |
| Positive Supply Current | | $I_S$+ (full power) | All outputs at $V_S$+/2, DIS = 0V $V_{O-Diff}$ = 0V | | 21 | | mA |
| Positive Supply Current | | $I_S$+ (power-down) | All outputs at $V_S$+/2, DIS = 3.3V, $V_{O-Diff}$ = 0V | | 0.4 | | mA |
| **Output Characteristics** | | | | | | | |
| Unloaded Output Differential Swing | | $V_{OUT}$ | $R_{L-DIFF}$ = no load | | 20 | | $V_{P-P}$ |
| **Input Characteristics** | | | | | | | |
| Input Offset Voltage - Differential Mode | | $V_{IOS-DM}$ | (VINA+ - VINB+) | -17 | -0.3 | 17 | mV |
| Input Offset Voltage - Common-Mode | | $V_{IOS-CM}$ | Delta to $V_S$+/2 | -17 | 4 | 17 | mV |

Unless otherwise noted, all tests are at the specified temperature $T_A$ = +25°C, $V_S$+ = +12V, $A_V$ = 10V/V, $R_F$ = 4.22kΩ, $R_L$ = 50Ω differential, DIS = 0V. **(Continued)**

| Parameter | Symbol | Test Conditions | Min (Note 6) | Typ (Note 7) | Max (Note 6) | Unit |
|---|---|---|---|---|---|---|
| Input $V_{OS}$ Drift | $V_{OS, DRIFT}$ | -25°C to +125°C $T_J$ | | ±2 | | µV/°C |
| Non-Inverting Input Bias Current - Differential Mode | $+I_{BDM}$ | ($+I_{BA}$ - $+I_{BB}$) | -3 | 0.2 | 3 | µA |
| Inverting Input Bias Current - Differential Mode | $-I_{BDM}$ | ($-I_{BA}$ - $-I_{BB}$) | -20 | -0.6 | 20 | µA |
| Non-Inverting $I_B$+ Drift | $I_{B+, DRIFT}$ | -25°C to +105°C $T_J$ | | ±6 | | nA/°C |
| Inverting $I_B$- Drift | $I_{B-, DRIFT}$ | -25°C to +105°C $T_J$ | | ±6 | | nA/°C |
| Power Supply Rejections to Differential Output (Input Referred) | PSRR | $V_S$+ = +8V to +28V | | 68 | | dB |
| Power Supply Rejections to Common-Mode Output (Output Referred) | | $V_S$+ = +8V to +28V | | 22 | | dB |
| Differential Input Resistance | $Z_{IN}$ | | | 6 | | kΩ |
| **Thermal Protection** | | | | | | |
| Thermal Shutdown | | | +125 | +160 | | °C |

**Notes:**

6. Compliance to datasheet limits is assured by one or more methods: production test, characterization, and/or design.
7. Typical values are for information purposes only.

# 3. Typical Performance Curves

$V_S$+ = +12V, $R_F$ = 4.22kΩ, $A_V$ = 10V/V differential, $R_L$ = 50Ω differential, $T_A$ = +25°C, DIS = 0V, unless otherwise noted.

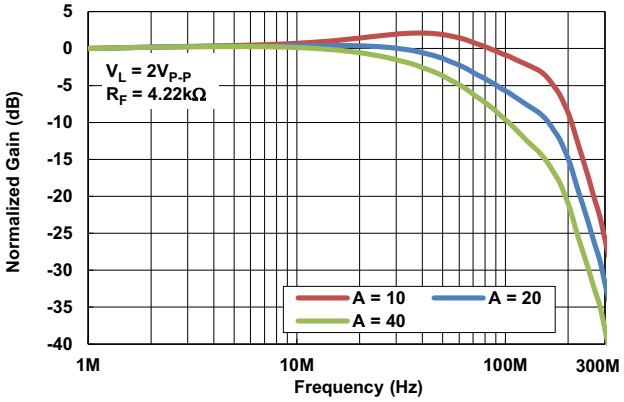



Figure 2. Small Signal Frequency Response vs Gain

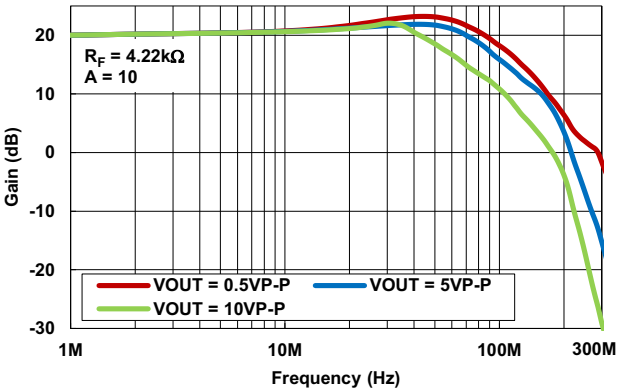



Figure 3. Large Signal Frequency Response

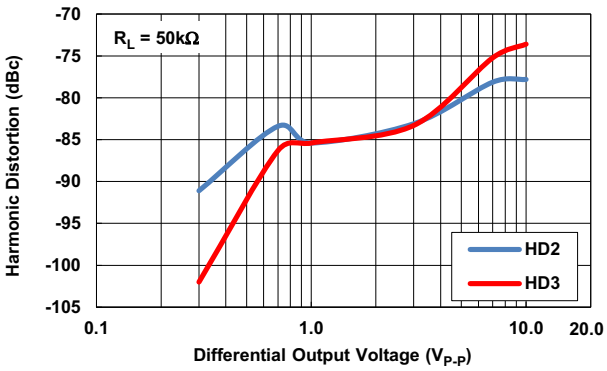



Figure 4. 1MHz Harmonic Distortion vs Output Swing

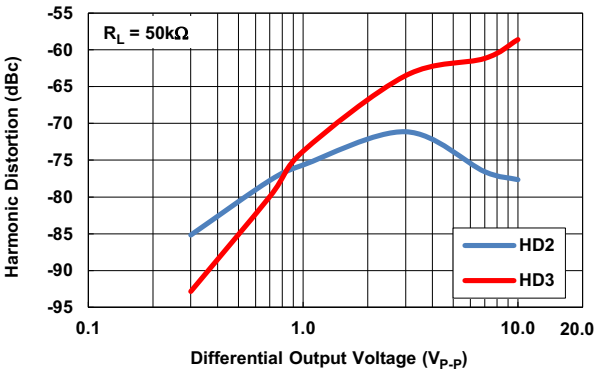



Figure 5. 4MHz Harmonic Distortion vs Output Swing

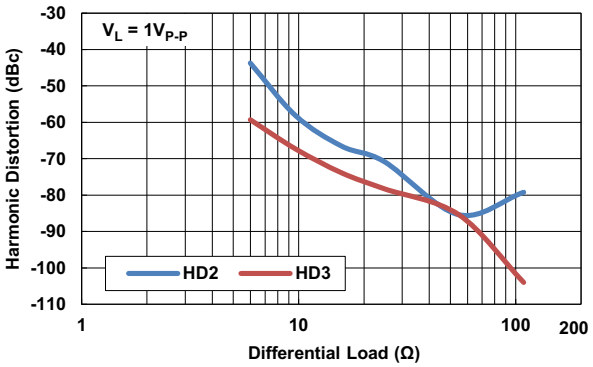



Figure 6. 1MHz Harmonic Distortion vs Load

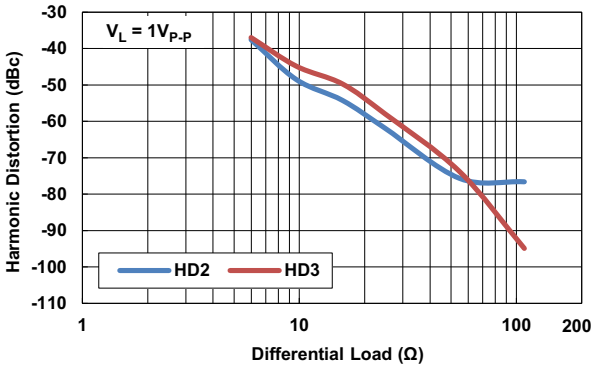



Figure 7. 4MHz Harmonic Distortion vs Load

$V_S$+ = +12V, $R_F$ = 4.22kΩ, $A_V$ = 10V/V differential, $R_L$ = 50Ω differential, $T_A$ = +25°C, DIS = 0V, unless otherwise noted. **(Continued)**

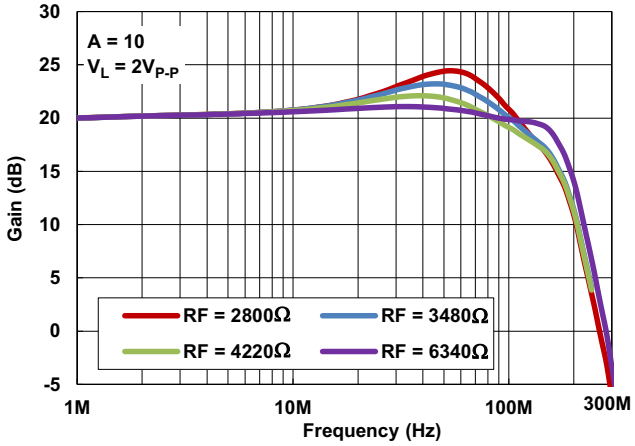



**Figure 8. Small Signal Frequency Response vs $R_F$**

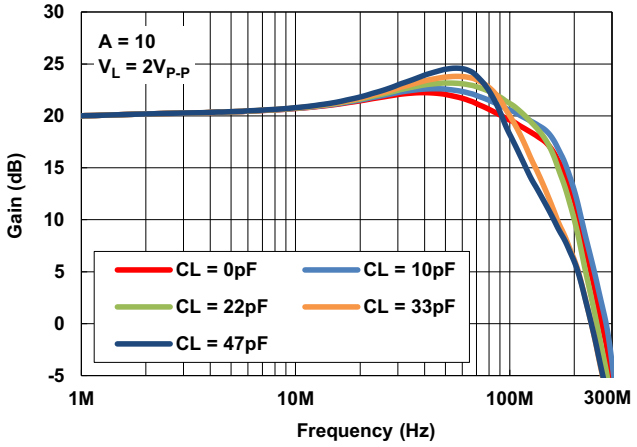



**Figure 9. Small Signal Frequency Response vs $C_{LOAD}$**

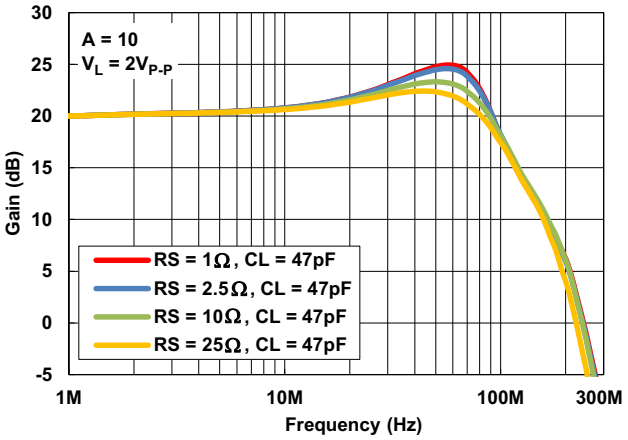



**Figure 10. Small Signal Frequency Response vs $R_S$ and $C_{LOAD}$**

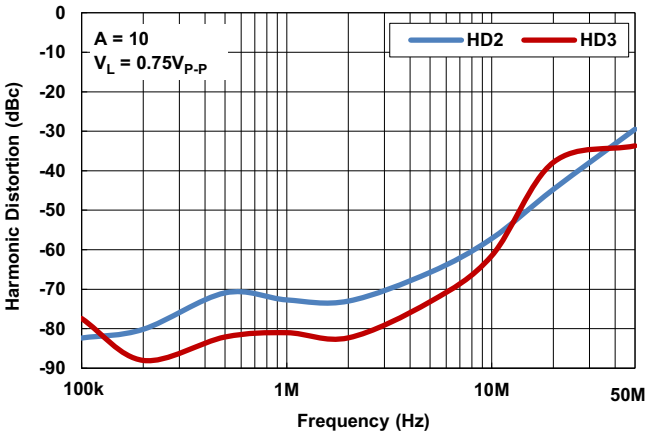



**Figure 11. Harmonic Distortion vs Frequency**

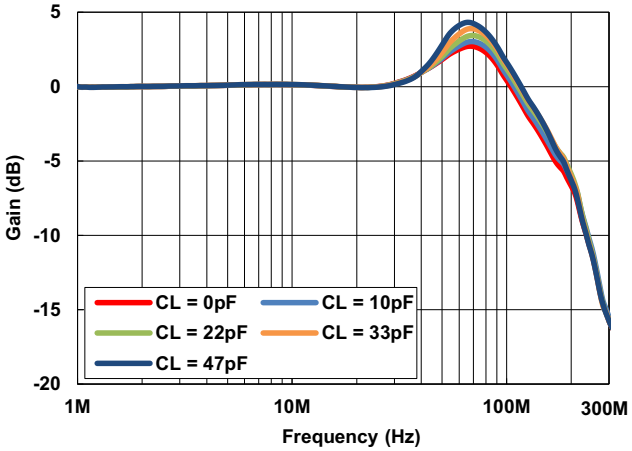



**Figure 12. Common-Mode Small Signal Frequency Response vs $C_{LOAD}$**

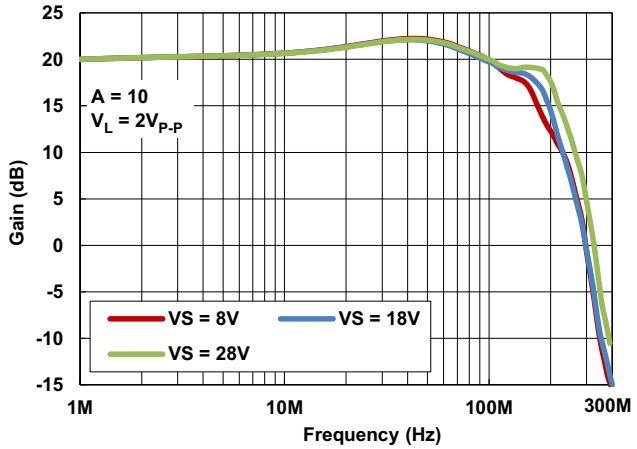



**Figure 13. Small Signal Frequency Response vs Supply Voltage**

$V_S$+ = +12V, $R_F$ = 4.22kΩ, $A_V$ = 10V/V differential, $R_L$ = 50Ω differential, $T_A$ = +25°C, DIS = 0V, unless otherwise noted. **(Continued)**

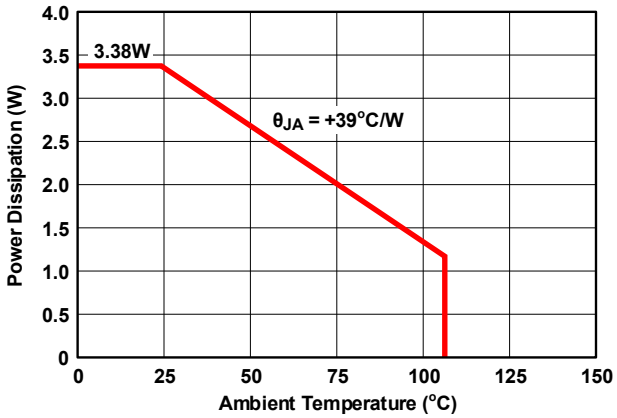



**Figure 14. Package Power Dissipation vs Ambient Temperature**

# 4. Test Circuit

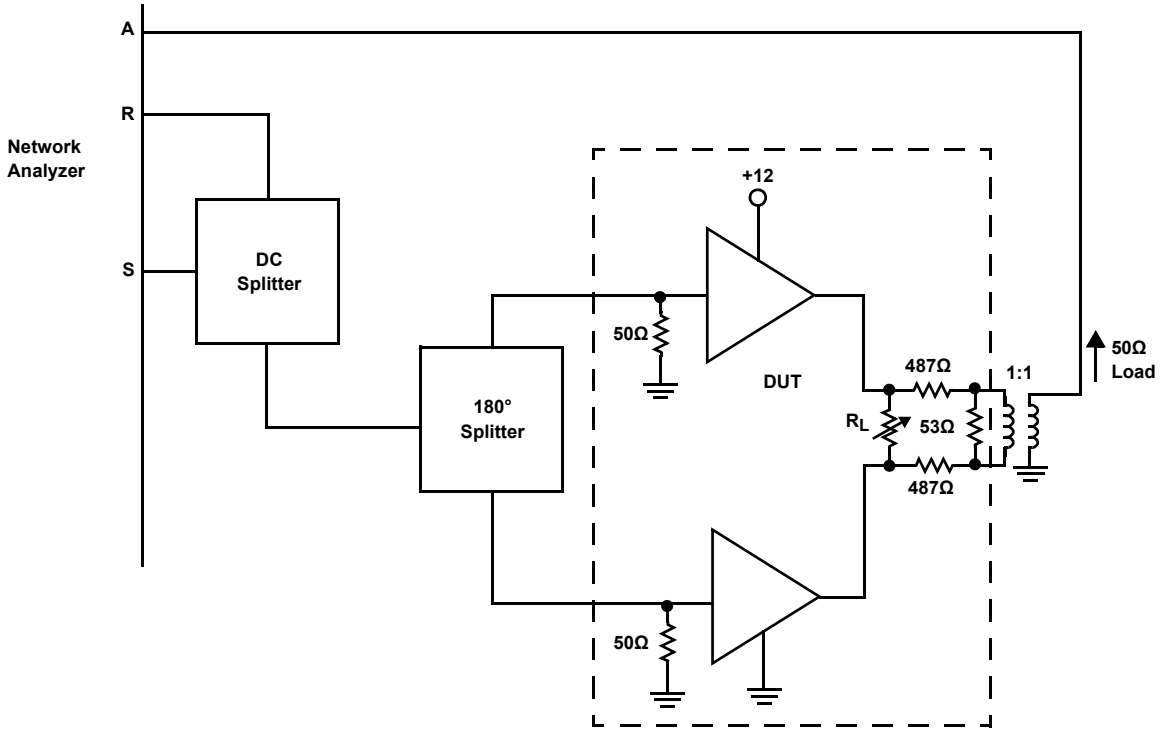



**Figure 15. Frequency Response Characterization Circuit**

# 5. Applications Information

## 5.1 Applying Wideband Current Feedback Op Amps as Differential Drivers

A Current Feedback Amplifier (CFA) such as the ISL15102 is particularly suited to the requirements of high output power, high bandwidth, and differential drivers. This topology offers a high slew rate on low quiescent power and the ability to hold AC characteristics relatively constant over a wide range of gains. The AC characteristics are principally set by the feedback resistor ($R_F$) value in simple differential gain circuits as shown in Figure 16.

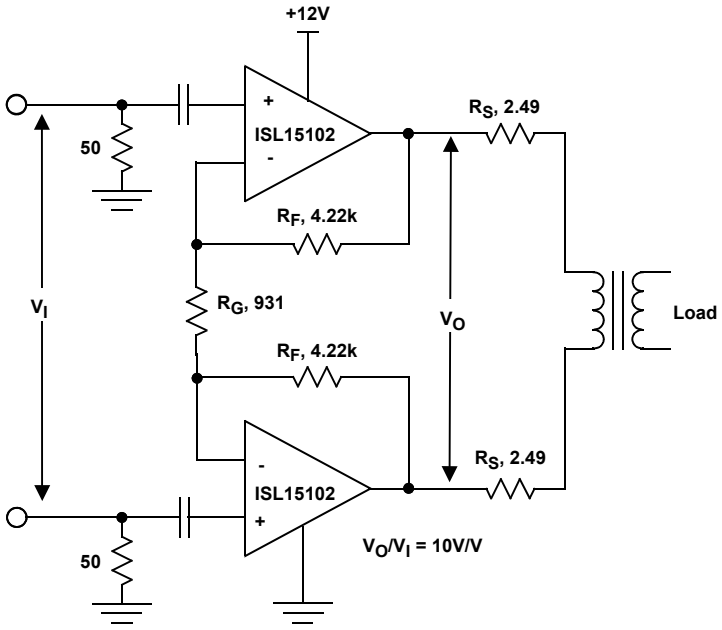



**Figure 16. Passive Termination Circuit**

In this differential gain of 10V/V circuit, the 4.22k feedback resistors ($R_F$) set the bandwidth, and the 931 gain resistor ($R_G$) controls the gain. The $V_O/V_I$ gain for this circuit is set by Equation 1:

$$\frac{V_O}{V_I} = 1 + \left(2 \cdot \frac{R_F}{R_G}\right) = 1 + \left(2 \cdot \frac{4.22k\Omega}{931\Omega}\right) = 10.06 \quad \text{(EQ. 1)}$$

The effect of increasing or decreasing the feedback resistor value is shown in Figure 8. Increasing $R_F$ will tend to roll off the response, while decreasing it will peak the frequency response up, extending the bandwidth. $R_G$ was adjusted in each of these plots to hold a constant gain of 10 (or 20dB). This shows the flexibility offered by the CFA topology; the frequency response can be controlled with the value of the feedback resistor, $R_F$, with resistor $R_G$ setting the desired gain.

The ISL15102 provides two very power efficient, high output current CFAs. These are intended to be connected as one differential driver. The Pin Configuration show that Channels A and B are intended to operate as a pair. Power-down control is provided through control pin DIS, which sets the power for Channels A and B together.

Very low output distortion at low power can be provided by the differential configuration. The high slew rate intrinsic to the CFA topology also contributes to the exceptional performance shown in Figure 11. This swept frequency distortion plot shows low distortion at 200kHz holding to very low levels up through 10MHz.

## 5.2 Input Biasing and Input Impedance

The ISL15102 has internal resistors at the non-inverting inputs for mid-rail biasing, so only external AC coupling capacitors are required for input biasing, shown in Figure 1. With a 100nF coupling capacitor and an input differential impedance of 6kΩ typical, the first order high-pass cut-off frequency is 530Hz.

## 5.3 Power Control Function

DIS controls the quiescent current for the port constructed from Amplifiers A and B. Taking DIS high (>2V), will put the device in Power-Down mode, reducing the supply current to typical 0.4mA. Taking DIS low (<0.8V), will place the drive in Full Power mode, consuming typically 22mA supply current. Table 2 summarizes the operation modes for the ISL15102.

**Table 2. Power Modes of the ISL15102**

| DIS | Operation |
|---|---|
| 0 | $I_S$ Full Power |
| 1 | Power-Down |

# 6. Performance Considerations

## 6.1 Driving Capacitive Loads

All closed-loop op amps are susceptible to reduced phase margin when driving capacitive loads. This shows up as peaking in the frequency response that can, in extreme situations, lead to oscillations. The ISL15102 is designed to operate successfully with small capacitive loads such as layout parasitics. As the parasitic capacitance increases, it is best to consider a small resistor in series with each output to isolate the phase margin effects of the capacitor. Figure 9 shows the effect of capacitive load on the differential gain-of-10 circuit. With 22pF on each output, we see about 3dB peaking. This will increase quickly at higher $C_{LOADS}$. If this degree of peaking is unacceptable, a small series resistor can be used to improve the flatness as shown in Figure 10.

## 6.2 Board Design Recommendations

The feedback resistors need to be placed as close as possible to the output and inverting input pins to minimize parasitic capacitance in the feedback loop. Keep the gain resistor also very close to the inverting inputs for its port and minimize parasitic capacitances to ground or power planes as well.

Close placement of the supply decoupling capacitors will minimize parasitic inductance in the supply path. High frequency load currents are typically pulled through these capacitors, so close placement of 0.01µF capacitors on each of the supply pins will improve dynamic performance. Higher valued capacitors, 6.8µF typically, can be placed further from the package as they are providing more of the low frequency decoupling.

Connect the thermal pad for the ISL15102 to ground. It is recommended to fill the PCB metal beneath the thermal pad with a 3x3 array of vias to spread heat away from the package. The larger the PCB metal area, the lower the junction temperature of the device will be.

Although the ISL15102 is relatively robust in driving parasitic capacitive loads, it is always preferred to place any series output resistors as close as possible to the output pins. Then trace capacitance on the other side of that resistor will have a much smaller effect on loop phase margin.

Protection devices that are intended to steer large load transients away from the ISL15102 output stage and into the power supplies or ground should have a short trace from their supply connections into the nearest supply capacitor, or they should include their own supply capacitors to provide a low impedance path under fast transient conditions.

# 7. Supply Transient Immunity

Power line modules can experience supply voltage transients of up to 40V. To estimate the transient immunity of the ISL15102 under these conditions, several units were tested beyond the specifications in the Absolute Maximum Ratings table. Figure 17 shows the device configuration used for this test and Figure 18 shows the actual test pulses applied.

In the test, a pulse generator applies 60 pulses of 42V peak voltage and 600ms pulse duration into the driver supply pins (VS) with a 10s pause interval between pulses. There was no change in the device quiescent current before and after the testing, and the device did not show any signs of physical or electrical damage or abnormality.

The primary objective of this test was to simulate the transient immunity of the PLC driver supply and does not imply performance or maximum limits beyond those specified in the Absolute Maximum Ratings.

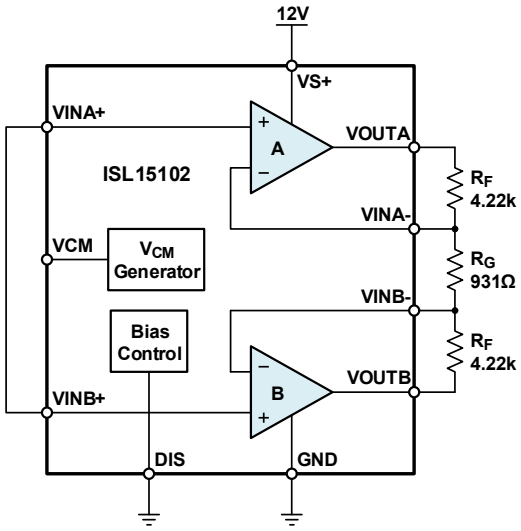



**Figure 17. Supply Transient Test Configuration**

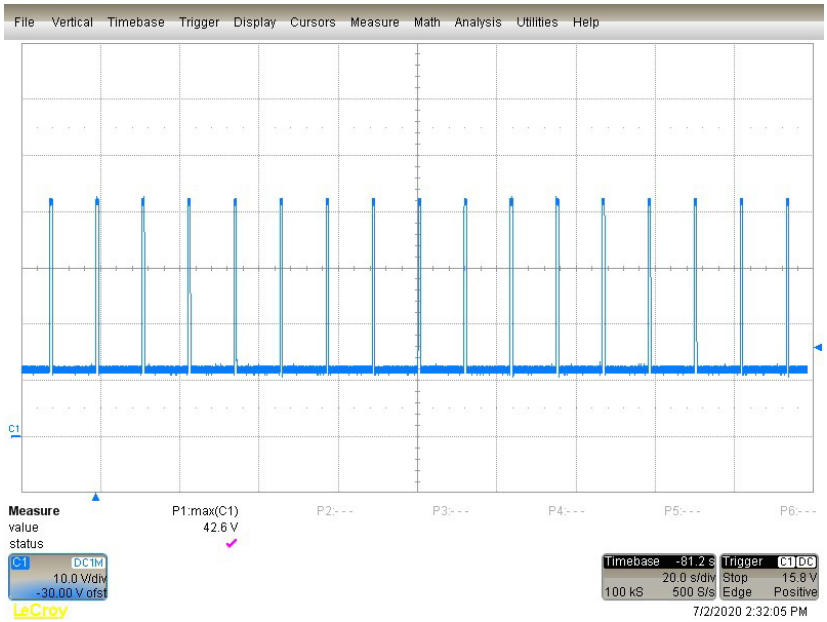



**Figure 18. Supply Transient Test Pulses**

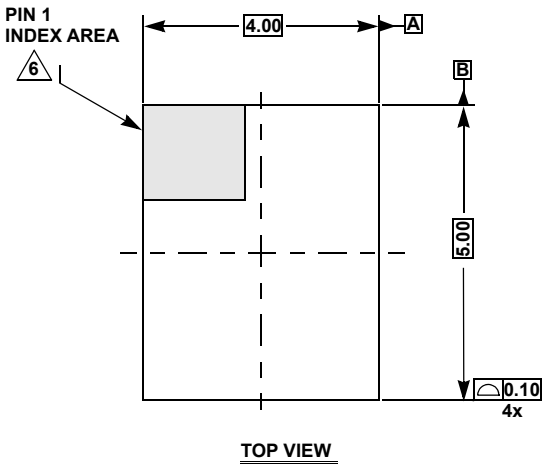
# 8. Revision History

| Rev. | Date | Description |
|---|---|---|
| 1.02 | Jun 13, 2024 | Updated operating temperature maximum from 85 to 105C throughout.<br>Removed Related Literature section.<br>Updated Figure 14. |
| 1.01 | Sep 3, 2020 | Updated links throughout.<br>Added Supply Transient Immunity section. |
| 1.00 | May 3, 2018 | Added ISL15102IRZ-EVALZ to the Ordering Information table.<br>Updated Figures 2-13 to correct formatting issues.<br>Figure 14, changed Y-axis unit of measurement from dB to W.<br>Removed About Intersil section<br>Updated the disclaimer. |
| 0.00 | Dec 1, 2017 | Initial release |

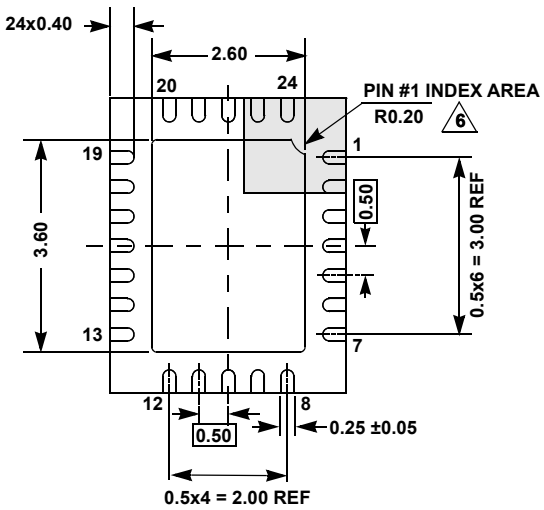
# 9. Package Outline Drawing

For the most recent package outline drawing, see L24.4x5F.

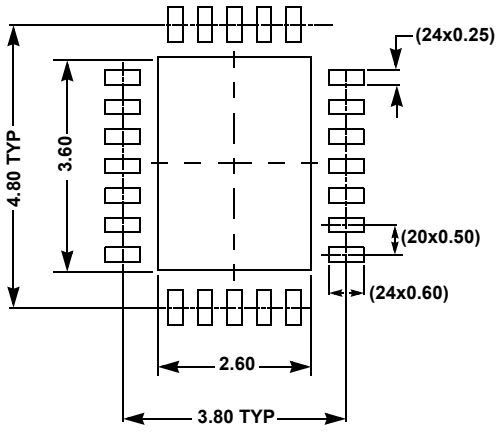
L24.4x5F
24 Lead Quad Flat No-Lead Plastic Package
Rev 0, 5/14



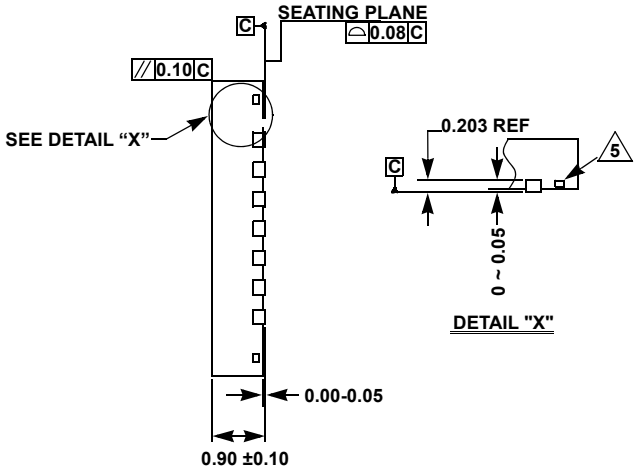

TOP VIEW




BOTTOM VIEW




TYPICAL RECOMMENDED LAND PATTERN




SIDE VIEW

**NOTES:**

1. Dimensions are in millimeters.
   Dimensions in ( ) are for Reference Only.
2. Dimensioning and tolerancing conform to ASMEY14.5m-1994.
3. Unless otherwise specified, tolerance: Decimal ± 0.05
4. Dimension applies to the metallized terminal and is measured between 0.20mm and 0.30mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.

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(Disclaimer Rev.1.01 Jan 2024)


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