IS-1825xSRH, IS-1825BSEH, ISL71823xSRH

Single Event and Total Dose Hardened, High-Speed Dual Output PWMs

FN9065
Rev.7.00
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The IS-1825ASRH, IS-1825BSRH, IS-1825BSEH, ISL71823ASRH, and ISL71823BSRH are single event and total dose hardened pulse width modulators designed to be used in high-frequency switching power supplies in either voltage or current-mode configurations. These devices include a precision voltage reference, a low power start-up circuit, a high-frequency oscillator, a wide-band error amplifier, and a fast current-limit comparator.

The IS-1825xSRH and IS-1825xSEH feature dual, alternating output operating from zero to less than 50% duty cycle, and the ISL71823xSRH features dual in-phase output operating from zero to less than 100% duty cycle. The B versions of the parts test the delay from clock out to PWM output switching after power has been applied to the modulator (t_{PWM}) (see Figure 2 on page 9). The SEH parts are wafer-by-wafer acceptance tested to 50krad(Si) at a low dose rate of <10mrad(Si)/s.

Constructed with the Rad-hard Silicon Gate (RSG) dielectrically isolated BiCMOS process, these devices are immune to single-event latch-up and have been specifically designed to provide a high level of immunity to single-event transients. All specified parameters are established and tested for 300krad(Si) total dose performance.

The devices are offered in a 16 Ld CDIP or a 20 Ld CDFP and fully specified to across the temperature range of -50°C to +125°C.

Applications

- Voltage or current mode switching power supplies
- Control of high current MOSFET drivers
- Motor speed and direction control

Features

- **Electrically screened to DLA SMD 5962-02511**
- **QML qualified per MIL-PRF-38535 requirements**
- **EH version is wafer-by-wafer acceptance tested to 50krad(Si) LDR**
- **Oscillator frequency: 1MHz (max)**
- **High output drive current: 1A peak (typ)**
- **Low startup current: 300µA (max)**
- Undervoltage Lockout
  - Start threshold: 8.8V (max)
  - Stop threshold: 7.6V (min)
  - Hysteresis: 300mV (min)
- Pulse-by-pulse current limiting
- Programmable leading edge blanking
- Radiation Hardness
  - High Dose Rate (HDR) (50-300rad(Si)/s): 300krad(Si)
  - Low Lose Rate (LDR) (0.01rad(Si)/s): 50krad(Si)
  - Latch-up immune (dielectrically isolated)
  - SEU immune: LET= 35MeV•cm^2/mg

Related Literature

- For a full list of related documents, visit our website
  - IS-1825ASRH, IS-1825BSRH, IS-1825BSEH, ISL71823ASRH, and ISL71823BSRH product pages

Table 1. Key Differences Between Family of Parts

Part Number	Dual Outputs	Radiation Hardened Assurance Testing		Clock-to-PWM Startup Test
		TID HDR Rating (50-300 rad(Si)/s)	TID LDR Rating (<10mrad(Si)/s)	
IS-1825ASRH	Out of Phase	300krad(Si)	-	-
IS-1825BSRH	Out of Phase	300krad(Si)	-	Yes
IS-1825BSEH	Out of Phase	300krad(Si)	50krad(Si)	Yes
ISL71823ASRH	In Phase	300krad(Si)	-	-
ISL71823BSRH	In Phase	300krad(Si)	-	Yes

Contents

1. Overview

1.1 Functional Block Diagram

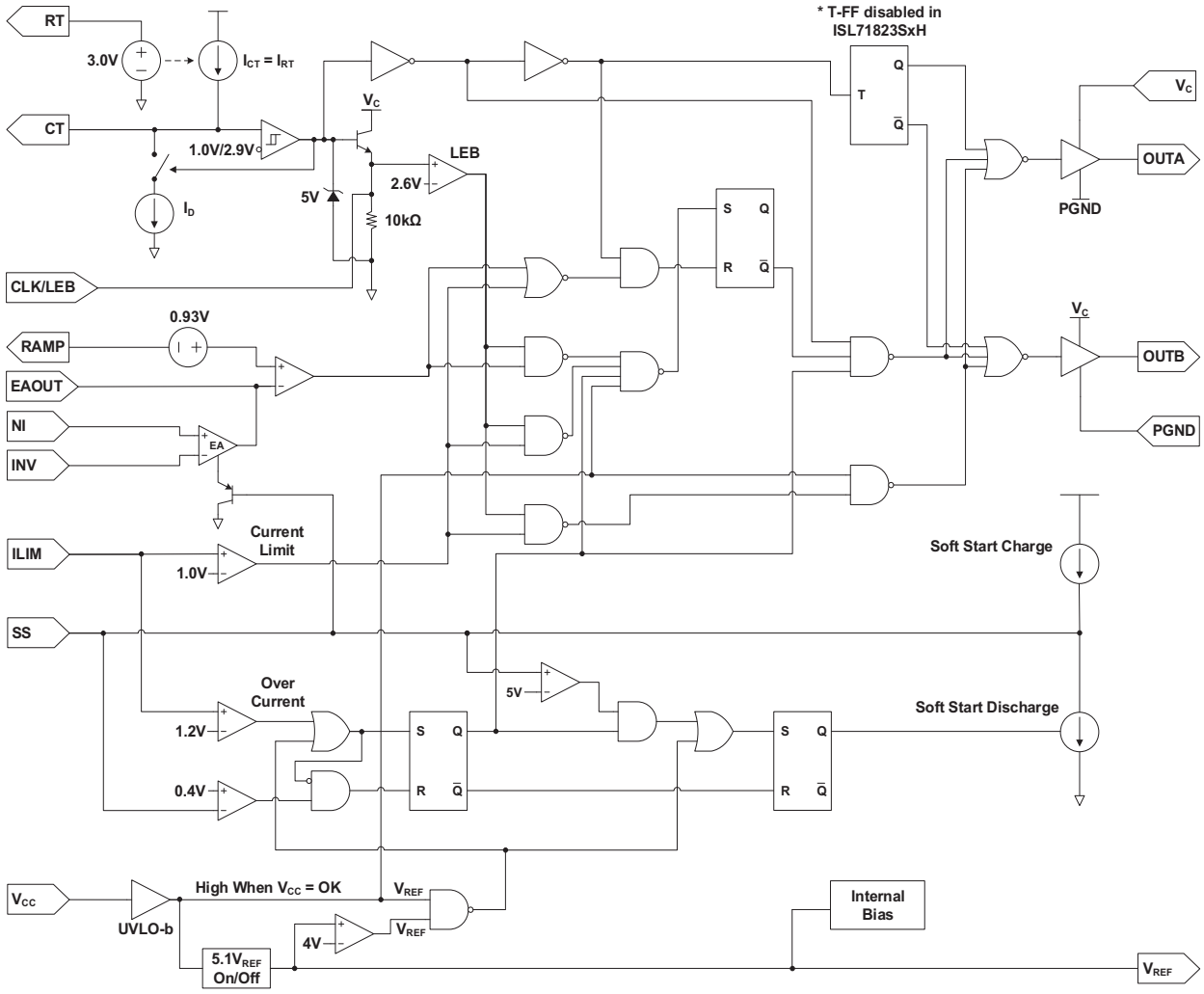


Figure 1. Block Diagram

1.2 Ordering Information

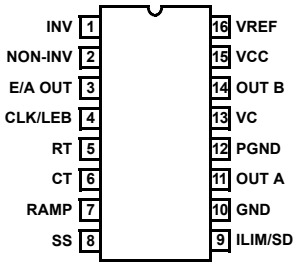
Ordering SMD Number (Note 1)	Part Number (Note 2)	Radiation Hardness Assurance		Temperature Range (°C)	Package (RoHS Compliant)	Package Drawing
		HDR	LDR			
N/A	IS0-1825ASRH/SAMPLE (Note 3)	-	-	-50 to +125	DIE	-
5962F0251101V9A	IS0-1825ASRH-Q	300krad(Si)	-	-50 to +125	DIE	-
5962F0251101QEC	IS1-1825ASRH-8	300krad(Si)	-	-50 to +125	16 Ld SBDIP	D16.3
5962F0251101QXC	IS9-1825ASRH-8	300krad(Si)	-	-50 to +125	20 Ld FP	K20.A
5962F0251101VEC	IS1-1825ASRH-Q	300krad(Si)	-	-50 to +125	16 Ld SBDIP	D16.3
5962F0251101VXC	IS9-1825ASRH-Q	300krad(Si)	-	-50 to +125	20 Ld FP	K20.A
N/A	IS1-1825ASRH/PROTO (Note 3)	-	-	-50 to +125	16 Ld SBDIP	D16.3
N/A	IS9-1825ASRH/PROTO (Note 3)	-	-	-50 to +125	20 Ld FP	K20.A
5962F0251102QEC	ISL71823ASRHQD	300krad(Si)	-	-50 to +125	16 Ld SBDIP	D16.3
5962F0251102QXC	ISL71823ASRHQF	300krad(Si)	-	-50 to +125	20 Ld FP	K20.A
5962F0251102VEC	ISL71823ASRHVD	300krad(Si)	-	-50 to +125	16 Ld SBDIP	D16.3
5962F0251102VXC	ISL71823ASRHVF	300krad(Si)	-	-50 to +125	20 Ld FP	K20.A
5962F0251102V9A	ISL71823ASRHVX	300krad(Si)	-	-50 to +125	DIE	-
N/A	ISL71823ASRHD/PROTO (Note 3)	-	-	-50 to +125	16 Ld SBDIP	D16.3
N/A	ISL71823ASRHF/PROTO (Note 3)	-	-	-50 to +125	20 Ld FP	K20.A
N/A	ISL71823ASRHX/SAMPLE (Note 3)	-	-	-50 to +125	DIE	-
5962F0251103V9A	IS0-1825BSRH-Q	300krad(Si)	-	-50 to +125	DIE	-
5962F0251103QEC	IS1-1825BSRH-8	300krad(Si)	-	-50 to +125	16 Ld SBDIP	D16.3
5962F0251103QXC	IS9-1825BSRH-8	300krad(Si)	-	-50 to +125	20 Ld FP	K20.A
5962F0251103VEC	IS1-1825BSRH-Q	300krad(Si)	-	-50 to +125	16 Ld SBDIP	D16.3
5962F0251103VXC	IS9-1825BSRH-Q	300krad(Si)	-	-50 to +125	20 Ld FP	K20.A
5962F0251104QEC	ISL71823BSRHQD	300krad(Si)	-	-50 to +125	16 Ld SBDIP	D16.3
5962F0251104QXC	ISL71823BSRHQF	300krad(Si)	-	-50 to +125	20 Ld FP	K20.A
5962F0251104VEC	ISL71823BSRHVD	300krad(Si)	-	-50 to +125	16 Ld SBDIP	D16.3
5962F0251104VXC	ISL71823BSRHVF	300krad(Si)	-	-50 to +125	20 Ld FP	K20.A
5962F0251104V9A	ISL71823BSRHVX	300krad(Si)	-	-50 to +125	DIE	-
5962F0251105V9A	IS0-1825BSEH-Q	300krad(Si)	50krad(Si)	-50 to +125	DIE	-
5962F0251105VEC	IS1-1825BSEH-Q	300krad(Si)	50krad(Si)	-50 to +125	16 Ld SBDIP	D16.3
5962F0251105VXC	IS9-1825BSEH-Q	300krad(Si)	50krad(Si)	-50 to +125	20 Ld FP	K20.A

Notes:

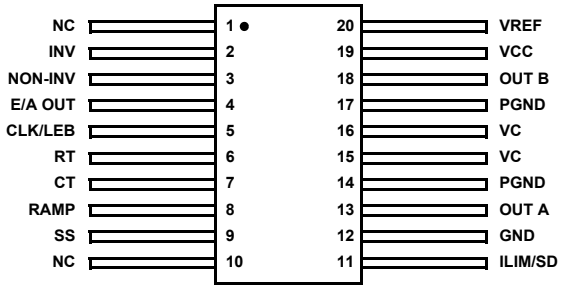
1. Specifications for Rad Hard QML devices are controlled by the Defense Logistics Agency Land and Maritime (DLA). The SMD numbers listed must be used when ordering.
2. These Pb-free Hermetic packaged products employ 100% Au plate - e4 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations.
3. The /PROTO and /SAMPLE are not rated or certified for Total Ionizing Dose (TID) or Single Event Effect (SEE) immunity. These parts are intended for engineering evaluation purposes only. The /PROTO parts meet the electrical limits and conditions across the temperature range specified in the DLA SMD and are in the same form and fit as the qualified device. The /SAMPLE die is capable of meeting the electrical limits and conditions specified in the DLA SMD at +25°C only. The /SAMPLE is a die and does not receive 100% screening across the temperature range to the DLA SMD electrical limits. These part types do not come with a certificate of conformance because there is no radiation assurance testing and they are not DLA qualified devices.

1.3 Pin Configuration

IS1-1825ASRH, IS1-1825BSRH, IS-1825BSEH
ISL71823BSRHVD, ISL71823ASRHQD
(CDIP2-T16 SBDIP)
TOP VIEW



IS9-1825ASRH, IS9-1825BSRH, IS9-1825BSEH
ISL71823ASRHQF, ISL71823BSRHVF
(CDFP4-F20 FLATPACK)
TOP VIEW



1.4 Pin Descriptions

Pin Name	Pin Number		Description
	SBDIP	Flatpack	
INV	1	2	Inverting input for the error amplifier.
NON-INV	2	3	Non inverting input for the error amplifier.
E/A OUT	3	4	Error amplifier output.
CLK/LEB	4	5	Clock out pin with leading edge blanking.
R_T	5	6	Timing resistor pin for programming the oscillator.
C_T	6	7	Timing capacitor pin for programming the oscillator.
RAMP	7	8	Non inverting input to the PWM comparator with a 1.25V internal offset.
SS	8	9	Soft-Start pin for controlling startup ramp time and inrush current.
ILIM/SD	9	11	Input to the current limit comparator.
GND	10	12	Ground return for the analog circuitry.
OUTA	11	13	High current totem pole output of the driver stage.
PGND	12	14, 17	Ground return for the output driver stage.
V_C	13	15, 16	Power supply pin for the output stage. Bypass this pin with a 0.1µF capacitor with low ESL and minimize the trace length by placing it as close to the pin as possible.
OUTB	14	18	High current totem pole output of the driver stage.
V_{CC}	15	19	Power supply pin for the device. Bypass this pin with a 0.1µF capacitor with low ESL and minimize the trace length by placing it as close to the pin as possible.
V_{REF}	16	20	5.1V voltage reference.
NC	-	1, 10	Not electrically connected.

2. Specifications

2.1 Absolute Maximum Ratings

Parameter	Minimum	Maximum	Unit
V_C, V_{CC}	-	35	V
Analog Inputs (INV, NON-INV, RAMP, ILIM/SD, SS)	-0.3	VCC + 0.3	V
Power Dissipation	-	714	mW

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

2.2 Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
CDIP Package D16.3 (Notes 4, 5)	70	18
CDFP Package K20.A (Notes 4, 5)	80	15

Notes:
4. θ_{JA} is measured with the component mounted on a high-effective thermal conductivity test board in free air. See TB379.
5. For θ_{JC}, the “case temp” location is the center of the package underside.

Parameter	Minimum	Maximum	Unit
Maximum Junction Temperature		+175	°C
Storage Temperature Range	-65	+150	°C
Lead Temperature (Soldering 10 seconds)	-	+260	°C

2.3 Recommended Operating Conditions

Parameter	Minimum	Maximum	Unit
Temperature	-50	+125	°C
V_C, V_{CC}	12	20	V

2.4 Electrical Specifications

Unless otherwise noted, $V_S = V_C = V_{CC} = 12V$, $R_T=3.65k\Omega$, $C_T=1nF$, $T_A = +25°C$. **Boldface limits apply across the operating temperature range, -50°C to +125°C; over a total ionizing dose of 300krad(Si) with exposure at a high dose rate of 50 to 300rad(Si)/s; or over a total ionizing dose of 75krad(Si) with exposure at a low dose rate of <10mrad(Si)/s (SEH devices only).**

Parameter	Symbol	Test Conditions	Min (Note 7)	Typ	Max (Note 7)	Unit
Reference Section						
Output Voltage	V_{REF}		5.00	5.10	5.20	V
			4.92	-	**5.28**	V
Line Regulation	V_{LINE}	$12.0V < V_S < 20.0V$	-15	6.2	15	mV
			-20	-	**20**	mV
Load Regulation	V_{LOAD}	$1.0mA < I_{OUT} < 10.0mA$	-25	2.7	25	mV
			50	-	**50**	mV
Total Output Variation	V_{OM}	$V_S = 12.0V, 20.0V$, $I_{OUT} = 1.0mA, 10.0mA$	5.00	5.10	5.20	V
			4.92	-	**5.28**	V
Short Circuit Current	I_{SC}	$V_{REF} = 0V$	30	64	-	mA
			20	-	-	
Oscillator Section						
Initial Accuracy	F_O		340	379	425	kHz
			300	-	**425**	kHz
Voltage Stability	F_{PSRR}	$12.0V < V_S < 20.0V$, $T_A = +25°C$	-3	-0.4	3	%
		$12.0V < V_S < 20.0V$, $T_A = -55°C, +125°C$	-5	-	5	%
		$12.0V < V_S < 20.0V$, $T_A = +25°C$, Post Rad	-3	-	3	%
Total Variation	F_{OM}	$V_S = 12.0V, 20.0V$	340	366	425	kHz
			300	-	**425**	kHz
Clock Out High Voltage	V_{CLKH}		4.00	4.41	-	V
			3.75	-	-	V
Clock Out Low Voltage	V_{CLKL}		-	5.8	**200**	mV
CT Ramp Peak Voltage	$V_{CT(PEAK)}$		-	2.9	-	V
CT Ramp Valley Voltage	$V_{CT(VALLEY)}$		-	1.0	-	V
Error Amplifier Section						
Input Offset Voltage	V_{OS}	$V_{CM} = 3.0V$, $V_O = 3.0V$	**-10**	0.66	**10**	mV
Input Bias Current	I_{IBAS}	$V_{CM} = 3.0V$, $V_O = 3.0V$	**-2**	-0.44	**2**	µA
Input Offset Current	I_{OS}	$V_{CM} = 3.0V$, $V_O = 3.0V$	**-2**	0.07	**2**	µA
Open Loop Gain	A_{VOL}	$1.0V < V_O < 4.0V$	**60**	117	-	dB
Common Mode Rejection Ratio	CMRR	$1.5V < V_{CM} < 4.0V$, $T_A = +25°C$	65	100	-	dB
		$1.5V < V_{CM} < 4.0V$, $T_A = -55°C, +125°C$	45	-	-	dB
		$1.5V < V_{CM} < 4.0V$, $T_A = +25°C$, Post Rad	65	-	-	dB
Power Supply Rejection Ratio	PSRR	$12.0V < V_S < 20.0V$	**70**	119	-	dB
Gain-Bandwidth Product	GBWP		-	13	-	MHz
Output Sink Current	I_{OL}	$V_{E/A\ OUT} = 1.0V$	**1**	11	-	mA
Output Source Current	I_{OH}	$V_{E/A\ OUT} = 4.0V$	**-0.5**	-9	**-**	mA
Output High Voltage	$V_{E/A\ OH}$	$I_{E/A\ OUT} = -0.5mA$	**4**	4.6	-	V

Unless otherwise noted, $V_S = V_C = V_{CC} = 12V$, $R_T=3.65k\Omega$, $C_T=1nF$, $T_A = +25°C$. **Boldface limits apply across the operating temperature range, -50°C to +125°C; over a total ionizing dose of 300krad(Si) with exposure at a high dose rate of 50 to 300rad(Si)/s; or over a total ionizing dose of 75krad(Si) with exposure at a low dose rate of <10mrad(Si)/s (SEH devices only).**

Parameter	Symbol	Test Conditions	Min (Note 7)	Typ	Max (Note 7)	Unit
Output Low Voltage	$V_{E/A\ OL}$	$I_{E/A\ OUT}$ = 1.0 mA	**-**	0.6	**1.0**	V
Rising Slew Rate	SR_R		-	12	-	V/µs
Falling Slew Rate	SR_F		-	14	-	V/µs
Pulse Width Modulator (PWM) Comparator Section						
Ramp Bias Current	I_{RAMP}	V_{RAMP} = 0V	**-**	-0.2	**-8**	µA
Duty Cycle Range	DC_{MAX}	IS-1825xSRH, IS-1825xSEH	**40**	44	-	%
		ISL71823xSRH	**80**	90	-	%
E/A OUT Zero DC Threshold Voltage	$RAMP_{OFFSET}$	V_{RAMP} = 0V	**0.81**	0.93	-	V
Delay to Output Time	t_{DELAY}	$V_{E/A\ OUT}$ = 0V to 5V Step	**-**	600	-	ns
Soft Start Section						
Charge Current	I_{CHG}	V_{SS} = 2.5V, T_A = +25°C	8	15	20	µA
		V_{SS} = 2.5V, T_A = +125°C	8	-	25	µA
		V_{SS} = 2.5V, T_A = -55°C	8	-	29	µA
		V_{SS} = 2.5V, T_A = +25°C, Post Rad	8	-	25	µA
Discharge Current	I_{DCHG}	Soft start voltage = 2.5V	**0.1**	0.2	**0.5**	mA
Current Limit / Start Sequence / Fault Section						
Restart Threshold	V_{RS}		-	0.4	**0.5**	V
ILIM Bias Current	I_{BLIM}	0.0V < V_{ILIM} < 2.0V	-	1.4	**15**	µA
Current Limit Threshold	V_{LIMIT}		**0.85**	0.98	**1.15**	V
Over Current Threshold	V_{OVER}		**1.05**	1.18	**1.26**	V
Current Limit Delay	$t_{ILIMIT-DEL}$		-	180	-	ns
Over Current Delay	$t_{OVER-DEL}$		-	100	-	ns
Output Section						
Output Low Saturation	V_{SATL}	I_{OUT} = 20mA, T_A = +25°C	-	0.7	0.8	V
		I_{OUT} = 20mA, T_A = -55°C, +125°C	-	-	1.0	V
		I_{OUT} = 20mA, T_A = +25°C, Post Rad	-	-	0.8	V
		I_{OUT} = 200 mA	-	1.0	**2.2**	V
Output High Saturation	V_{SATH}	I_{OUT} = 20mA	**10**	11.2	-	V
		I_{OUT} = 200 mA	**9**	10.8	-	V
Under Voltage Lockout (UVLO) Output Low Saturation Voltage	$UVLO_{OLS}$	I_{OUT} = 20mA	-	0.7	**1.2**	V
Clock Out to PWM Switching Startup Delay (See Figure 2) (IS-1825BSxH and ISL71823BSRH only)	t_{PWM}	T_A = +25°C	200	291	380	µs
		T_A = +125°C	400	-	660	µs
		T_A = -55°C	100	-	278	µs
		T_A = +25°C, Post Rad	200	-	380	µs
Under Voltage Section						
Start Threshold Voltage	V_{START}		**8.2**	8.6	**8.8**	V
Stop Threshold Voltage	V_{STOP}		**7.6**	8.0	**8.4**	V
Under Voltage Lockout Hysteresis	V_{HYS}		**0.3**	0.6	**1.2**	V

Unless otherwise noted, $V_S = V_C = V_{CC} = 12V$, $R_T=3.65k\Omega$, $C_T=1nF$, $T_A = +25°C$. **Boldface limits apply across the operating temperature range, -50°C to +125°C; over a total ionizing dose of 300krad(Si) with exposure at a high dose rate of 50 to 300rad(Si)/s; or over a total ionizing dose of 75krad(Si) with exposure at a low dose rate of <10mrad(Si)/s (SEH devices only).**

Parameter	Symbol	Test Conditions	Min (Note 7)	Typ	Max (Note 7)	Unit
Supply Current Section						
Startup Current	I_{SU}	V_S = 8.0V	-	55	**300**	µA
Supply Current	I_{CC}	$V_{INV} = V_{RAMP} = V_{ILIM/SD}$ = 0.0V $V_{NON-INV}$ = 1.0V	-	25	**36**	mA

Notes:

6. Typical values shown are not guaranteed.
7. Parameters with MIN and/or MAX limits are 100% tested at -50°C, +25°C, and +125°C, unless otherwise specified.
8. V_C and V_{CC} must always be at the same potential.

2.5 Timing Diagram

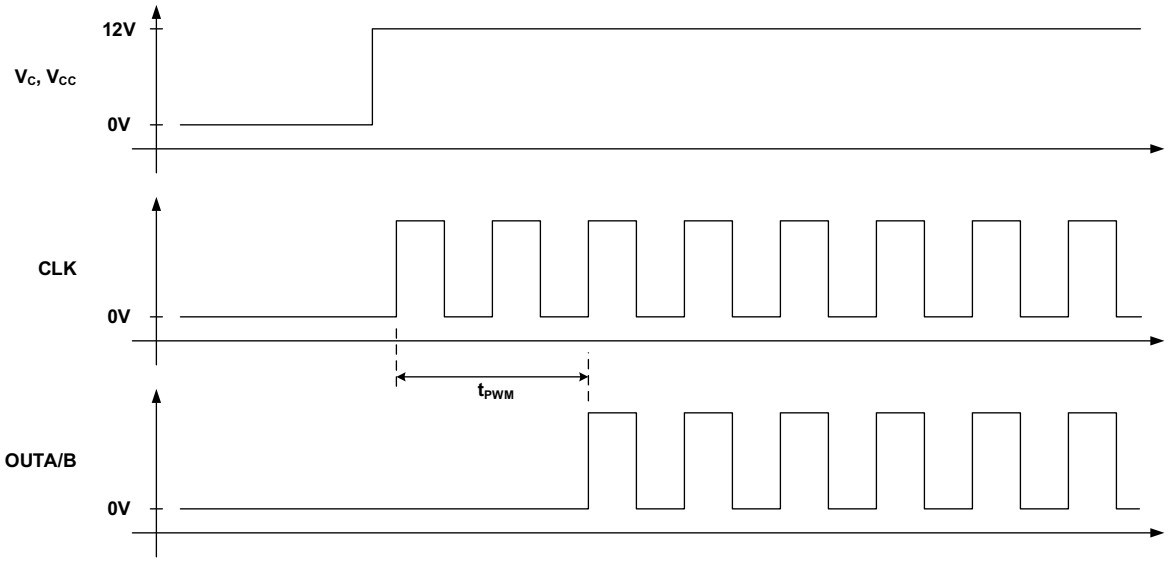


Figure 2. Timing Diagram for Clock Out to PWM Switching Delay Test (t_{PWM})

3. Typical Performance Curves

Unless otherwise noted, $V_S = V_C = V_{CC} = 12V$, $R_T=3.65k\Omega$, $C_T=1nF$, $T_A = +25°C$

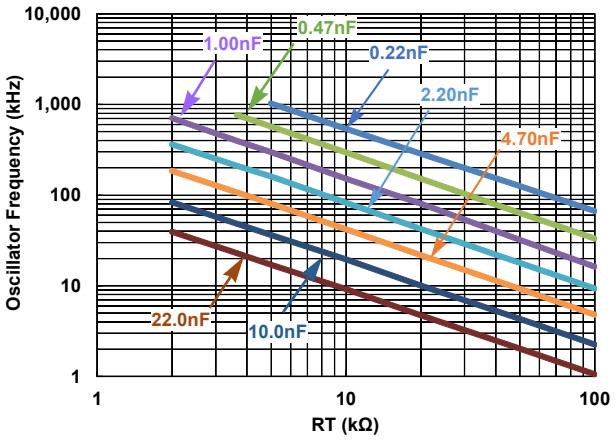


Figure 3. Oscillator Frequency vs RT and CT (+25°C)

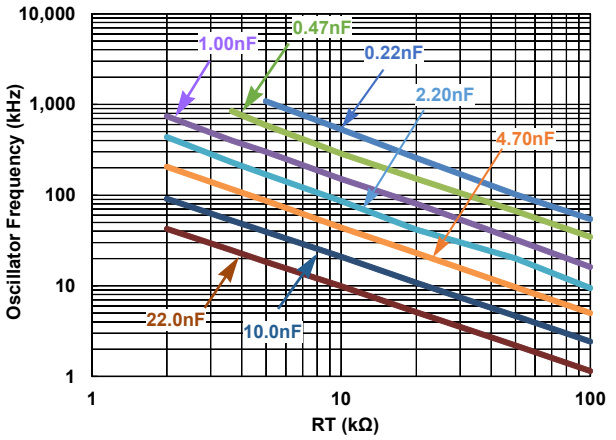


Figure 4. Oscillator Frequency vs RT and CT (+125°C)

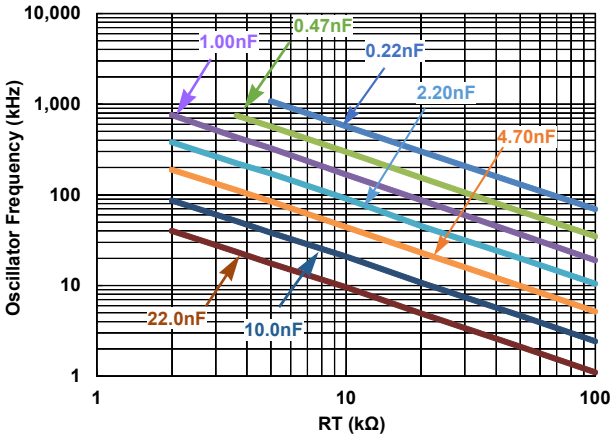


Figure 5. Oscillator Frequency vs RT and CT (-50°C)

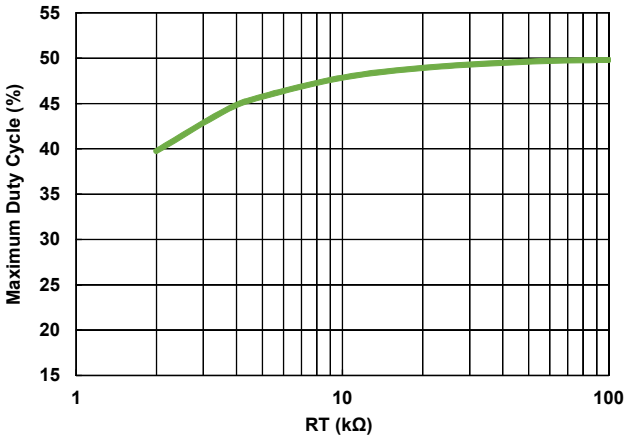


Figure 6. Maximum Duty Cycle vs RT (+25°C)

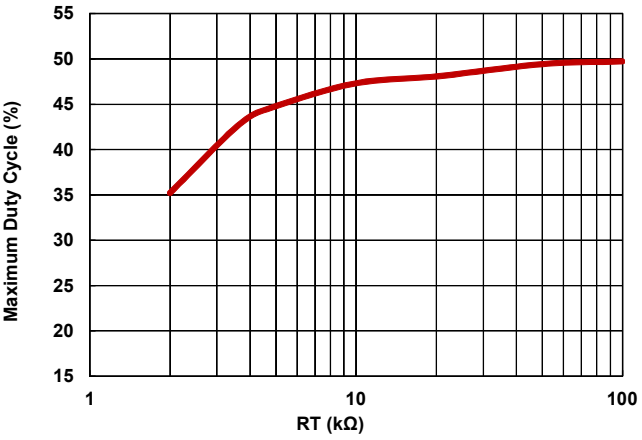


Figure 7. Maximum Duty Cycle vs RT (+125°C)

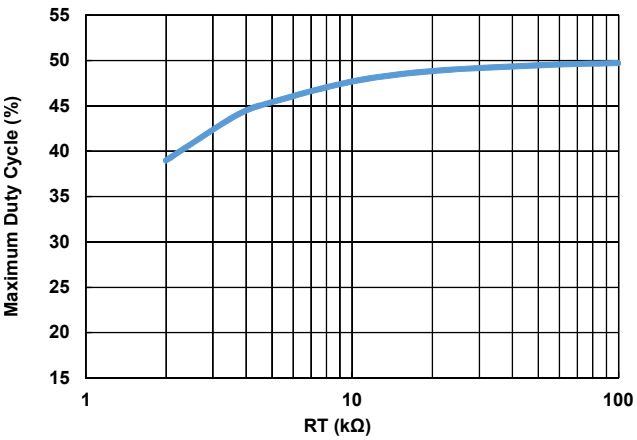


Figure 8. Maximum Duty Cycle vs RT (-50°C)

Unless otherwise noted, $V_S = V_C = V_{CC} = 12V$, $R_T=3.65k\Omega$, $C_T=1nF$, $T_A = +25°C$ **(Continued)**

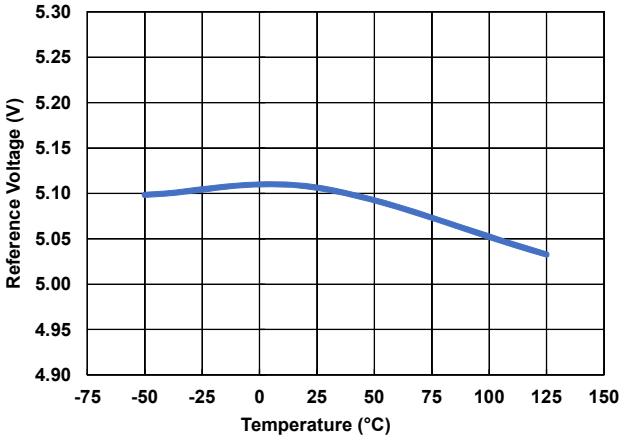


Figure 9. V_{REF} vs Temperature

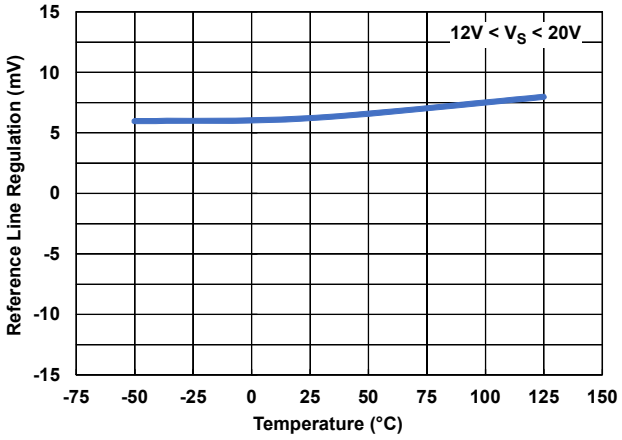


Figure 10. V_{REF} Line Regulation vs Temperature

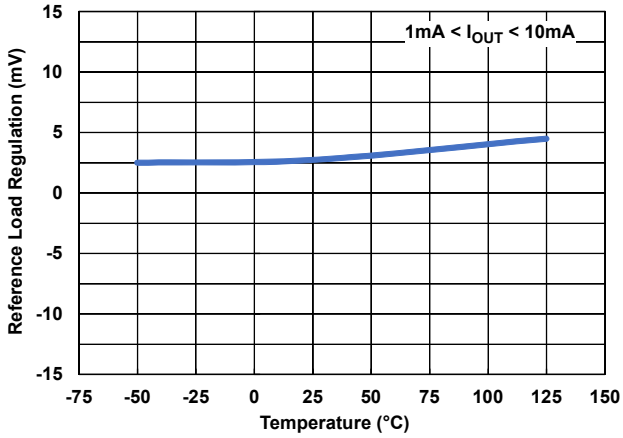


Figure 11. V_{REF} Load Regulation vs Temperature

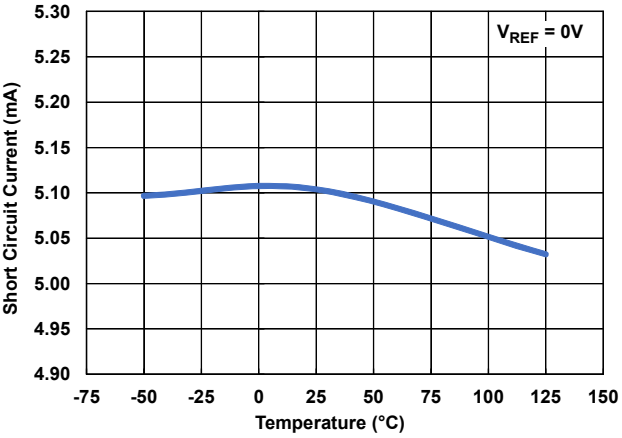


Figure 12. V_{REF} Short Circuit Current vs Temperature

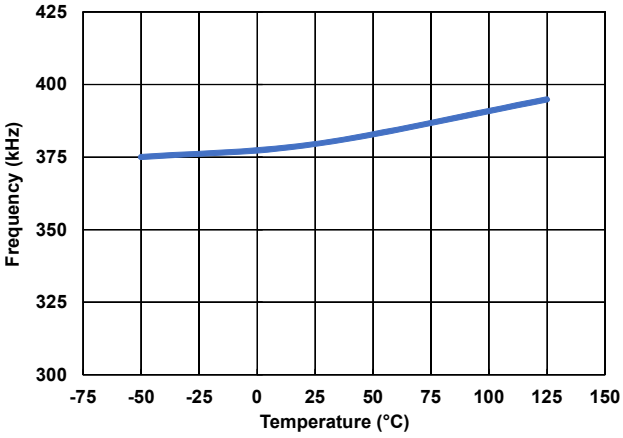


Figure 13. Oscillator Initial Accuracy vs Temperature

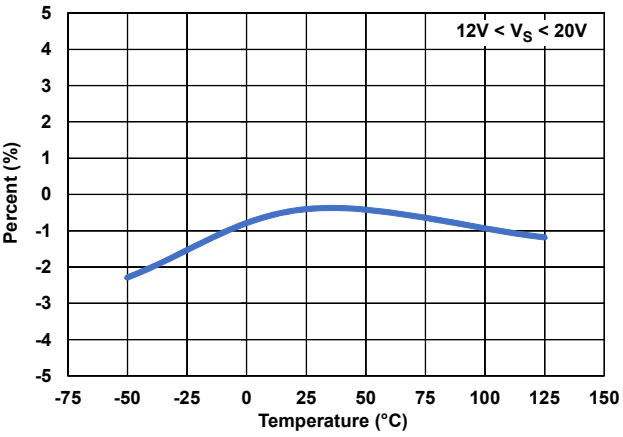


Figure 14. Oscillator Voltage Stability vs Temperature

Unless otherwise noted, $V_S = V_C = V_{CC} = 12V$, $R_T=3.65k\Omega$, $C_T=1nF$, $T_A = +25°C$ **(Continued)**

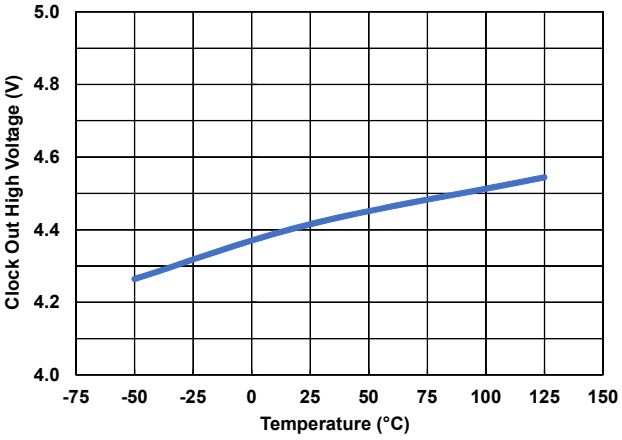


Figure 15. Oscillator V_{CLKH} vs Temperature

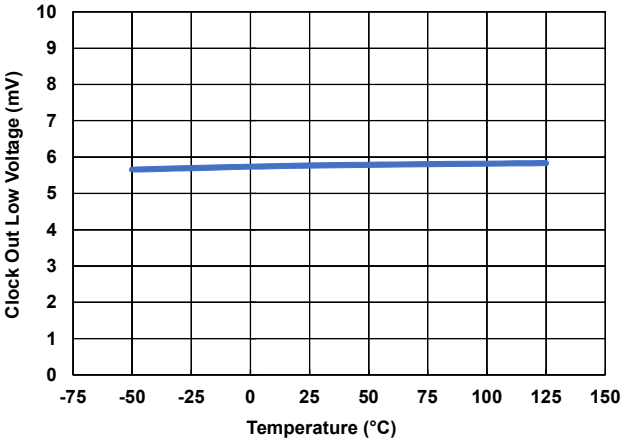


Figure 16. Oscillator V_{CLKL} vs Temperature

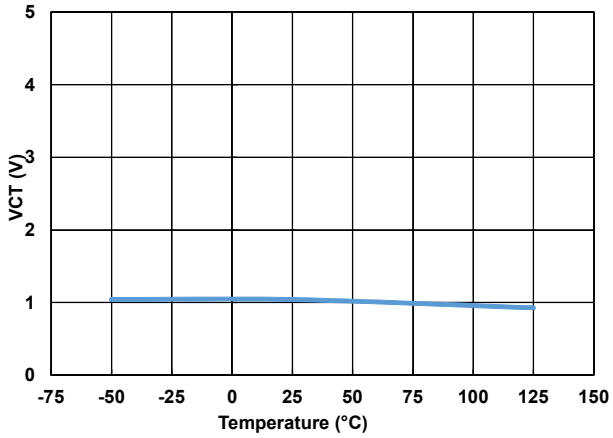


Figure 17. CT Valley Voltage vs Temperature

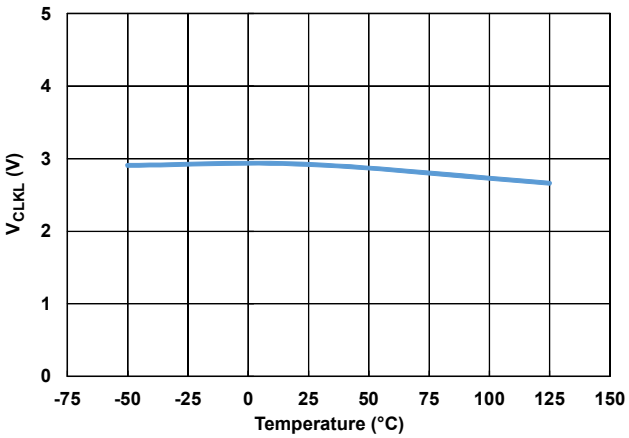


Figure 18. CT Peak Voltage vs Temperature

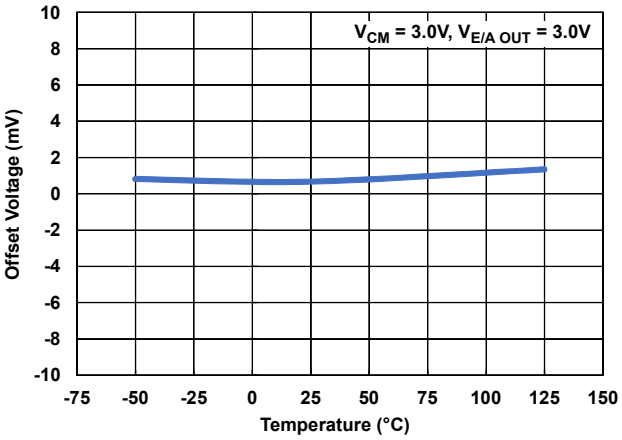


Figure 19. Error Amp V_{OS} vs Temperature

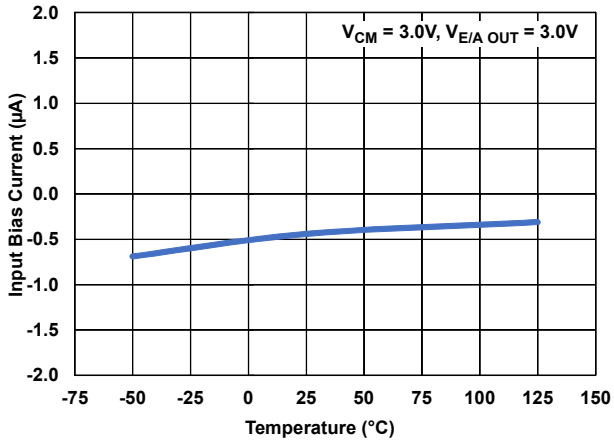


Figure 20. Error Amp I_{BIAS} vs Temperature

Unless otherwise noted, $V_S = V_C = V_{CC} = 12V$, $R_T=3.65k\Omega$, $C_T=1nF$, $T_A = +25°C$ **(Continued)**

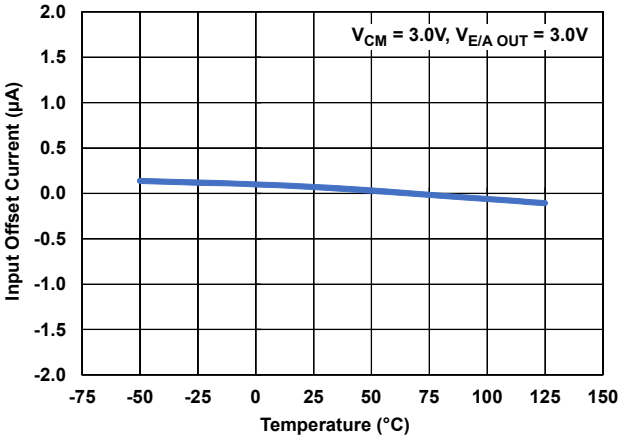


Figure 21. Error Amp I_{OS} vs Temperature

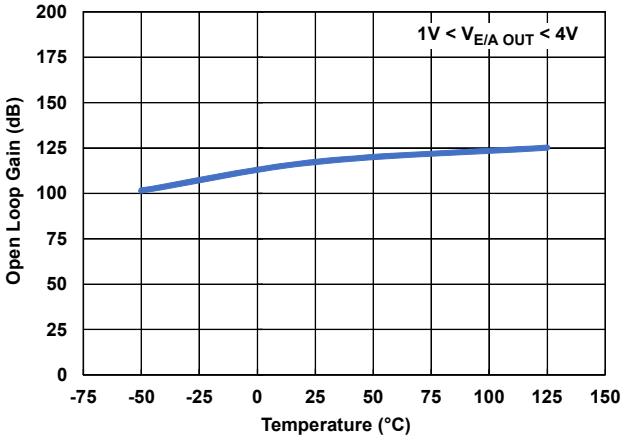


Figure 22. Error Amp A_{VOL} vs Temperature

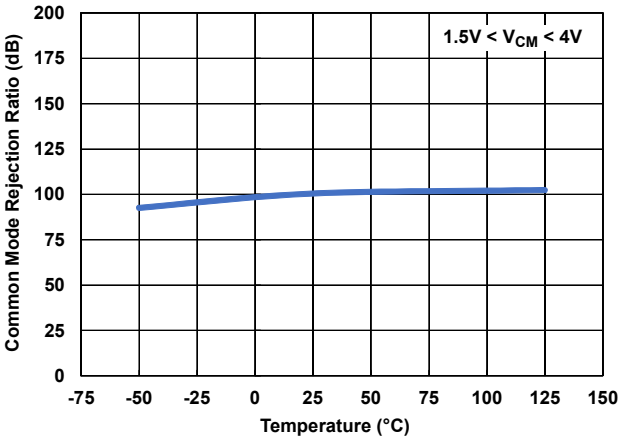


Figure 23. Error Amp CMRR vs Temperature

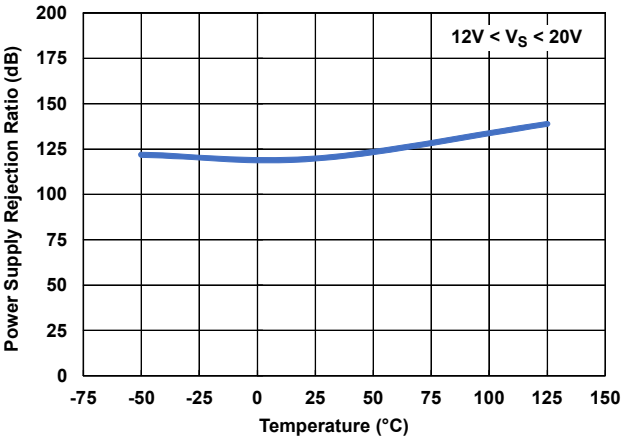


Figure 24. Error Amp PSRR vs Temperature

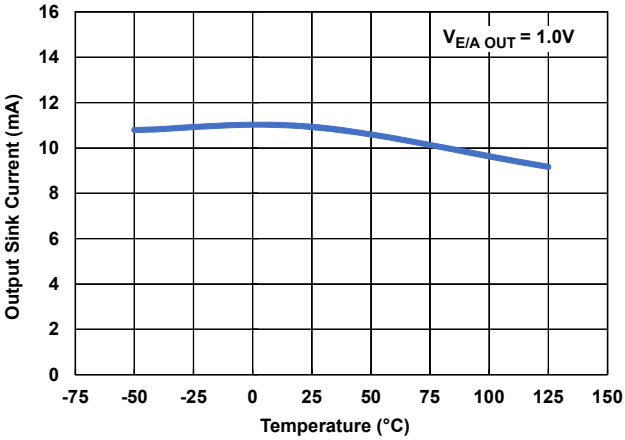


Figure 25. Error Amp I_{OL} vs Temperature

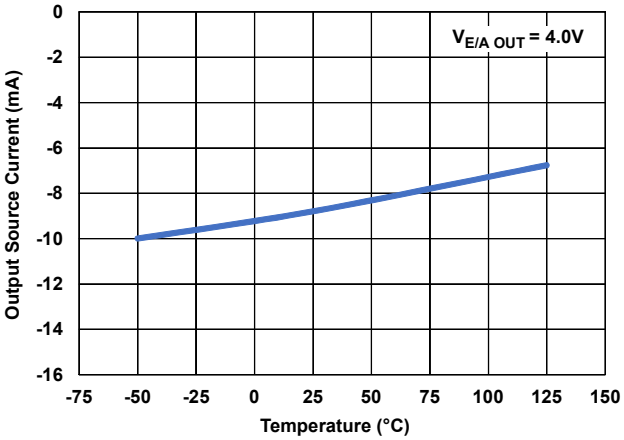


Figure 26. Error Amp I_{OH} vs Temperature

Unless otherwise noted, $V_S = V_C = V_{CC} = 12V$, $R_T=3.65k\Omega$, $C_T=1nF$, $T_A = +25°C$ **(Continued)**

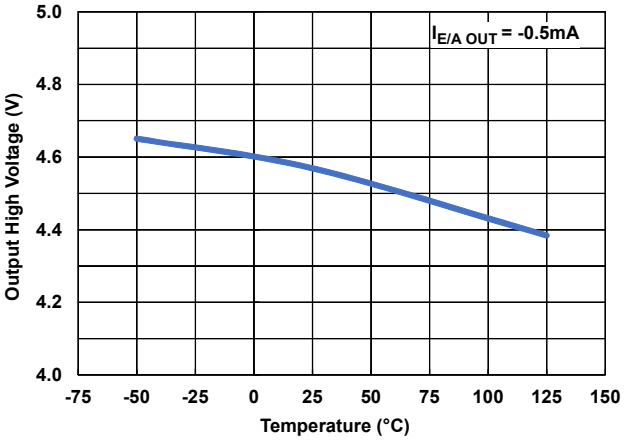


Figure 27. Error Amp V_{OH} vs Temperature

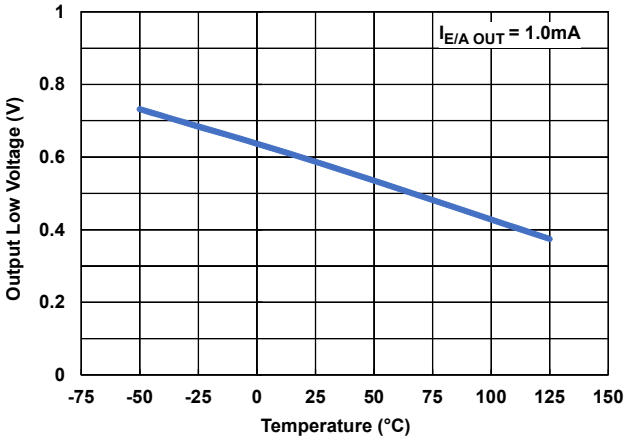


Figure 28. Error Amp V_{OL} vs Temperature

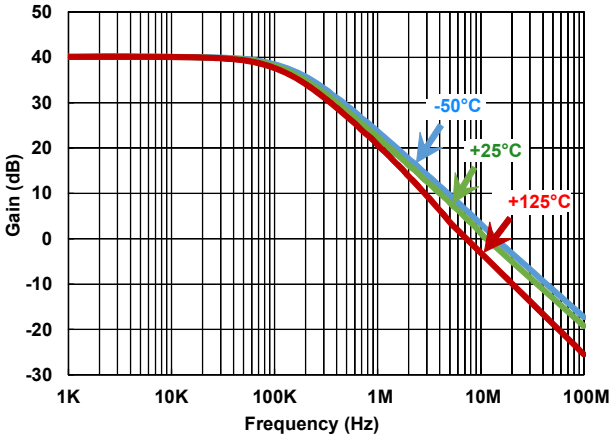


Figure 29. Error Amplifier Frequency Response

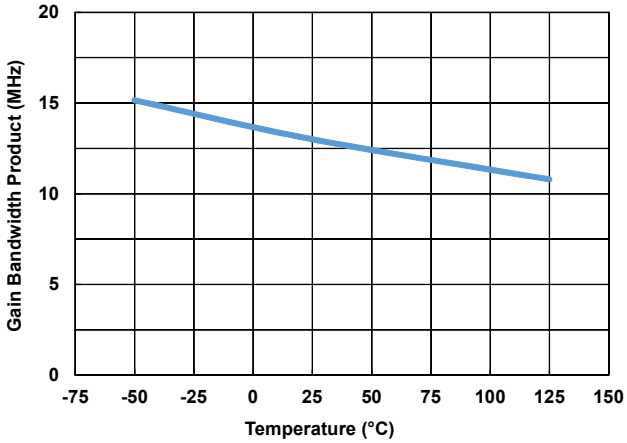


Figure 30. Error Amplifier GBWP vs Temperature

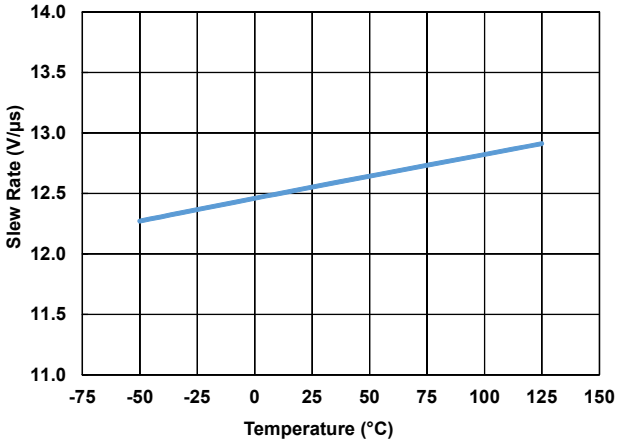


Figure 31. Error Amplifier Rising Slew Rate vs Temperature

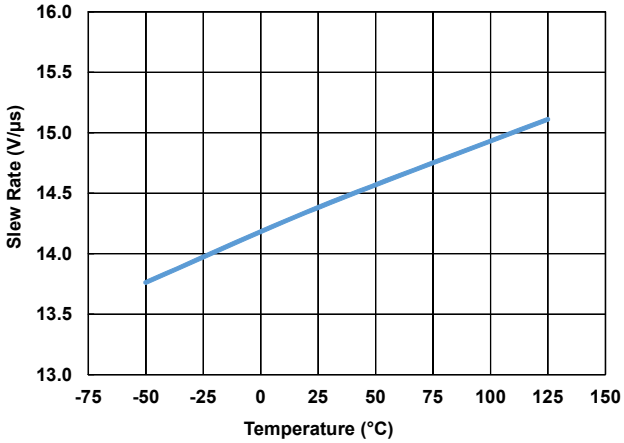


Figure 32. Error Amplifier Falling Slew Rate vs Temperature

Unless otherwise noted, $V_S = V_C = V_{CC} = 12V$, $R_T=3.65k\Omega$, $C_T=1nF$, $T_A = +25°C$ **(Continued)**

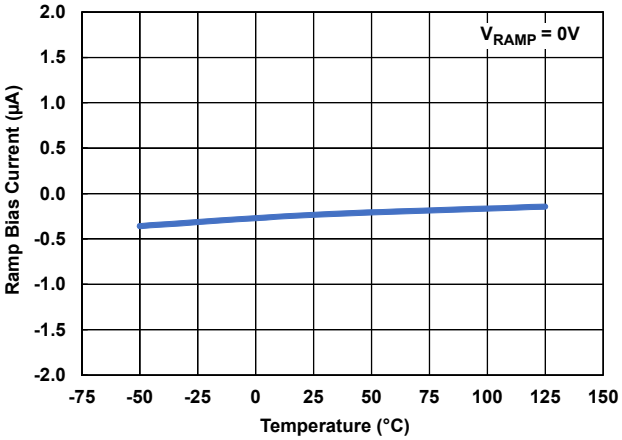


Figure 33. Ramp Bias Current vs Temperature

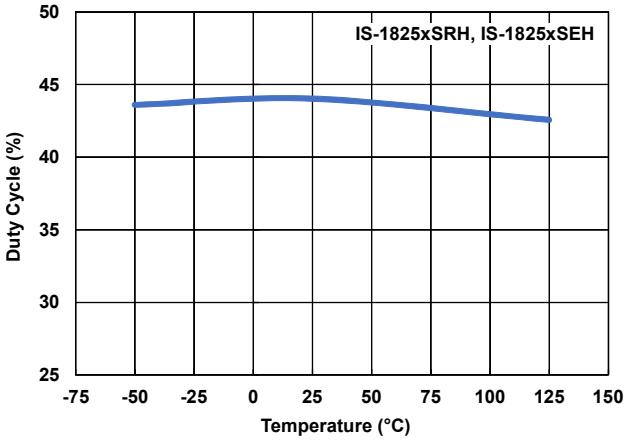


Figure 34. Maximum Duty Cycle vs Temperature

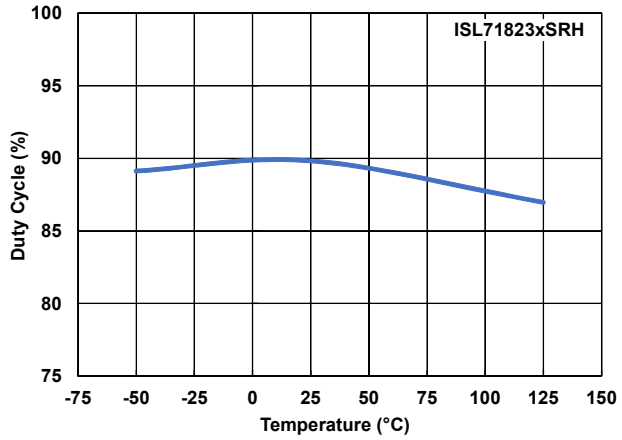


Figure 35. Maximum Duty Cycle vs Temperature

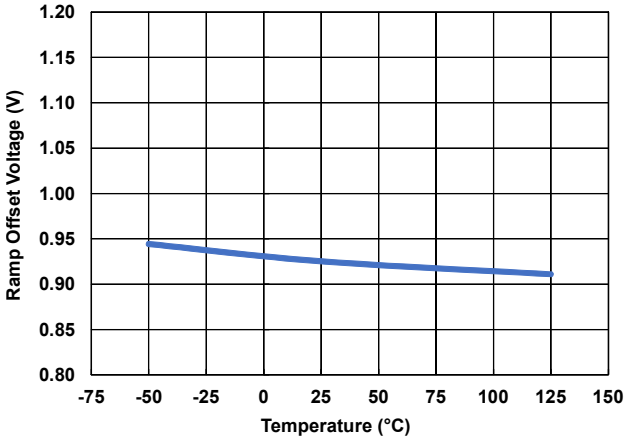


Figure 36. Ramp Offset vs Temperature

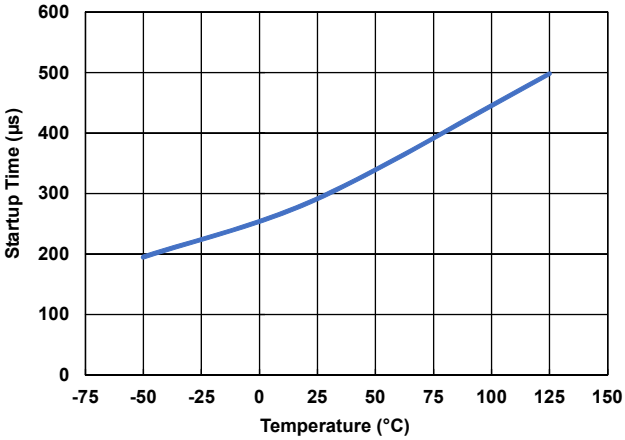


Figure 37. Clock to PWM Startup Delay vs Temperature

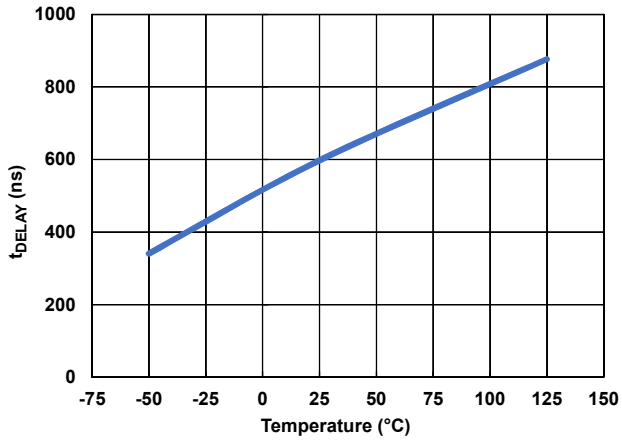


Figure 38. PWM Comparator to OUT Delay vs Temperature

Unless otherwise noted, $V_S = V_C = V_{CC} = 12V$, $R_T=3.65k\Omega$, $C_T=1nF$, $T_A = +25°C$ **(Continued)**

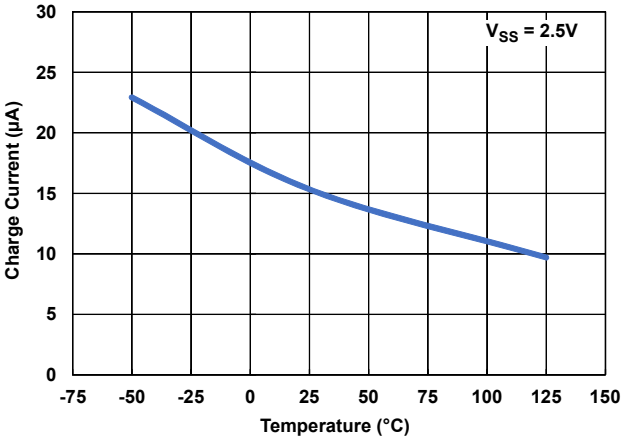


Figure 39. Soft Start Charge Current vs Temperature

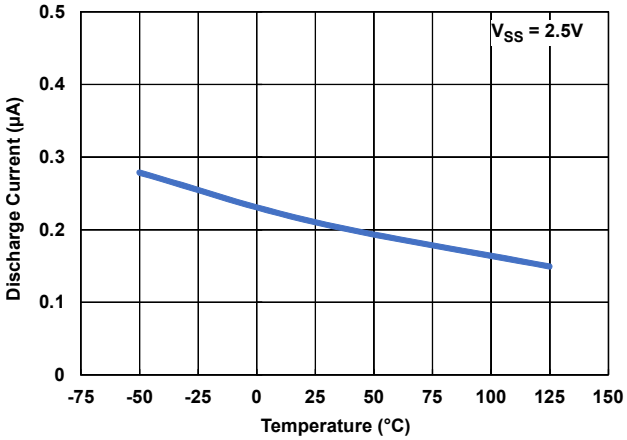


Figure 40. Soft Start Discharge Current vs Temperature

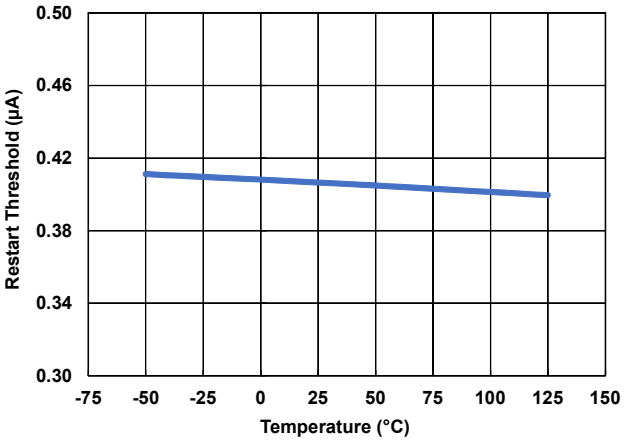


Figure 41. I_{LIM} Restart Threshold vs Temperature

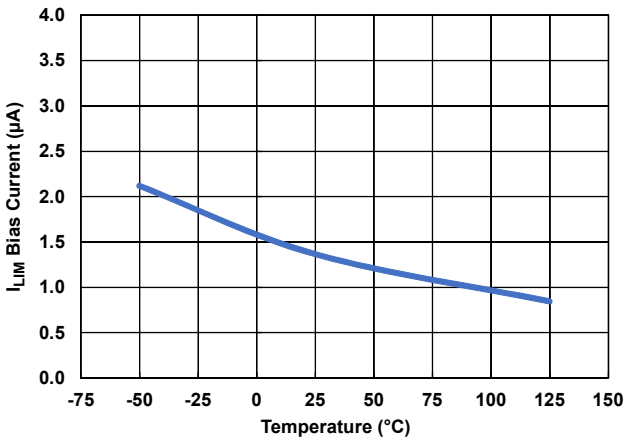


Figure 42. I_{LIM} Bias Current vs Temperature

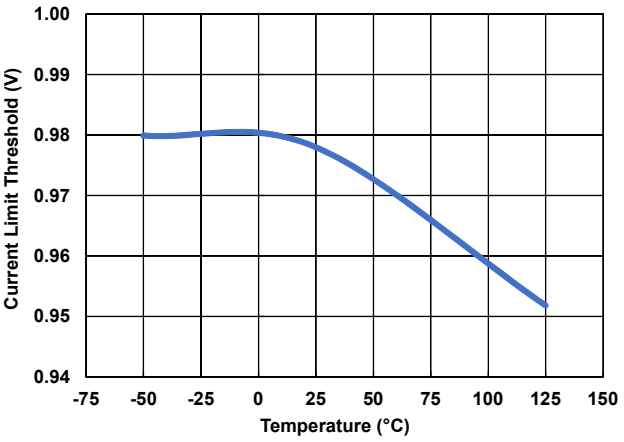


Figure 43. V_{LIMIT} vs Temperature

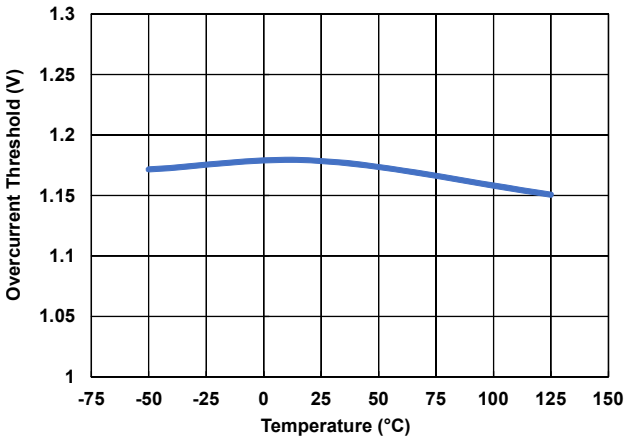


Figure 44. V_{OVER} vs Temperature

Unless otherwise noted, $V_S = V_C = V_{CC} = 12V$, $R_T=3.65k\Omega$, $C_T=1nF$, $T_A = +25°C$ **(Continued)**

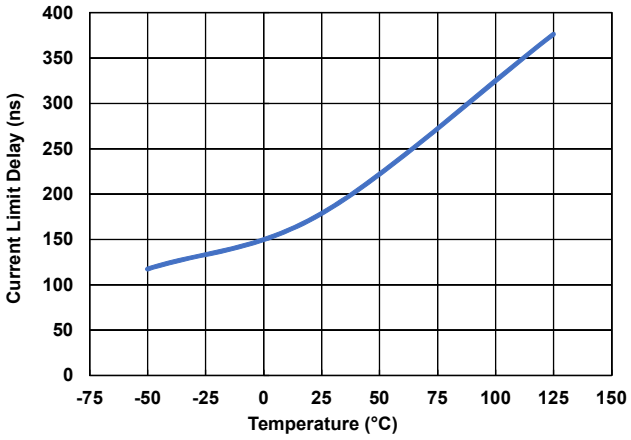


Figure 45. Current Limit Delay vs Temperature

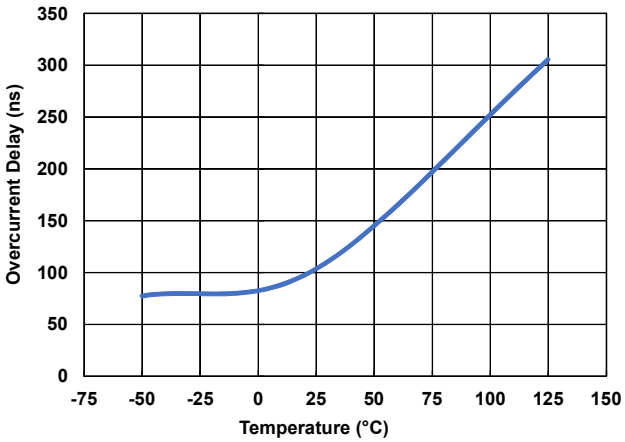


Figure 46. Overcurrent Delay vs Temperature

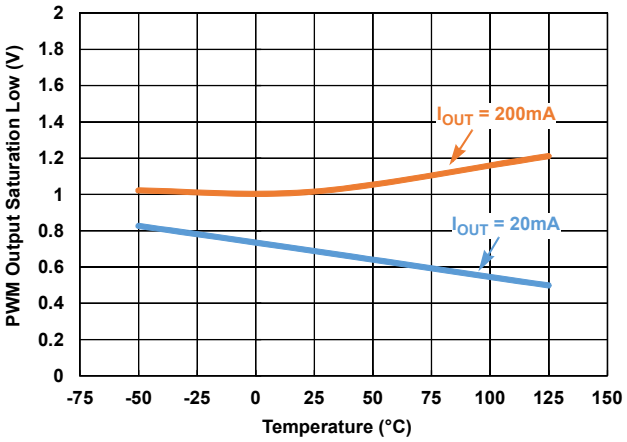


Figure 47. V_{SATL} vs Temperature

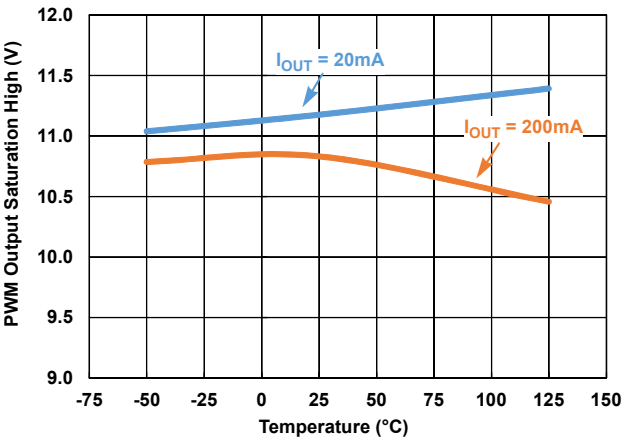


Figure 48. V_{SATH} vs Temperature

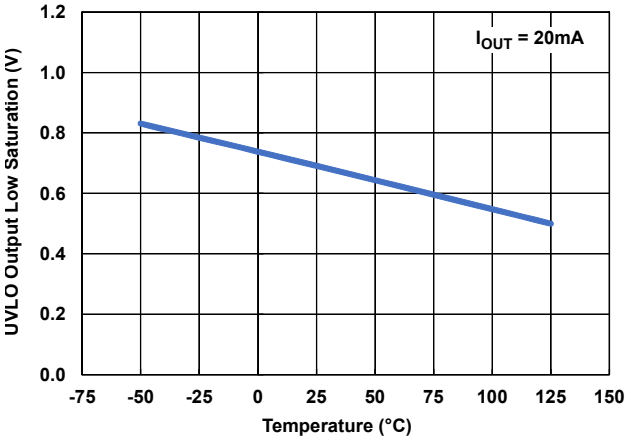


Figure 49. $UVLO_{OLS}$ vs Temperature

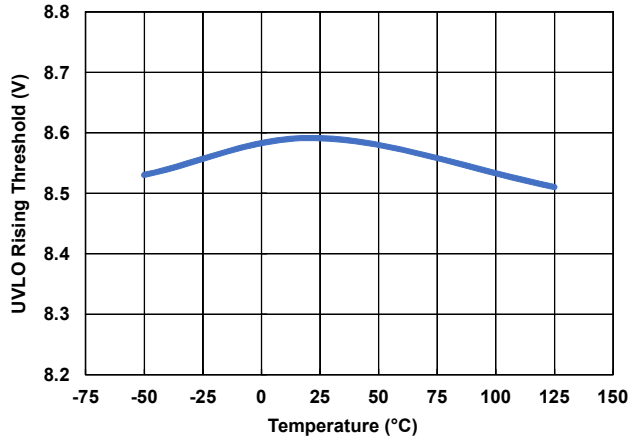


Figure 50. V_{START} vs Temperature

Unless otherwise noted, $V_S = V_C = V_{CC} = 12V$, $R_T=3.65k\Omega$, $C_T=1nF$, $T_A = +25°C$ **(Continued)**

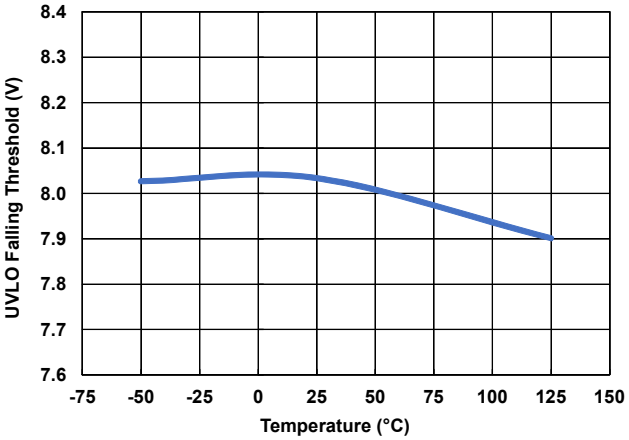


Figure 51. V_{STOP} vs Temperature

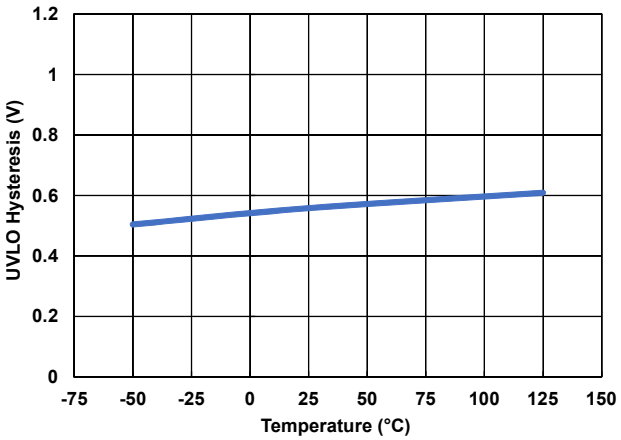


Figure 52. V_{HYS} vs Temperature

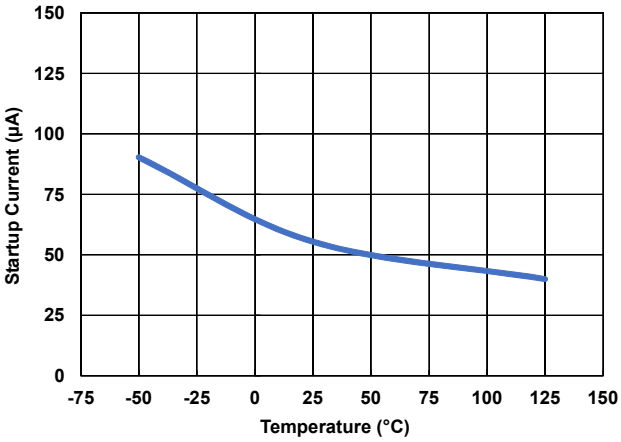


Figure 53. Startup Current vs Temperature

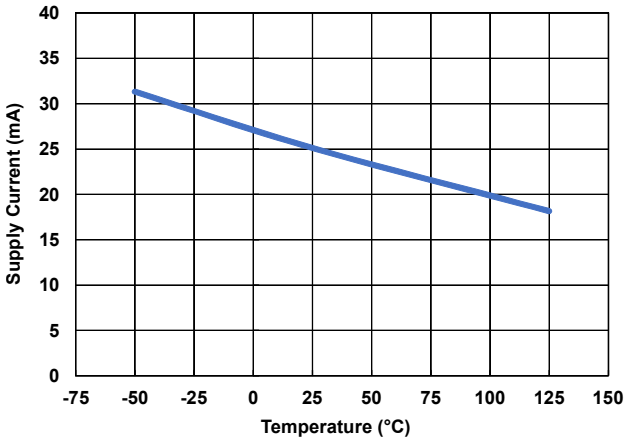


Figure 54. Supply Current vs Temperature

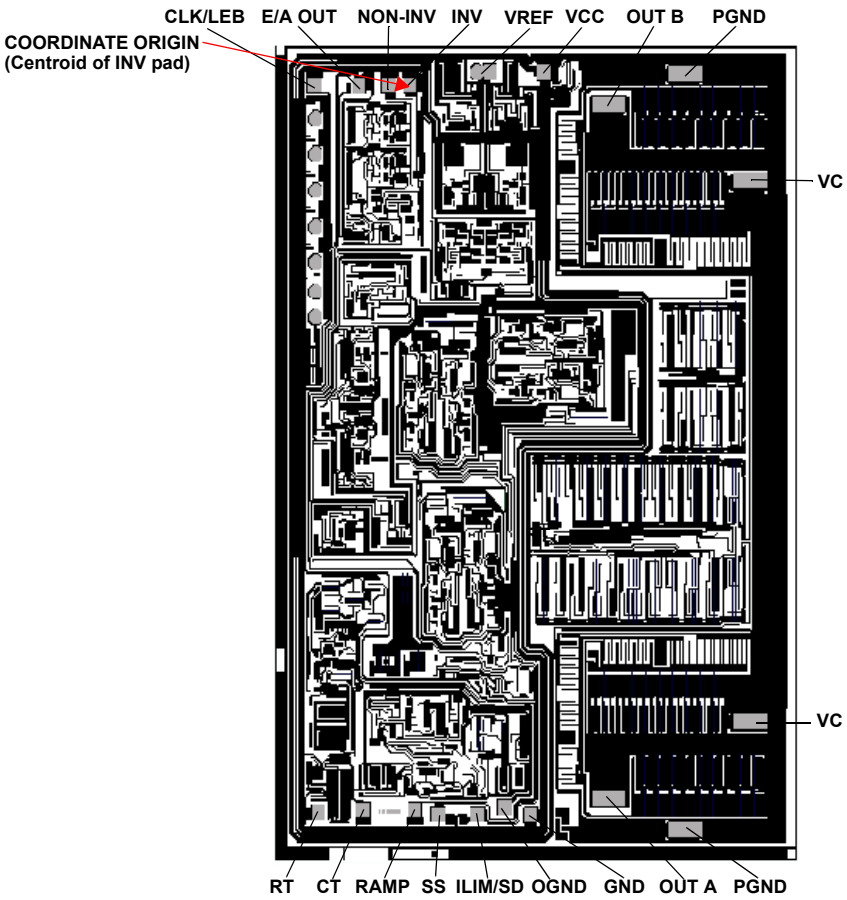
4. Die and Assembly Characteristics

Table 2. Die and Assembly Related Information

Die Information	
Dimensions	4310µm x 5840µm (170 mils x 230 mils) Thickness: 483µm ±25.4µm (19 mils ±1 mil)
Interface Materials	
Glassivation	Type: Phosphorus Silicon Glass (PSG) Thickness: 8.0kÅ ±1.0kÅ
Top Metallization	Type: AlCu (99.5%/0.5%) Thickness: 16.0kÅ ±2kÅ
Backside Finish	Silicon
Process	Radiation Hardened Silicon Gate, Dielectrically Isolated (DI)
Assembly Information	
Substrate Potential	Unbiased (DI)
Additional Information	
Worst Case Current Density	$<2x10^5$ A/cm^2
Transistor Count	585

4.1 Metallization Mask Layout

IS-1825xSRH, IS-1825xSEH, ISL71823xSRH



Notes:

9. Both the OGND (oscillator ground) and the GND (control circuit ground) pads must be bonded to ground. These pads are both bonded to the GND pin on the packaged devices.
10. All double-sized bond pads must be double bonded for current sharing purposes.

4.2 Bond Pad Coordinates

Table 3. Layout X-Y Coordinates (Centroid of bond pad)

Pad Number	Pad Name	X (µm)	Y (µm)	dX (µm)	dY (µm)
1	INV	0	0	110	110
2	NON-INV	-173	0	110	110
3	EA/OUT	-420	-5	110	110
4	CLK/LEB	-788	0	110	110
5	RT	-757	-5222	110	110
6	CT	-387	-5205	110	110
7	RAMP	46	-5205	110	110
8	SS	232	-5235	110	110
9	ILIM/SD	563	-5235	110	110
10	OGND	783	-5180	110	110
11	GND	1004	-5235	110	110
12	OUTA	1642	-5117.5	280	109
13	PGND	2274	-5341.5	280	109
14	VC	2812	-4570.5	280	109
15	VC	2812	-683.5	280	109
16	PGND	2274	87.5	280	109
17	OUTB	1642	-136.5	280	109
18	VCC	1107	94.5	110	110
19	VREF	622	110.5	110	110

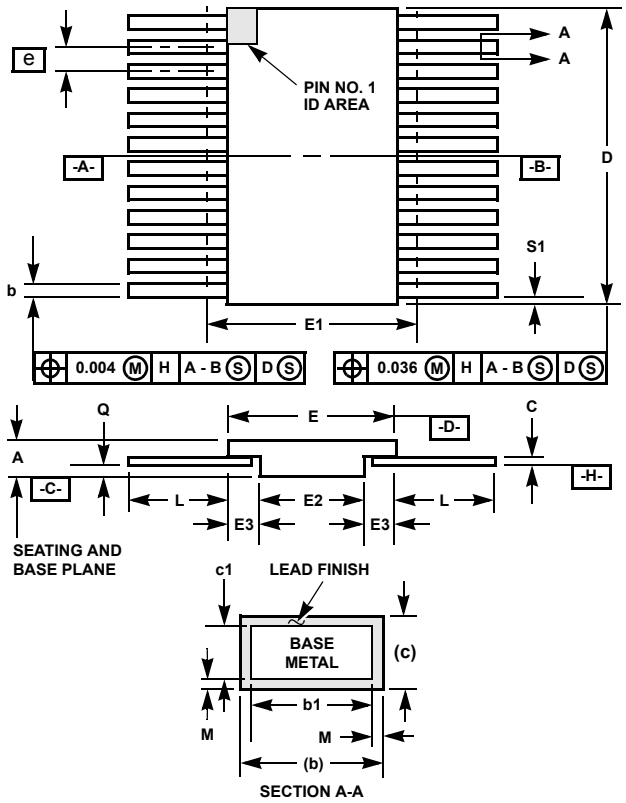
5. Revision History

Rev.	Date	Description
7.00	Jan 15, 2018	Updated second paragraph on page 1, changed “10mrad(Si)/s” to “<10mrad(Si)/s”. Added last paragraph on page 1. Added Table 1 on page 1. Added TOC. Updated Ordering information table by adding 2 new columns and Note 3 along with its cross reference. Added Pin Description section. Added Absolute Maximum Ratings, Thermal Information, and Recommended Operating Conditions sections. Added the Electrical Specifications table. Updated Figure 2. Added Typical Performance Curves. Added the Functional Block Diagram. Removed “About Intersil” section. Added new disclaimer Converted to the current document format.
6.00	Jan 5, 2017	Updated Related Literature on page 1. Removed ISL70417SEHVF from the ordering information table. Removed MSL note because it does not apply to hermetic packages. Updated Metallization Mask Layout. Updated About Intersil section.
5.00	Apr 23, 2013	Removed Part number IS-1825ASEH and added part numbers IS-1825BSEH, IS-1825BSRH, and ISL71823BSRH to ordering information table on page 2. SMD numbers in Ordering Information table corrected. Added timing diagram for CLK to OUT delay tPWM.
4.00	Apr 5, 2012	Updated to new Intersil template. Added Part IS-1825ASEH to Title and ordering information. Changed DSCC to DLA. Added typical oscillator performance curves. Updated ordering information by adding package, package drawing number, and sample parts.
3.00	Feb 19, 2008	Added ISL71823ASRH which is a metal option of the IS-1825ASRH.
2.00	Jun 14, 2005	Changed “u” to “µ” on pg 1 Features.
1.00	Jun 14, 2005	Removed “Trimmed Oscillator Discharge Current” from the Features section of both datasheets because the oscillator is not trimmed. Cosmetic edit only.
0.00	Jun 21, 2002	Initial release

6. Package Outline Drawings

For the most recent package outline drawing, see K20.A.

6.1 Ceramic Metal Seal Flatpack Packages (Flatpack)



K20.A MIL-STD-1835 CDFP4-F20 (F-9A, CONFIGURATION B)
20 LEAD CERAMIC METAL SEAL FLATPACK PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.045	0.115	1.14	2.92	-
b	0.015	0.022	0.38	0.56	-
b1	0.015	0.019	0.38	0.48	-
c	0.004	0.009	0.10	0.23	-
c1	0.004	0.006	0.10	0.15	-
D	-	0.540	-	13.72	3
E	0.245	0.300	6.22	7.62	-
E1	-	0.330	-	8.38	3
E2	0.130	-	3.30	-	-
E3	0.030	-	0.76	-	7
e	0.050 BSC		1.27 BSC		-
k	0.008	0.015	0.20	0.38	2
L	0.250	0.370	6.35	9.40	-
Q	0.026	0.045	0.66	1.14	8
S1	0.00	-	0.00	-	6
M	-	0.0015	-	0.04	-
N	20		20		-

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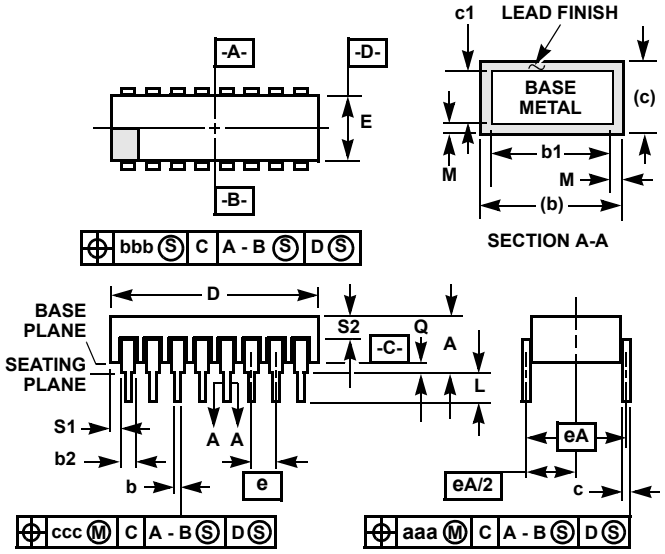
Notes:

1. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark. Alternately, a tab (dimension k) may be used to identify pin one.
2. If a pin one identification mark is used in addition to a tab, the limits of dimension k do not apply.
3. This dimension allows for off-center lid, meniscus, and glass overrun.
4. Dimensions b1 and c1 apply to lead base metal only. Dimension M applies to lead plating and finish thickness. The maximum limits of lead dimensions b and c or M shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.
5. N is the maximum number of terminal positions.
6. Measure dimension S1 at all four corners.
7. For bottom-brazed lead packages, no organic or polymeric materials shall be molded to the bottom of the package to cover the leads.
8. Dimension Q shall be measured at the point of exit (beyond the meniscus) of the lead from the body. Dimension Q minimum shall be reduced by 0.0015 inch (0.038mm) maximum when solder dip lead finish is applied.
9. Dimensioning and tolerancing per ANSI Y14.5M - 1982.
10. Controlling dimension: INCH.

6.2 Ceramic Dual-In-Line Metal Seal Packages (SBDIP)



D16.3 MIL-STD-1835 CDIP2-T16 (D-2, CONFIGURATION C)
16 LEAD CERAMIC DUAL-IN-LINE METAL SEAL PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.200	-	5.08	-
b	0.014	0.026	0.36	0.66	2
b1	0.014	0.023	0.36	0.58	3
b2	0.045	0.065	1.14	1.65	-
b3	0.023	0.045	0.58	1.14	4
c	0.008	0.018	0.20	0.46	2
c1	0.008	0.015	0.20	0.38	3
D	-	0.840	-	21.34	-
E	0.220	0.310	5.59	7.87	-
e	0.100 BSC		2.54 BSC		-
eA	0.300 BSC		7.62 BSC		-
eA/2	0.150 BSC		3.81 BSC		-
L	0.125	0.200	3.18	5.08	-
Q	0.015	0.060	0.38	1.52	5
S1	0.005	-	0.13	-	6
S2	0.005	-	0.13	-	7
α	90^o	105^o	90^o	105^o	-
aaa	-	0.015	-	0.38	-
bbb	-	0.030	-	0.76	-
ccc	-	0.010	-	0.25	-
M	-	0.0015	-	0.038	2
N	16		16		8

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Notes:

1. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark.
2. The maximum limits of lead dimensions b and c or M shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.
3. Dimensions b1 and c1 apply to lead base metal only. Dimension M applies to lead plating and finish thickness.
4. Corner leads (1, N, N/2, and N/2+1) may be configured with a partial lead paddle. For this configuration dimension b3 replaces dimension b2.
5. Dimension Q shall be measured from the seating plane to the base plane.
6. Measure dimension S1 at all four corners.
7. Measure dimension S2 from the top of the ceramic body to the nearest metallization or lead.
8. N is the maximum number of terminal positions.
9. Braze fillets shall be concave.
10. Dimensioning and tolerancing per ANSI Y14.5M - 1982.
11. Controlling dimension: INCH.

For the most recent package outline drawing, see D16.3.

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