White Paper

Taking Advantage of GaN in Small Satellite "New Space" Applications

Kiran Bernard, Applications Engineer, Industrial Analog & Power Group, Renesas Electronics Corp.

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Abstract

The "New Space" movement aims to take a more cost-effective approach for Low Earth Orbit (LEO) missions. In the past, satellite payloads ensured reliability by building redundancy into a single system to ensure that a given system could last 10 to 20 years. The New Space method is to achieve redundancy on the system level where they build numerous satellites with the expectation that when one satellite goes down, there are many others to take its place. The expected lifetime for satellites in LEO is about three to five years, significantly lower than the 10- to 20-year requirements of a Geostationary Orbit (GEO). While traditional space applications are usually several generations behind in technology compared to the commercial electronics industry, the New Space movement allows manufacturers to adopt newer technology previously unheard of in space. Gallium Nitride is one such technology, and its adoption in the power electronics space market has been slowed down due to the previous lack of drivers. With enhancement mode Gallium Nitride (GaN) FET availability, and now a radiation tolerant PWM controller and GaN FET driver, GaN deployment in power management applications can be realized. Substantial improvements in board space savings and power efficiency are now realities with these products due to GaN FET best-in-class gate charge performance and higher switching frequency capability. Further GaN FET performance and GaN FET driver solution details will be discussed in this paper.

GaN FETs – Ideal for Powering Small Satellites

There are several characteristics of GaN FETs that make them attractive for use in power supplies in satellites. In this paper, we will explore the physical attributes (inherent radiation tolerance and small die size), electrical characteristics (such as no parasitic p-n diode, fast switching), and power system advantages (increased efficiency and smaller total size).

In contrast to silicon MOSFETs, GaN FETs do not have a gate oxide layer and, thus, gamma radiation does not form traps (holes) to form in a gate oxide layer. GaN FETs also perform well in single-event effects (SEE) testing [1].

Figure 1 shows the structure of a GaN FET. The starting point is a standard silicon wafer. GaN and other materials are added on top, as shown in Figure 1. Notice that this GaN FET is a lateral device; current flow is horizontal through the GaN 2-dimensional electron gas (as shown by "-" in the diagram).

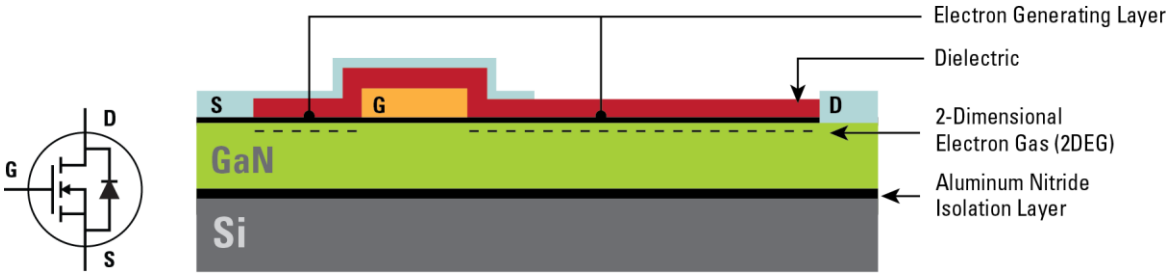

***Figure 1** – EPC's GaN Power Transistor Structure*

GaN is a wide bandgap material. Compared with silicon, the separation between the drain and source can, in theory, be a factor of 10 smaller. For the same RDSON, the width of the channel can be much narrower, in part due to the much shorter length. While silicon MOSFETs are very close to their theoretical limit, GaN FETs have room for further improvement; see Figure 2. In addition, for satellite applications, converting standard-production MOSFETs to space-grade MOSFETs causes a performance degradation versus the inherent ability of GaN FETs to meet space applications requirements [2].

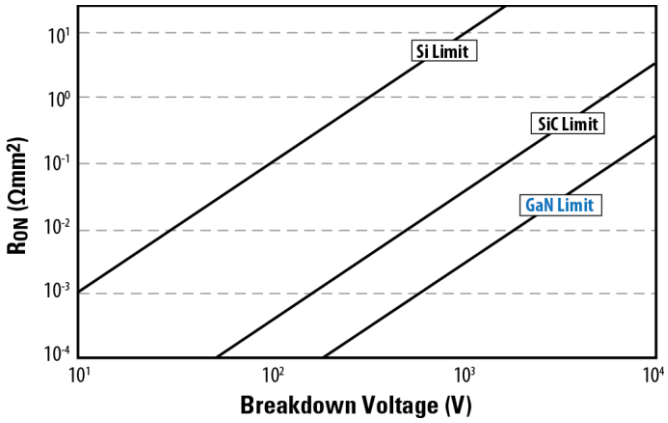

***Figure 2** – Resistance vs. breakdown voltage*

The smaller die size of a GaN FET versus a silicon MOSFET leads to performance improvements in switching power applications. Parasitics such as output capacitance and layout inductance are reduced. This leads to reduced switching losses and/or higher frequency operation with the same loss.

GaN FETs do not have a parasitic p-n diode. This is convenient in that there is no reverse recovery. Reverse recovery not only causes a longer dead time to recover the diode charge, it also is a function of several factors, such as temperature, current, and time the diode conducts. The question comes up: if GaN FETs do not have this element, do they conduct in the reverse direction (from source to drain) when the gate is "off" (Vgs = 0V)? Yes, GaN FETs do conduct in the reverse direction, using the same channel they use in the forward direction (not a parasitic element). The voltage drop of this conduction is greater than the drop of a diode; however, total loss can be minimized by using a very short dead time. Due to no reverse recovery, a dead time in the order of 5 to 15 ns can be used. In addition, if desired, an optional parallel Schottky diode can be used around a GaN FET (typically a small diode).

Switching Power Supply Applications

GaN FETs allow power supply designers to further optimize their designs. Advantages for the total power supply include: size, weight, efficiency, EMI, and potentially, fewer voltages and higher loop bandwidth.

Size and Weight: The fast switching and reduced parasitics lead to reduced losses for each switching cycle. The power supply designer can choose how to use this advantage: either raise the frequency, or increase the efficiency, or a balance of both (higher frequency and simultaneous higher efficiency). While GaN FETs themselves are smaller than equivalent MOSFETs, especially for satellite applications, a large benefit is for the size and weight of the overall power supply. Increased efficiency can result in reduced size/weight of heat sinking, as well as a reduced draw from the power source. Increased frequency can result in smaller inductors and capacitors, and for inductors, a reduced value of inductance may result in lower copper losses.

Bandwidth: Due to the ability to efficiently raise the switching frequency, the speed of the feedback loop can be made faster if also desired. The advantages of faster transient response include the possibility of reducing the size of the output capacitance because the power supply would have the ability to respond quicker to a load change and, thus, not need as much energy from the output capacitors to ride out the effect of the transient.

EMI: Increasing frequency and switching speed may seem to increase the issue of EMI, but GaN can have advantages here. Reduced parasitics mean less energy stored and released in these parasitic elements each switching cycle. Due to smaller size, board layout can be improved to reduce the loop inductance. Below is an example switching waveform taken from a power supply half-bridge evaluation board [3]. Note that even though this buck converter has fast rise and fall times, the voltage overshoot is low due to the optimized layout.

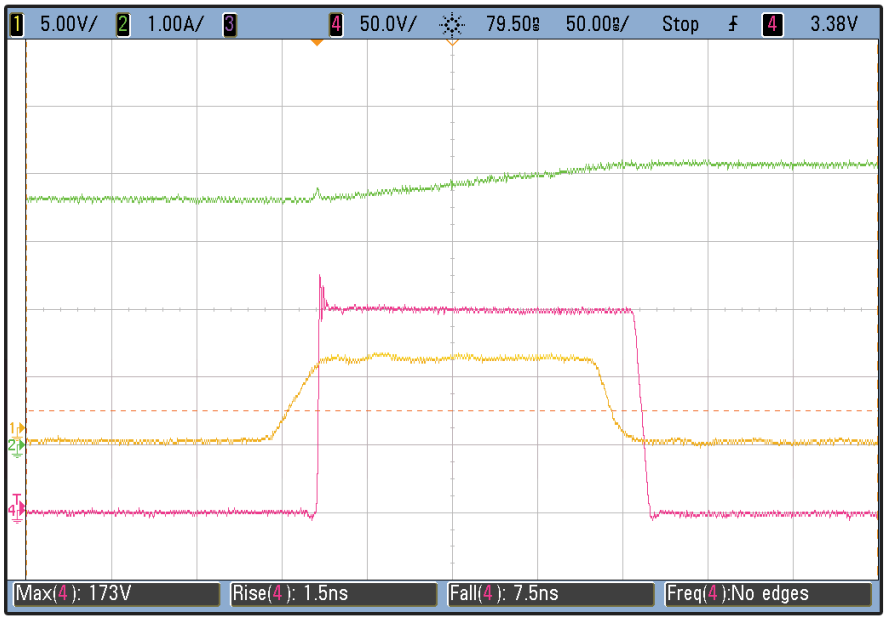

***Figure 3** – Waveforms for 150V_{IN} to 5V_{OUT} @ 4A (200kHz) Buck Convertor.*

CH1: VPWM Input Voltage
CH2: Inductor Current
CH4: V_{OUT} Switch Node Voltage

Gate Driver

To use GaN FETs to their full advantage, a specialized gate driver is needed: fast and regulated to the ideal drive voltage. The maximum gate voltage allowed is 6V, and most GaN FET drivers for commercial-grade applications use 5V as the drive voltage; however, for satellite applications, increased voltage margins are often required. The ideal gate drive voltage for these applications is 4.5V. This voltage has minimal impact on R_{DSON} versus a 5V gate drive. Using a drive voltage less than 4.5V nominal could, in a worst-case situation, cause too much increase in R_{DSON}. The curves in GaN data sheets are for typical devices and, thus, should not be interpreted as "a nominal gate drive voltage of 4V or less is a good choice."

Most FET controllers and drivers on the market today provide drive voltages in excess of 10V, which would damage the gates of GaN FETs. Having a driver that can level shift MOSFET voltage levels down to a 4.5V gate drive would be ideal to take advantage of the readily available PWM controllers on the market. There are two important factors to consider when considering a driver: 1) Does it have a well-regulated gate drive when switching? 2) How does it ensure the GaN FET will remain off when it should?

A well-regulated gate drive will maintain the gate voltage regardless of its supply line and output load variations. The nature of a driver is such that it needs to be able to provide amps of current within a short time repeatedly. This is usually achieved by tuning the compensation of the internal regulator for a given output capacitance. As this is usually taken care of by the IC manufacturer, the real challenge here is dealing with any stray inductance in the line between this output capacitance and the gate of the GaN FET. Amps of current in short periods of time result in large voltage transients that can be damaging to its gate. To get around this, we first ensure that the copper trace between the driver's output and the gate of the FET is as short as it can possibly be. Figure 4 shows an example of an optimized layout for a low side application:

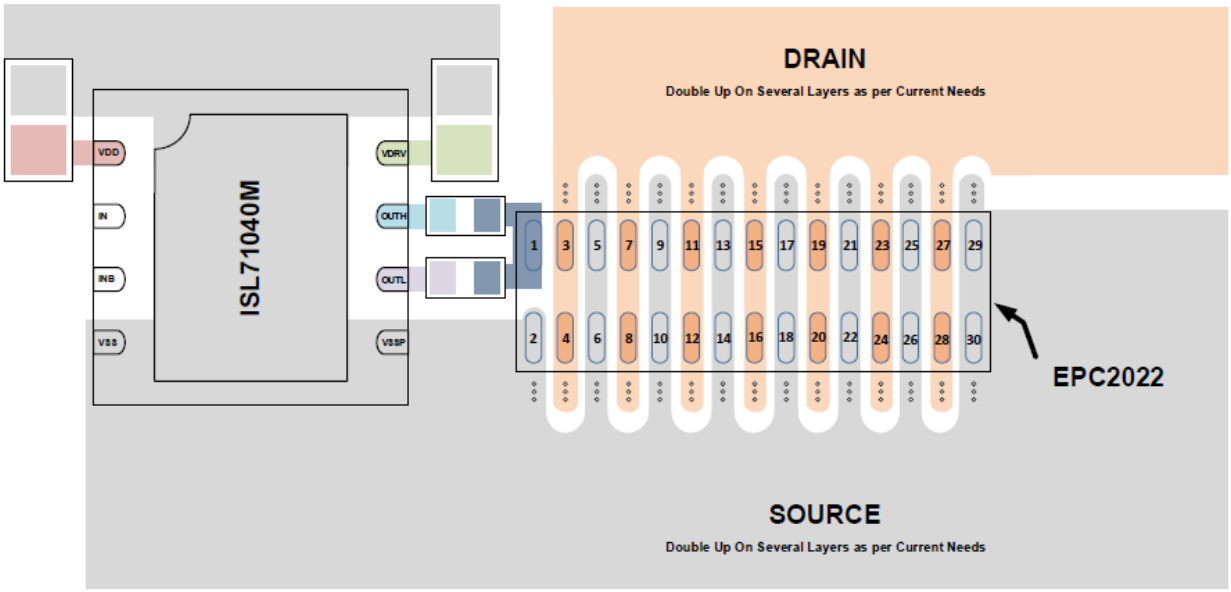

Figure 4 *– Optimized layout for minimizing inductance in the gate drive loop; the gate loop is as thick and short as it can be. The path to minimize is from VDRV (green) through OUTH (blue) to the Gate (dark blue) and back down to VSSP (grey) via OUTL (purple).*

The next task is to ensure that the gate return loop's inductance is also minimized. In the example above, the gate return (Substrate) is merged with the source plane to achieve this. Once the layout is taken into account, if there are still undesirable voltage spikes on the gate waveform, the gate resistors can be increased to compensate. It is also important to make sure that the driver has a fail-safe built in that will turn off the FET

when, or if, something goes wrong. If the inputs somehow are no longer driven, they should settle in a state that shuts off the FET. Another case to keep the switch off is when the gate drive voltage is not high enough to drive the GaN with its optimal R_{DSON}.

Apart from the technicalities that encompass designing a robust PWM controller and low side gate driver, designing for satellite systems poses some unique hurdles to overcome. For satellites to function as intended in orbit, its components need to maintain proper operation with prolonged exposure to Low Dose Rate (LDR) Total Ionizing Dose (TID), as well as be able to deal with interactions with ionized particles (such as heavy ions) in space. Having a PWM controller and GaN FET driver that don't flip states when a heavy ion deposits a charge on a junction or have its device threshold shift with LDR TID is something that must be mitigated in the IC design and process design phase. Here are some graphs that show what a driver can do when it's designed from the ground up for space (as opposed to a commercial up-screened IC).

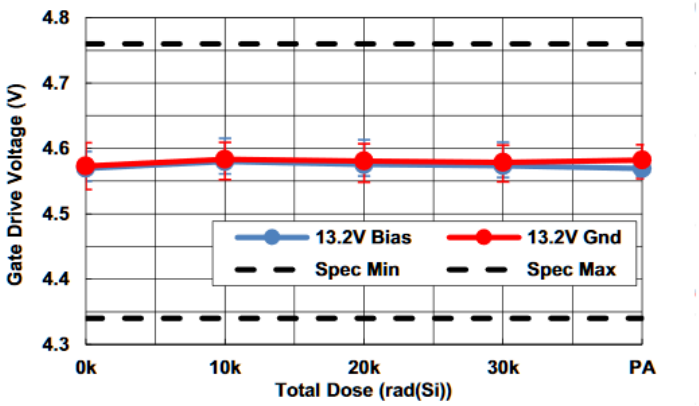

***Figure 5** – ISL71040M Gate Drive Voltage vs. Low Dose Rate (<10 mrad(Si)/s)*

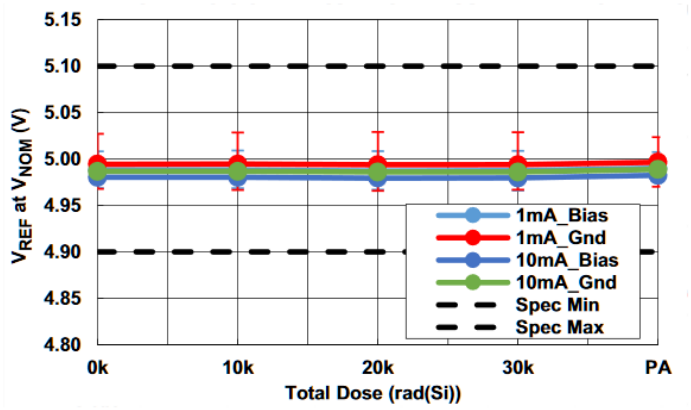

***Figure 6** – ISL71043M Overall Accuracy vs. Low Dose Rate (<10 mrad(Si)/s)*

The PWM controller that interfaces with the GaN FET driver needs to perform well under heavy ions. It is often tempting to adopt parts from the commercial world and up-screen devices due to the initial upfront cost, but unless the device was designed for space applications in mind, its performance will be severely diminished at the very least, or non-functional. Here is an example of a commercial switching voltage regulator with a 2V output that was exposed to heavy ions:

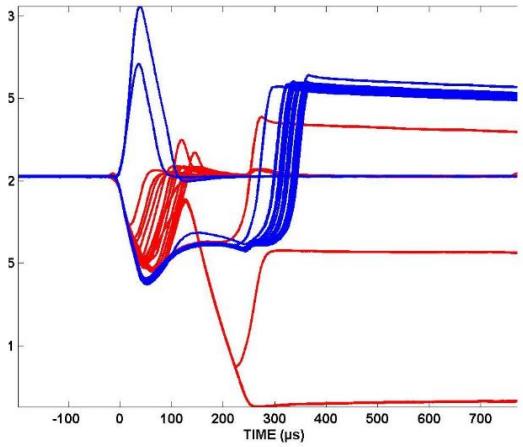

***Figure 7** – SET response of ISL85410 exposed to a LET = 43 MeV•cm2/mg at 25°C.*

In some cases, the output settled back to 2V after an ion strike, but in most cases, it completely shut down or started regulating some other voltage. While the former could be fixed with a simple power cycle, the latter can cause serious harm to the payload. Here's an example of a controller that works well under heavy ions:

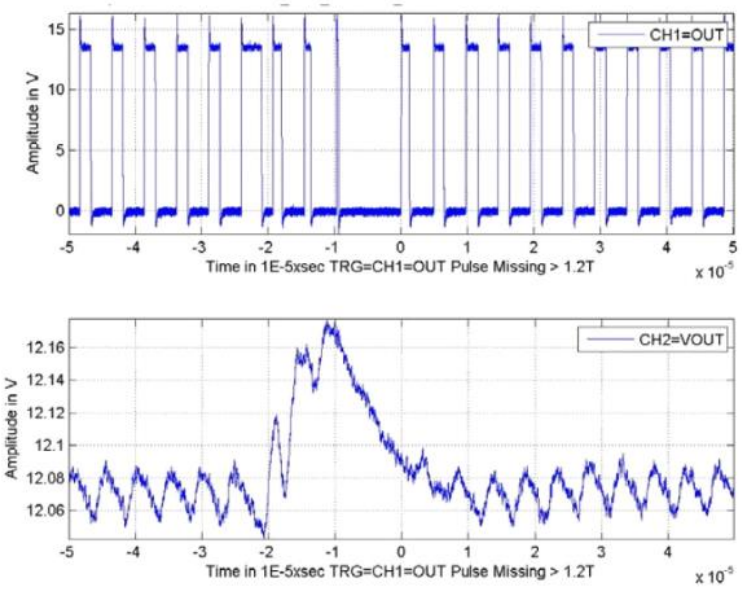

***Figure 8** – Example of a positive VOUT transient with the ISL71043M exposed to LET=43MeV•cm2/mg at 25°C.*

Figure shows that the controller experiences an ion strike that results in a slightly enlarged LX pulse and is quickly corrected by the feedback loop.

For the ISL71040M at an LET of 43 MeV•cm^2/mg, there were no Single Event Transients recorded with a static input, and for a dynamic input at 500kHz where SETs were defined as a ±20ns perturbation in pulse width, it had a very small cross section of ≤1.7x10^{-6}cm^2.

Conclusion

GaN FETs are a very good fit for satellite applications, but require a good gate driver to realize their full potential. Together, they allow more efficient switching, higher frequency operation, reduced gate drive voltage, and smaller solution sizes compared to the traditional silicon counter parts.

Footnotes:

[1] Alex Lidow et al, GaN Transistors for Efficient Power Conversion, Wiley, 2015, p. 172-178.

[2] HEMTs In Space - A New Take On Rad Hardness, Compound Semiconductor, https://compoundsemiconductor.net/article/99757-HEMTs-in-space-a-new-take-on-rad-hardness.html

[3] EPC9014 Quick Start Guide, EPC, page 2 Figure 4.