Space Grade Power Solution for the Xilinx® XQRKU060 FPGA

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Abstract

The trend with FPGAs follows the rest of the semiconductor market where the goal is to keep moving to the next smallest process node. Moving to smaller process nodes generally mean better efficiency and smaller transistors which translate to more processing power for a given die area. From a power management perspective, smaller nodes mean lower core voltages that require more current with margins that keep getting tighter. In the space industry, engineers tend to lean towards power solutions that are more risk adverse and thus apply margins on top of margins to ensure staying within the operating range of the FPGA. This poses a unique challenge for power electronics in that exceeding these tight voltage margins can lead to reliability concerns for the FPGA itself. This paper discusses the power requirements of the Xilinx XQRKU060 FPGA and how Renesas' Intersil family of high reliability products can be used to develop a best-in-class power solution.

Introduction

The XQRKU060 is a high-performance monolithic FPGA that has high DSP and block RAM-to-logic ratios and integrated next generation transceivers. It's developed on Xilinx's 20nm UltraScale process and features Single Event Upset (SEU) mitigated configuration memory and a block RAM design that has built-in Error Detection and Correction (EDAC). It uses a considerable number of patented techniques that reduce the overall SEU cross-section which is key tooperating in a heavy ion prone area.

The XQRKU060 requires a complex power solution with multiple low voltage supply rails with higher operating currents and needs to meet power sequencing requirements in order to avoid high inrush currents. In the satellite industry there's a necessity to improve Size, Weight and Power (SWaP) without sacrificing reliability and space qualifications. Renesas' broad portfolio of power management products can be used to create an efficient, smaller and light-weight power solution that can meet and exceed the demands of today's radiation hardened FPGAs, ASICs and microprocessors.

XQRKU060 Power Supply Requirements

Power Supply Rails

When it comes to developing a power solution for an FPGA, it's important to consider all the other devices that interact with it. As you can see in Figure 1, there's typically interface devices, DDR, boot memory and even a housekeeping MCU. These devices need radiation hardened power solutions and need to be sequenced such that they are powered and ready when the FPGA needs to communicate with them.

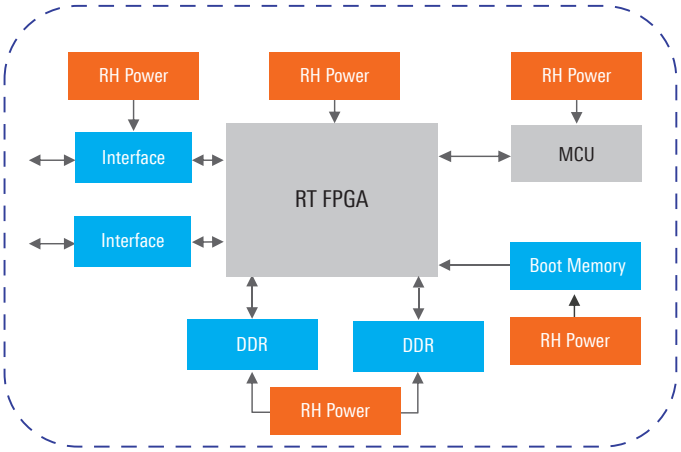

Figure 1: High level block diagram of a FPGA based system

Recommended Operating Conditions

Table 1 summarizes the recommended operating voltages. This information was taken from the XQRKU060 FPGA Datasheet[2]. To optimize the design, the typical operating points from the following table is determined using Xilinx's Power Estimator (XPE) tool.

Symbol	Description	Min	Typ	Max	Units
FPGA Logic					
VCCINT	Internal supply voltage	Typ – 4%	Use XPE	Typ + 4%	V
VCCBRAM	Block RAM supply voltage	Typ – 3%	Use XPE	Typ + 3%	V
VCCAUX	Auxiliary supply voltage	Typ – 3%	Use XPE	Typ + 3%	V
VCCAUX_IO	Auxiliary I/O supply voltage	Typ – 3%	Use XPE	Typ + 3%	V
VCCO	I/O supply voltage	Typ – 4%	Use XPE	Typ + 4%	V
VIN	I/O input voltage	–0.2	–	VCCO + 0.2	V
	I/O input voltage (when VCCO = 3.3V) for VREF and differential I/O standards except TMDS_33	–	–	2.625	V
GTH Transceivers					
VMGTAVCC	Analog supply voltage for the GTH transceivers	Typ – 2%	Use XPE	Typ + 2%	V
VMGTAVTT	Analog supply voltage for the GTH transmitter and receiver termination circuits	Typ – 2%	Use XPE	Typ + 2%	V
VMGTAVTTRCAL	Analog supply voltage for the resistor calibration circuit of the GTH transceiver columns	Typ – 2%	Use XPE	Typ + 2%	V
VMGTVCCAUX	Auxiliary analog QPLL voltage supply for the transceivers	Typ – 2%	Use XPE	Typ + 2%	V
SYSMON					
VCCADC	SYSMON supply relative to GNDADC	Typ – 3%	Use XPE	Typ + 5%	V
VREFP	SYSMON externally supplied reference voltage relative to VREFN	Typ – 4%	1.25	Typ + 4%	V
VBATT	Battery voltage	1	–	1.89	V

Power Sequencing Requirements

There are over half a dozen rails that need to be sequenced and each of them have its own sequencing order during start-up, shutdown, and fault conditions. The rails specific to the XQRKU060 can be broken out into 3 groups, shown in Figure 2 where the first 2 groups require sequencing, and all remaining rails that don't need sequencing fall into group 3.

Group 1	Group 2	Group 3
• V_{CCINT}	• V_{CCINT}	• V_{CCADC}
• V_{CCBRAM}	• $V_{MGTAVCC}$	• V_{REF}
• $V_{CCAUX/\_IO}$	• $V_{MGTAVTT}$	• $VM_{GTVCCAUX}$
• V_{CCO}		

Figure 2: XQRKU060 rails broken out based on sequencing requirements

Group 1 contains the core rails for the XQRKU060, group 2 is for the multi gigabit transceivers and group 3 is everything else. To implement sequencing, the easiest way is to cascade regulators from their PGOOD pins to the subsequent regulators ENABLE pin as in Figure 3:

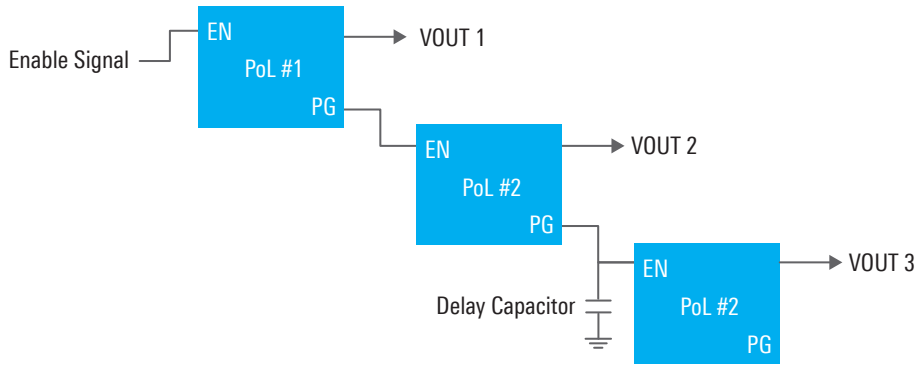

Figure 3: Power Supply Sequencing using PGOOD to ENABLE connections

This setup is extremely simple to implement and is very cost efficient. However, it does not provide power down sequencing (which is just as critical as the power up sequence) or fault detection. Another thing to consider is the delay time associated with the PGOOD thresholds. Figure 4 shows that the delay can change by a factor of 2 across the full military temperature range.

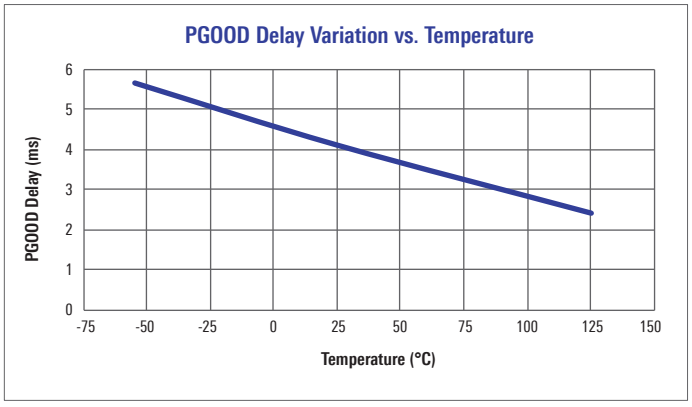

Figure 4: PGOOD Delay versus Temperature

A better way to implement sequencing is through an event-based sequencer like the Intersil ISL70321SEH. It's very simple to implement both power up and down sequencing with built in fault detection. The ISL70321 features a precision voltage reference used for monitoring, adjustable rising/falling delays and adjustable PGOOD timers. The ISL70321SEH can be infinitely cascaded to sequence more than 4 rails and outputs a DONE and Fault signal that can be used as indicators for system management software.

XQRKU060 FPGA Development Kit

Development Kit Overview

Figure 5 shows the block diagram of the power solution for the XQRKU060. A total of nine regulators are used to generate all the necessary rails to power the digital loads. The main input rail is 5V DC which is controlled by an ON/OFF switch. The main 5V DC bus is fed to the sequencers and the regulators that generate the 0.95V, 1.35V/0.675V, 1.8V, 2.5V and 3.3V voltage rails. 0.95V is used to power the core rail for the FPGA while the 2.5V is an intermediate bus that is distributed around the board and used as inputs to other regulators for further conversion.

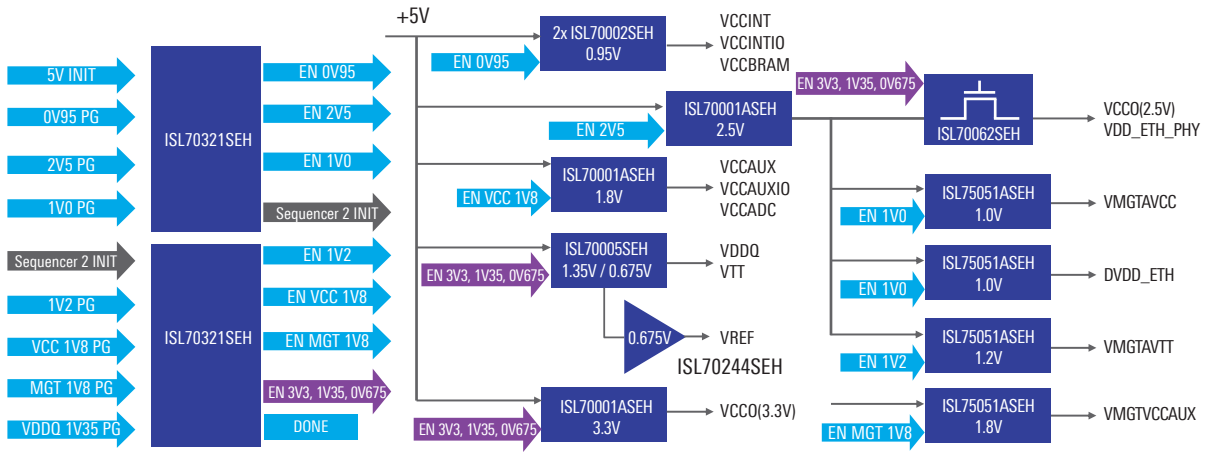

Figure 5: Power Tree for the XQRKU060

The "5V INIT" signal starts the power sequence and the voltage outputs from the respective regulators are monitored to start the next regulator in sequence. If at any point a regulator fails to come up within the specified PGOOD timer, the entire system is shut down and the fault pin $\overline{KILL}$ goes low to indicate an error has occurred. Provided the power up sequence has successfully completed, the DONE signal from the ISL70321SEH goes high. The monitoring and control function of the ISL70321SEH can be summarized as follows:

- The 5V DC bus drives the UP pin of the ISL70321SEH. The power up sequence is initiated when the 5V bus reaches 4.3V.
- When the 5V bus is up, the core rail (0.95V) for the FPGA are enabled for the VCCINT, VCCINTIO and VCCBRAM.
- When the 0.95V rail is above 0.8V the 2.5V intermediate bus voltage is enabled.
- When the 2.5V rail is above 2.09V, the 1.0V rails for VMGTAVCC and DVDD_ETH are enabled simultaneously.
- When the 1.0V rail is above 0.87V, the 1.2V rail for MGTAVTT is enabled.
- When the 1.2V rail is up, the 1.8V rails for the MGTVCCAUX, VCCAUX, VCCAUXIO and VCCADC are enabled.
- The last rails to come up are the VDDQ/VTT/VREF, VCCO(2.5V), VCCO(3.3V) and VDD_ETH_PHY.

Table 2 summarizes the part number, description, and operating conditions of the POLs and LDOs used in the reference design.

Part Number	Description	Input	Output Name	Output	Load Capable
ISL70002SEH	Radiation Hardened and SEE Hardened 22A Synchronous Buck Regulator with Current Sharing	5V	VCCINT VCCINTIO VCCBRAM	0.95V	38A
ISL70001ASEH	Radiation Hardened and SEE Hardened 6A Synchronous Buck Regulator	5V	IBV VCCO(2.5V) VDD_ETH_PHY	2.5V	6A
ISL70001ASEH	Radiation Hardened and SEE Hardened 6A Synchronous Buck Regulator	5V	VCCAUX VCCAUXIO VCCADC	1.8V	6A
ISL70001ASEH	Radiation Hardened and SEE Hardened 6A Synchronous Buck Regulator	5V	VCCO(3.3V)	3.3V	6A
ISL70005SEH	Radiation Hardened Dual Output Point-of-Load, Integrated Synchronous Buck and Low Dropout Regulator	5V 1.35V	VDDQ VTT	1.35V 0.675V	3A ±1A
ISL70244SEH	Radiation Hardened 19MHz Rail-to-Rail I/O Op Amp with Slew Rate Enhancement	0.675V	DDR VREF	0.675	-
ISL75051ASEH	3A, Radiation Hardened, Positive, Ultra-Low Dropout Regulator	2.5V	VMGTAVCC	1.0V	3A
ISL75051ASEH	3A, Radiation Hardened, Positive, Ultra-Low Dropout Regulator	2.5V	DVDD_ETH	1.0V	3A
ISL75051ASEH	3A, Radiation Hardened, Positive, Ultra-Low Dropout Regulator	2.5V	VMGTAVTT	1.2V	3A
ISL75051ASEH	3A, Radiation Hardened, Positive, Ultra-Low Dropout Regulator	2.5V	VMGTVCCAUX	1.8V	3A

Table 2: Radiation Hardened Power Management IC Configuration

ISLKU060DEMO1Z Reference Board

Renesas, in collaboration with Ibeos, developed a power supply solution for the XQRKU060 called the ISLKU060DEMO1Z. It provides customers a fully validated radiation hardened power solution that they can use in their designs.

The schematics and Gerber files for the reference design are available online on the ISLKU060DEMO1Z product page. Designers can use these files as a starting point or use them directly in their own designs. A link to the board's landing page can be found at the end of this document. Figure 9 and Figure 10 are images that show the top and bottom views of the reference design.

Figure 6 Renesas' Intersil – KU060 Reference Board (bottom

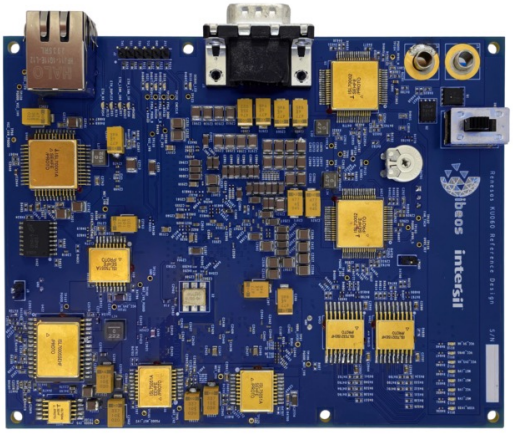

Figure 7 Renesas' Intersil - RTG4 Reference Board (top)

To verify functionality of the boards, the startup waveform was captured and then bitstream files were loaded into the FPGA. For the power supply sequence, correct supply sequence is as follows:

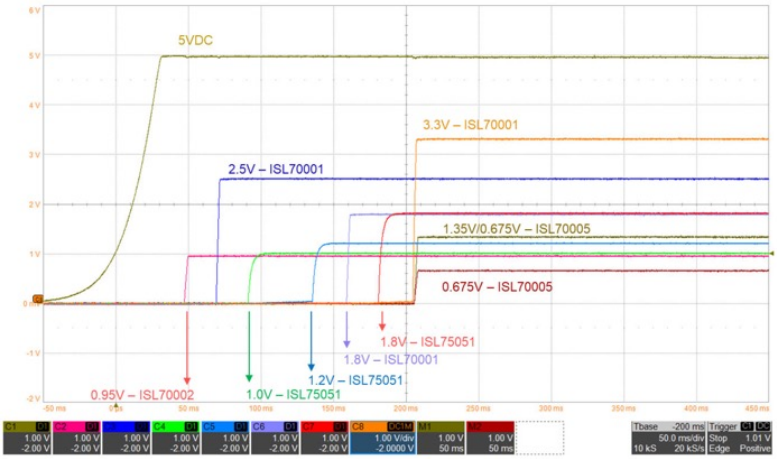

Figure 8: Start up sequence of the ISLKU060DEMO1Z

For the FPGA's functionality, 2 bitstream files (provided by Ibeos) were used to exercise the DDR3 memory and the RS485 communication. The first bitstream outputs the following 20 bytes of data out on the RS485 port which are captured by an oscilloscope.

Expected Data:
{0xDE, 0xAD, 0xBE, 0xEF, 0x00, 0x01, 0x02, 0x04, 0x08, 0x0C,0x10, 0x20, 0x40, 0x80, 0xC0, 0xFF, 0xFF, 0xFF, 0xFF, 0xFF};

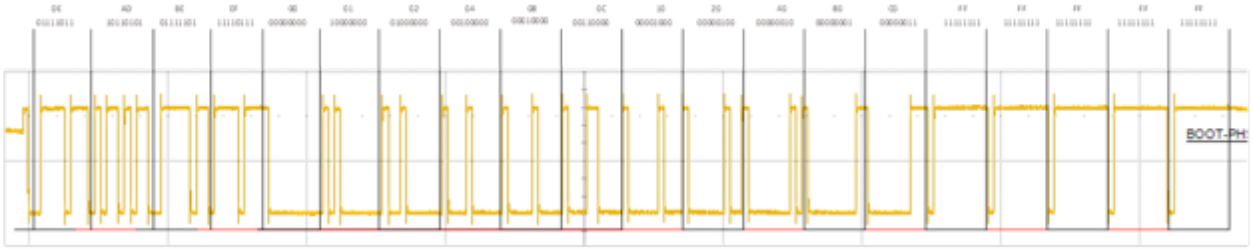

Figure 9: First program's RS485 output

The second bitstream exercises both DDR3 and RS485. Its output is much more verbose and thus decoding the output with a scope is not reasonable. A python script on the host PC was used to decode the output to verify successful execution. Successful operation is determined by getting the same 20 bytes of data shown in Figure 9.

Conclusion

As the satellite industry moves towards smaller process nodes, the core voltages for high performance FPGAs will trend lower and lower with tighter regulation limits. Power solutions for such FPGAs must meet the tight regulation limits while still being robust and reliable. This paper discusses how Renesas's Intersil space grade power management and analog portfolio can provide a highly reliable and efficient power solution for the XQRKU060.

The ISLKU060DEMO1Z is a complete development platform that utilizes all rad hard ICs to implement a worry-free power supply reference design. All the necessary design files are available on the ISLKU060DEMO1Z product landing page which simplifies the power supply design process. This makes it easy for engineers to easily prototype their designs on hardware that is as close to flight grade as possible which shortens the development cycle.

Next Steps

- Visit the ISLKU060DEMO1Z web page
- Learn more about the ISLKU060DEMO1Z
- Learn more about the ISL70001ASEH
- Learn more about the ISL75051ASEH
- Learn more about the ISL70005SEH
- Learn more about the ISL70321SEH
- Learn more about the ISL70244SEH
- Learn more about the ISL70062SEH

References

1. RT Kintex Ultrascale FPGA Product Overview
2. XQRKU060 FPGA Datasheet, DS882 Datasheet Revision 1.2

Doc number: R34WP0004EU0000