Battery Management

Battery Protection Using Low-Side FETs Controlled by GPIOs

Abstract

In an MCU plus battery front end (BFE) controlled battery pack, GPIOs may operate as an alternate protection FET control path where low-side FETs are preferred. Use cases include (1) extending the upper voltage range of battery IC to higher voltages by shutting down the high-side charge pumps and (2) repurposing a high-side solution to a low-side solution with minimal BOM changes. A solution with the ISL94216 device acts as a model for a low-side GPIO controlled solution; however, in this white paper, the techniques and principles for low-side GPIO control generally apply to battery ICs with GPIOs (such as the ISL94216) and for battery pack MCUs with GPIOs (such as the RL78). The ISL94216 BFE simplifies the adoption of low-side control considerably by offering bit settings to swap the control logic from the high-side FET pins to the built-in GPIOs.

Introduction

BFE devices (such as the ISL94216 or ISL94212) periodically check battery status and the operating environment to prevent catastrophic failures, so when the devices are combined with an MCU, they optimize battery life. For managing battery pack state, an internal analog-to-digital converter (ADC) provides accurate monitoring of pack parameters, typically cell voltage, temperature, and load current. Also, a BFE typically supports communication protocols, and this allows customers to connect an MCU in a battery management solution to control GPIOs or monitor the battery status.

The ISL94216 is a 16-cell BFE IC, an essential component of any battery management system (BMS), and the ISL94216 is designed for both high-side and low-side FET control. The ISL94216 datasheet focuses on high-side control; however, through a simple configuration setting, the ISL94216 seamlessly supports low-side power FET control while retaining all control logic, firmware, and peripheral support circuitry. This white paper provides a guide for using the ISL94216 in low-side battery applications, where the low-side control brings the added benefit of extending the maximum voltage to 67.2V. A low-side configuration with a disabled charge pump allows the ISL94216 to operate at a higher maximum pack voltage.

The maximum voltage for standard lithium-ion cells is ~4.2V. An operating maximum rating of 67.2V supports 16-cell series applications. Figure 1 shows the ISL94216 in a battery pack configured for a low-side application.

Figure 1. ISL94216 Example Configuration for Low-Side Power FET Control

The circuit in Figure 1 is tuned for low-power and performance. This white paper details several control options shown in the diagram.

Contents

A Functional Overview

The ISL94216 default configuration includes high-side FET control, and after a power-on reset (POR) or reset, the device reconfigures easily to low-side control by the MCU (as described in the following sections). The recommended low-side FET configuration, that is illustrated in Figure 1, operates as follows: It starts with the device in Low Power Mode, with no load or charger connected, and both the CFET and DFET are off. When a load is attached between the Pack+ and Pack- pins, the LDMON pin activates through the circuitry in Block 1 triggering the load present detect circuit and setting the ISL94216 Load PRESI bit (register 0x64), which wakes the ISL94216 and changes the mode to IDLE. The transition to IDLE mode signals the load detection to the MCU. There are various firmware implementation options to signal the MCU to enable gate control, and one of these options is to have the MCU use the signal to the FETSON pin. Next, the MCU enables the Gate Driver VREG shown in Block 4, through the EN_VREG signal. This regulator provides power to the gate drive voltage controlled by the FET Driver in Block 5. The FET Driver enables DFET when signaled from the ISL94216 through GPIO2. These blocks are detailed in the following sections.

Load Detection (1)

In high-side power FET configurations, the LDMON pin must be pulled below 1.2V for the LD PRESI bit to be set. In low-side applications, the PACK- pin is pulled towards PACK+ when a load is connected, the opposite polarity of the load detect circuitry. The circuitry in the white box (1) reverses the polarity so that a load is detectable for low-side power FET applications.

Using an NMOS with a resistor divider reverses the logic polarity of load detection. To connect to the NMOS drain, the circuit repurposes the ISL94216 load detection internal pull-up resistor. The circuit is designed to have a pull-down resistance of 1MΩ; as well, an R_{GS} resistance of 33kΩ and 1MΩ detects loads of 15kΩ or less. For charger detection, the ISL94216 relies on the MCU.

GPIO Setup for Low-Side Operation (2)

The ISL94216 is designed for both high-side and low-side FET control. An internal change from high-side to low-side FET control only requires a GPIO configuration setting. Low-side FET control uses the GPIO pins of the ISL94216. Set the GPIO configuration bits, 0x12.[5:4], to **Power FET Gate Drive Out** (B11). This setting connects GPIO2 to the DFET state and GPIO3 to the CFET state. These states are dependent on bits 0x24.1 DFET EN and 0x24.0 CFET EN (in datasheet sections "0x24.1 DFET EN" and "0x24.0 CFET EN") along with other settings and faults as described in the datasheet section "CFET and DFET Pins (50, 51)". The DFET and CFET states follow the same expected behavior of the DFET and CFET pins except that the state does not depend on the (disabled in low-side mode) charge pump; as a result, although the high-side DFET and CFET pins are off, the state can be **ON** (LOW) when the 0x24.7 CPMP EN bit (datasheet section "0x24.7 CPMP EN") is **0** and/or the 0x65.5 CPMP NRDY bit (datasheet section "0x65.5 CPMP NRDY") is **1**.

A Hi-Z pin status for pins GPIO2 and GPIO3 equates to DFET and/or CFET being disabled. While the device is in SHIP and LOW POWER modes, the DFET and CFET pins are in a HI-Z state. All faults that control the power FETs also control pins GPIO2 and GPIO3. For example, an open-wire detection automatically turns off the power FETs for a high-side application. For a low-side application, the power FET GPIO pins are set to a HI-Z state with an open-wire fault.

Error! Reference source not found. defines the logic state of the GPIO output pins (3, 2, 0) as a function of the GPIO1 input, the device Mode, and the internal DFET and CFET enable bits.

Table 1. GPIO Pins in FETs Out Mode

Internal State Variable			Input Pin	Output Pins			
Mode	DFET	CFET	FETs Off (GPIO1)	FETs On (GPIO0)	DFET (GPIO2)	CFET (GPIO3)	
SCAN or IDLE	OFF	OFF	LOW	LOW	HI-Z	HI-Z	
	OFF	ON	LOW	HI-Z	HI-Z	LOW	
	ON	OFF	LOW	HI-Z	LOW	HI-Z	
	ON	ON	LOW	HI-Z	LOW	LOW	
	X	X	HIGH	LOW	HI-Z	HI-Z	
LOW POWER or SHIP	X	X	X	HI-Z	HI-Z	Hi-Z	

GPIO1 is configured as a FETs Off digital input pin. The pin allows the MCU to turn off the power FETs without serial communication from the MCU to the device. If the logic input is high, both DFET and CFET GPIO pins, along with the high-side DFET and CFET pins (if enabled), turn off. If the logic input is low, the DFET and CFET states pass to GPIO2 and GPIO3. Before choosing this configuration, disable both CFET and DFET by setting their enable bits to **0**; next, write 0x3C to register 0x12.

GPIO0 is configured as a FETs ON digital output pin. The output of the pin is LOW when CFET and DFET are both off. It is high impedance when one or both CFET and DFET GPIO outputs are **ON**.

Further details are in the datasheet, see section "0x12.5:4 GPIO CONFIG".

MCU (3)

Just as in a high-side application, the ISL94216 is connected to an MCU to provide a full battery management solution. The MCU is responsible for register configuration, reading data registers, control override, and other features such as external communications. Ideal choices for functionality and cost for the MCU include the Renesas 16-bit RL78 family and 32-bit RX family. Typically, the ISL94216 provides a full front-end battery solution, so the MCU is selected without consideration for front-end functions. Most of the firmware that supports a high-side FET solution operates in a low-side FET application with only the prior-noted minor updates required to implement GPIO FET control.

V_{REG} for Power FET Driver (4)

The voltage regulator in Block 4 provides the gate drive voltages required by the CFET, DFET, and FET Driver. The regulator input is connected to V_{PACK} to prevent individual cell(s) from being loaded resulting in cell mismatches. The regulator powers the drive circuitry (for this example, with a regulated output of 12V using the ISL89411) that turns ON and OFF the power FETs. An alternative PMIC that can supply the MCU is the RAA212832, which is a programmable buck with two LDO outputs. The voltage regulator is activated through a signal from the MCU on either a load or charger detect.

Power FET Driver (5)

Block 5 consists of the ISL89411 dual FET driver that is designed for a gate voltage of 12V and an operating voltage between 4.5V and 19V. A Zener is connected to DRV2 to protect the driver output pin when a load is connected. This Zener should be selected with Zener voltage above the Max Battery Voltage. A series gate resistor (not shown) should be added to the CFET and DFET gate connections, and the gate resistor should be chosen with consideration to any rise/fall time requirements.

CFET and DFET Circuits (6)

Block 6 shows the MOSFETs along with the related drive and protection circuitry. The order of the CFET and DFET is reversed on the low side from the high-side configuration, with the CFET next to the pack pin (Pack- for low side). With the CFET at the Pack- terminal, the CFET may be exposed to higher voltages on a load connect; therefore, a Zener across the FETs gate-source, or other protection circuitry is necessary to ensure that the gate source voltage does not exceed the MOSFET maximum gate voltage rating.

Summary

GPIOs on the ISL94216 are configurable for low-side FET control with minimum effort to extend the battery front-end voltage operation. Depending on the requirements, alternative solutions using GPIOs are plausible; contact your local Renesas sales representative for more information.

Revision History

Revision	Date	Description
1.0	Nov.19.20	Initial release

IMPORTANT NOTICE AND DISCLAIMER

RENESAS ELECTRONICS CORPORATION AND ITS SUBSIDIARIES ("RENESAS") PROVIDES TECHNICAL SPECIFICATIONS AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for developers skilled in the art designing with Renesas products. You are solely responsible for (1) selecting the appropriate products for your application, (2) designing, validating, and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. Renesas grants you permission to use these resources only for development of an application that uses Renesas products. Other reproduction or use of these resources is strictly prohibited. No license is granted to any other Renesas intellectual property or to any third party intellectual property. Renesas disclaims responsibility for, and you will fully indemnify Renesas and its representatives against, any claims, damages, costs, losses, or liabilities arising out of your use of these resources. Renesas' products are provided only subject to Renesas' Terms and Conditions of Sale or other applicable terms agreed to in writing. No use of any Renesas resources expands or otherwise alters any applicable warranties or warranty disclaimers for these products.

(Rev.1.0 Mar 2020)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.

Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit:
www.renesas.com/contact/