

White Paper

How to Improve DC/DC Converter Performance with Phase Shifting Time Delay

November 2020

Abstract

In most step-down power conversions, where multiple output voltages are required to regulate off a single input source, the switching regulators can impose high input root mean square (RMS) current and noise when delivering point-of-load (POL) power to FPGAs, DSPs and microprocessors. To combat this, designers will typically implement high input filtering (at additional cost) to reduce conducted electromagnetic interference (EMI) and/or radiated EMI, and to control the higher system I^2R power losses.

Another technical challenge designers must deal with in systems employing audio amplifiers is “beat frequency”, which is the frequency difference between the power supply’s switching DC/DC converters. If the beat frequencies are between 100Hz and 23kHz, the audio amplifier will likely detect them and disrupt system performance.

This article examines how to synchronize multiple DC/DC buck regulators in a Master/Slave configuration using phase shift time delay. Phase shifting multiple converters prevents ON time overlapping and reduces RMS current, ripple and input capacitor requirements, which will improve system EMI and power efficiency. This approach also eliminates the need for high input filtering and addresses the problems associated with beat frequencies.

As you can see in Figure 1, converter 1 is the “Master”, which provides the set frequency for the rest of the “Slave” converters.

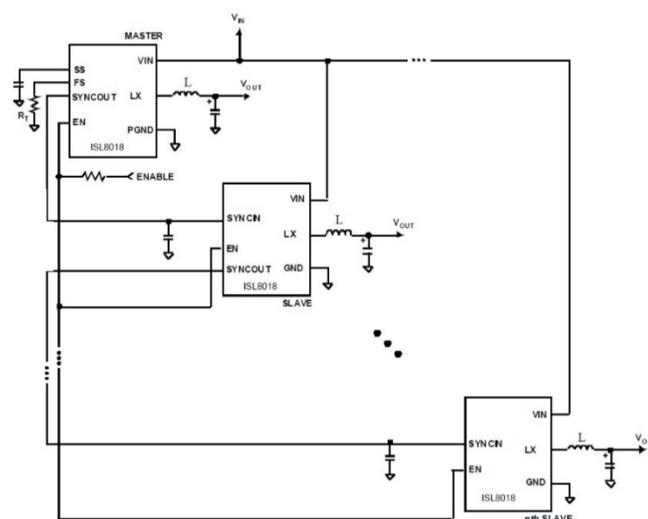


Figure 1: ISL8018 DC/DC converter application using a Master/Slave configuration

Synchronizing multiple DC/DC converter channels is easy and straight-forward but programming the phase shift can be a challenge. Let's look at a comparison of DC/DC converters configured in-phase and out-of-phase as shown in Figure 2. Both designs use a 3-phase method to provide 24A of output current. You can add more phases for higher current capability, if required. For both approaches, each converter is optimized to 8A. The configuration on the left is operating in-phase, while the design on the right shifted each phase approximately 120°. The three converters on the left will have a peak input ripple of 24A (three x 8A) or 12A RMS at 50% duty cycle. The three converters operating out-of-phase on the right run at 8A or 4.3 RMS at 50% duty cycle.

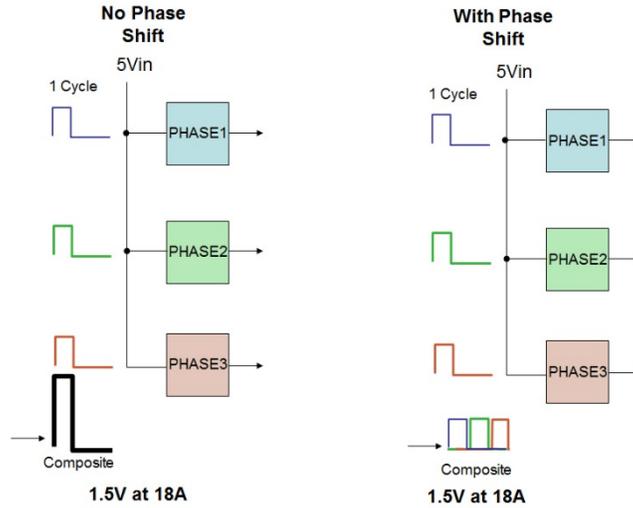


Figure 2: Comparison of 3-phase DC converters in-phase and out-of-phase

As previously mentioned, using phase shifting significantly reduces the input and output capacitors requirement. The RMS input current is governed by equation 1:

$$\Delta I_{in_rms}(n, D) = \left[\left[\left(D - \frac{k(n, D)}{n} \right) \cdot \left(\frac{k(n, D) + 1}{n} - D \right) \right] + \left(\frac{n}{12D^2} \right) \left[\frac{V_{OUT} \cdot (1 - D)}{L \cdot F_s \cdot I_{OUT}} \right]^2 \cdot \left[\frac{(k(n, D) + 1)^2}{\left(D - \frac{k(n, D)}{n} \right)^3 + k(n, D)^2 \cdot \left(\frac{k(n, D)}{n} - D \right)^3} \right] \right]^{1/2}$$

Where n is the number of phases, L is the output inductor, Fs is the switching frequency, and k(n,D)=floor(n*D), the floor function returns the greatest integer less than or equal to the input value.

Figure 3 shows the plot of $\Delta I_{IN_RMS}(n,D)$ vs. duty cycle.

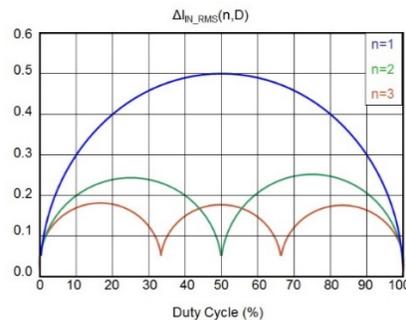


Figure 3: Plot of $\Delta I_{IN_RMS}(n,D)$ vs. duty cycle

In Table 1, we see the summarized performance result comparisons between three converters operating in-phase and three converters operating out-of-phase.

Parameter	In-Phase	Out-of-Phase
Number of Phases, n	3	3
RMS Input Current	10.8A	3.1
Input Voltage Ripple (10mΩ R _{ESR} capacitor)	240mV	80mV
Input Ripple Frequency	1MHz	3MHz

Table 1: Out-of-phase approach provides significant benefits over an in-phase design

A synchronous buck regulator, like the ISL8018, provides a simple, low cost method to implement out-of-phase operation. The SYNCOUT feature of the master switching regulator sources a current pulse, I_{SYNC} , starting at every clock cycle. The current source terminates and discharges to 0V after it reaches the 1V SYNCOUT voltage. The SYNCIN feature of the slave regulator's detection threshold is 0.9V. When each rising edge of SYNCIN reaches 0.9V, the ON pulse of its PHASE is triggered. Simply adding a small, inexpensive capacitor across SYNCIN to GROUND changes the SYNCOUT current source slew rate.

See Figure 4 for the Master/Slave circuit diagram, In Figure 5 you will see its logic implementation. The phase shift time (t in ns) is equal to $2.8 \cdot C_{PHASE}$ in pF.

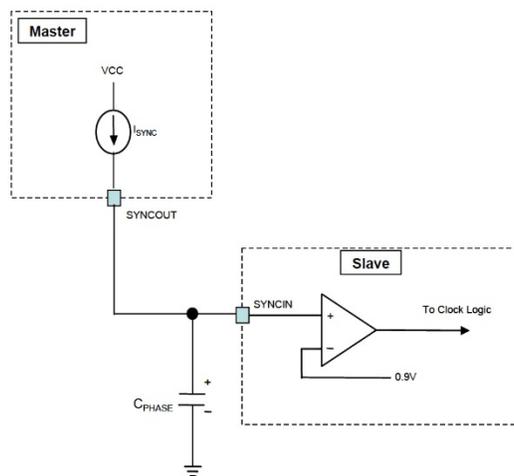


Figure 4: Master/Slave circuit implementation

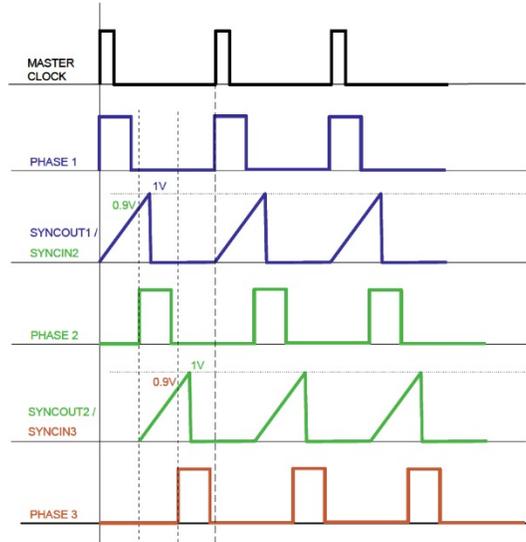


Figure 5: Master/Slave logic implementation

Implementing the current source is simple and requires only 70mil² die area. You can trim it to achieve $\pm 5\%$ tolerance. Likewise, the threshold of SYNCIN can be trimmed to $\pm 0.5\%$. The application capacitance is in the pF range, which only requires a low cost NPO or COG dielectric class ceramic capacitor, with a tight tolerance of $\pm 1\%$. Therefore, the phase shift tolerance is approximately 5.12%.

As previously mentioned, the ISL8018 can be synchronized from a Master or an external clock. This feature is necessary when multiple regulators operate in close proximity to one another. Figure 6 shows converters 1 and 2, which are operating with frequencies f_1 and f_2 , respectively. The input will see a “beat” frequency (f_b), which is the difference between f_1 and f_2 . This f_b will show up in GROUND if there is no isolation. The output may appear as seen in Figure 7 where the envelope is the “beat” frequency.

Usually, the beat frequency is very low, especially if same type of converter is used for multiple rails. This low will show up throughout the system. In computing, telecommunication, industrial or medical equipment that include audio, the system’s audio amplifier will most likely pick up the beat frequency noise. As previously mentioned, adding a common-mode or differential-mode noise filter will add cost to the system design.

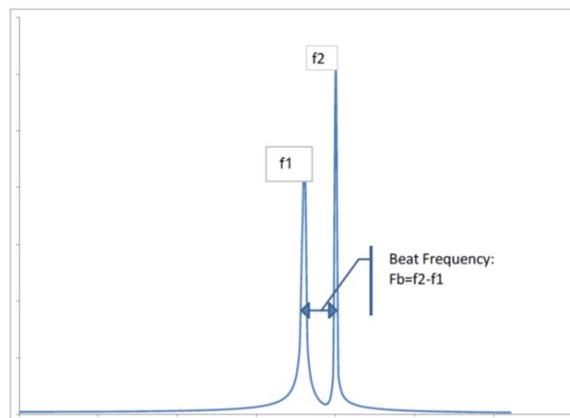


Figure 6: Frequency spectrum of the input source

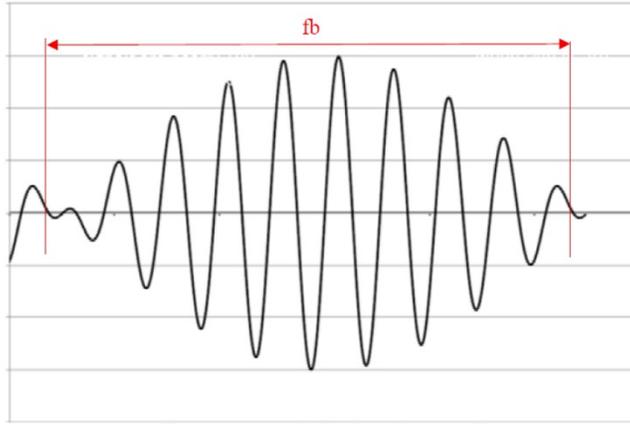


Figure 7: Ground ripple voltage noise

However, the SYNC feature of the ISL8018 DC/DC converter can solve the beat frequency problem by employing multiple converters operating with the same clock. Then f_b will equal 0Hz, thereby eliminating the beat frequency throughout the entire system.

Conclusion

DC/DC converters such as the ISL8018 can provide a low-cost solution to noise sensitive applications, especially those that include audio circuitry. Employing multiple POL DC/DC converters in a Master/Slave configuration using the phase shifting time delay approach helps designers optimize their power supply design by reducing RMS current, ripple and input capacitor requirements. Additionally, the ISL8016 is a 6A version of ISL8018 for lower current applications.

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