Controller Scalability Methods for Digital Point Of Load Converters

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***Abstract*— Unmodeled dynamics cause DC-DC controller design to be an iterative procedure where controller parameters are tuned and re-tuned to achieve the desired transient performance. Once the controller is designed any change of the output filter requires a new compensator design to guarantee stable operation. In this paper programmability of controller parameters in digital Point Of Load (POL) converters is exploited to investigate methods to scale an existing controller to accommodate variation of the resonant frequency of the LC filter, with the aim to eliminate the need for such iterative tuning. A new method to scale a compensator is then proposed to maintain bandwidth and phase margin of the original controller design. Experimental results are provided for 12-to-1.2V, 20A, 500kHz 0.18µm CMOS digital POL converter to show the effectiveness of the proposed method.**

Keywords—scalability, controller scaling, auto-tuning, digital control, Point Of Load,* DC-DC *converter

I. INTRODUCTION

In the design of a POL converter, once the elements characterizing the power stage are dimensioned, a controller that meets both stability and closed-loop dynamic requirements has to be designed. While stability criteria are well understood ([1]-[2]), controller design to optimize transient performance in the presence of unmodeled dynamics requires an iterative procedure where controller parameters are tuned, measured and re-tuned in order to achieve the desired performance. Appropriate tuning methods can eliminate the need for such iteration by observing that the characteristics of a particular DC-DC converter change in a known way. This is useful in case the resonant frequency of the LC filter changes, especially when the bulk capacitance value is uncertain. Solutions to allow compensator tuning have been investigated and proposed in both the analog [3] and digital domains [4]-[13].

Auto-tuning methods seek to address the issue of parameter variation. In general, the compensator auto-tuning process of a digital PWM controller is a two step procedure: firstly, in the system identification phase, characteristics of the plant to compensate are extracted by injecting a perturbation signal on the duty cycle and measuring its effect on the output voltage. Secondly, when at least the resonant frequency of the plant is identified, the controller enters a tuning phase in which it is tuned to meet the specified design targets. The need for a system identification phase in the auto-tuning process leads to one or more of the following issues that make auto-tuning problematic: 1) perturbations are injected in the system in steady state, thus causing jitter on the PWM signal and unwanted noise on the output voltage; 2) computational complexity of the system identification process is high; 3) the identification phase requires a long learning phase. Significant effort has been made to reduce the impact of these issues as well as to eliminate the system identification phase ([12]-[13]). In [12], for example, one of the controller variables, e.g. the gain, is tuned by observing the amplitude and the frequency of the error signal in steady state. In [13], instead, LMS adaptive filters are used to identify the plant to be compensated and a PD controller is tuned to obtain desired location of system closed-loop poles. Although the proposed auto-tuning processes do not require any perturbation of the plant they still suffer from having a tuning process that brings the closed-loop system at the limit of stability ([12]) and of having a very long learning phase. Additionally, in all the proposed tuning methods ([4]-[13]) controller parameters are tuned independently thus lengthening the tuning phase. Depending on the tuning algorithm used, the resulting controller may not be optimal and may not achieve the desired close loop performance.

In this paper it is proposed that the controller parameters of a digital POL converter may be tuned by defining relations between compensator parameters and *a single common tuning variable,* where compensator parameters are tuned as a function of converter resonant frequency. In this way when a reference controller is designed for a specific power stage scenario its closed-loop characteristics can be transformed in a known way to fit different power stages by varying the single common tuning variable.

Some work has been done so far on the scalability of controllers applied to DC-DC converters ([14]), but the importance of this area to the application of digital DC-DC converters motivates more attention. Consequently the aim of this paper is to investigate compensator scaling methods to scale a digital controller from an existing design, focusing on

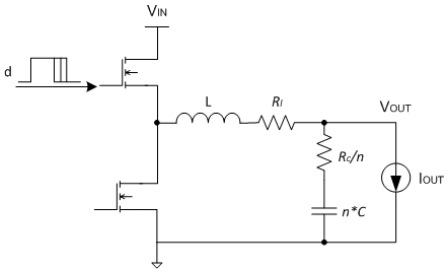

Fig. 1 Schematic of a Buck converter. $G_{vd}(s)$ is the control to output transfer function showing how the duty cycle d acts on the regulation of the output voltage V_{out}.

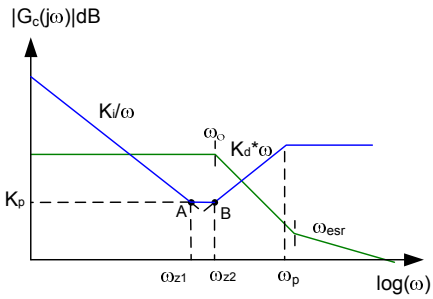

Fig. 2 Frequency response of $G_c(s)$. K_i, K_p, K_d must be intended in dB. The zeros ω_{z1} and ω_{z2} are the projections of the points A and B on the $log(\omega)$ axis.

the case where controller tuning is used to accommodate a change of one of the power stage parameters (i.e. bulk capacitance or output inductor).

In this paper three compensator scaling methods based on a single tuning variable are presented and analyzed. In particular, a new controller scaling method is proposed which is shown to maintain both bandwidth and phase margin of the original design as well as closed-loop characteristics. The proposed scaling methods address practical and simple solutions for compensator scaling, leading to simple scaling formulas and therefore resulting in low computational complexity. Moreover, all proposed tuning methods are suitable to be implemented as auto-tuning algorithms, if desired, once the resonant frequency of the LC filter is known.

II. Problem Formulation

Without loss of generality, let us consider a buck converter as in Fig. 1, having an LC output filter made up of one inductor L and the parallel of n equal capacitors C. The control to output transfer function is given by:

$$G_{vd}(s) = \frac{(s/\omega_{esr}+1)}{\left(\frac{s}{\omega_o}\right)^2 + \frac{s}{Q\cdot\omega_o}+1} V_{in} \quad (1)$$

where $\omega_o = 1/\sqrt{n\cdot L\cdot C}$ is the resonance frequency of the plant $G_{vd}(s)$, $\omega_{esr} = 1/(R_c\cdot C)$ is the zero caused by the ESR of the output capacitor (R_c) and $Q\cdot\omega_o = L(R_l+R_c/n)$, R_l being the DCR of the inductor L. Assume the compensator $G_c(s)$ is designed according to some desired criteria for the case n=1 and stabilizes the plant $G_{vd}(s)$ with bandwidth ω_c and phase margin PM. $G_c(s)$ has the structure:

$$G_c(s) = K\frac{(s/\omega_{z1}+1)(s/\omega_{z2}+1)}{s(s/\omega_p+1)} \quad (2)$$

Typically, compensating a converter to meet regulation objectives implies placing the zeros of the compensator $G_c(s)$ in the vicinity of ω_o to compensate the phase variation due to the LC output filter while the pole ω_p is placed close to ω_{esr} to guarantee sufficient attenuation of the frequencies above the bandwidth ω_c. Furthermore consider the scenario where the number of output capacitors n increases. In this situation ω_o moves to lower frequencies while the zero in ω_{esr} does not change its location. Therefore the controller $G_c(s)$, designed for the case n=1, may still stabilize the plant but loop bandwidth and phase margin are adversely affected, reducing the benefit of the additional output capacitors. For example, it will be shown that doubling the output capacitance results in significantly less improvement in the output voltage deviation under load step conditions than it would be expected if this reduction in loop bandwidth and phase margin had not been considered. The purpose of this paper is to investigate methods to scale the compensator $G_c(s)$ in a way that stability and closed-loop dynamics are preserved, thus resulting in optimum transient response as designed, yielding the full benefit of additional capacitors.

III. Compensator Scaling Methods

Compensator scaling methods can be better understood when the controller $G_c(s)$ is expressed in its proportional, integral, derivative (PID) form. The controller transfer function in (2) can then be rewritten as:

$$G_c(s) = K_p + \frac{K_i}{s} + \frac{K_d s}{(s/\omega_p+1)} \quad (3)$$

where K_p, K_i, K_d are respectively the proportional, integral and derivative coefficients of $G_c(s)$; ω_p is the high frequency pole. An equivalent controller to (3) in the digital domain can be derived applying scaling factors to K_p, K_i, K_d once the sampling frequency of the controller is chosen. For ease of explanation controller scaling methods will be analyzed in the analog (S-)domain and the same results can be transferred to the digital (Z-)domain.

Fig. 2 shows a bode plot of $G_c(s)$ highlighting its proportional, integral and derivative asymptotes as from (3). The term K_i/ω (integral asymptote) models the integrator behavior of $G_c(s)$ at low frequencies, while the derivative asymptote $K_d\cdot\omega$ is responsible for its behaviour at high frequency. The proportional asymptote K_p, parallel to the $log(\omega)$ axis, intersects the integral and derivative asymptotes (points A and B) which gives rise to the controller zeros ω_{z1} and ω_{z2}, i.e. projections of the points A and B on the $log(\omega)$ axis.

Typically, the desired control bandwidth ω_c, is constrained to lie between ω_o and ω_{esr} of $G_{vd}(s)$ and this assumption holds throughout the paper. Control bandwidths lower than ω_o lead to very slow controllers. Bandwidth values higher than ω_{esr} do

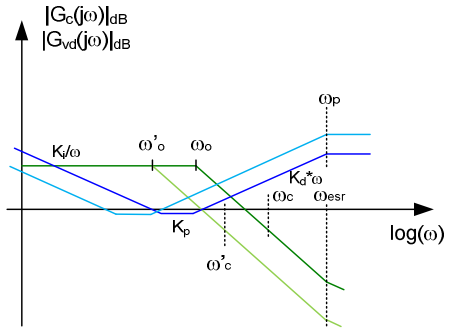

Fig. 3 Graphical representation of the asymptote shifting principle used in Method 1 to scale the original controller $G_c(s)$ (blue curve) designed to stabilize the plant $G_{vd}(s)$ (green curve) to accommodate a variation of ω_o (light green curve) due to an increase of n times of the bulk capacitance. The scaled compensator is represented by the cyan curve. $\omega'_c=\omega_c \cdot \Delta\omega_o$ is the bandwidth of the scaled controller.

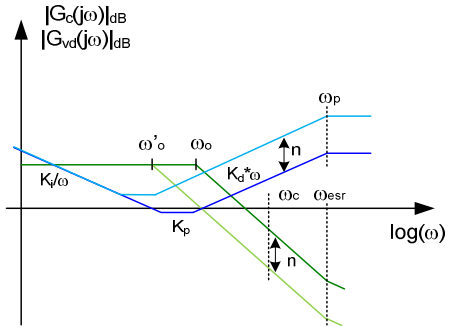

Fig. 4 Graphical representation of the asymptote shifting principle used in Method 2 to scale the original controller $G_c(s)$ (blue curve) designed to stabilize the plant $G_{vd}(s)$ (green curve) to accommodate a variation of ω_o (light green curve) due to an increase of n times of the bulk capacitance. The scaled compensator is represented by the cyan curve.

not improve converter dynamics with respect to load transient since the minimum achievable undershoot is set by the capacitor ESR, together with load step amplitude. The aim of the controller scaling methods is to shift controller asymptotes to accommodate variations of the plant $G_{vd}(s)$ to preserve controller stability as well as closed-loop dynamics.

Once the location of ω_p is fixed, by comparing (3) with (2) the following relations can be derived

$$\begin{aligned} K_i &= K \\ K_p' &= \frac{K_p}{K_i} = \frac{1}{\omega_{z1}} + \frac{1}{\omega_{z2}} - \frac{1}{\omega_p} \\ K_d' &= \frac{K_d}{K_i} = \frac{1}{(\omega_{z1} \cdot \omega_{z2})} - \frac{K_p'}{\omega_p} \end{aligned} \qquad (4)$$

Starting the design of $G_c(s)$ for the case n=1 and placing the high frequency pole ω_p at frequency ω_{esr} to have a zero-pole cancellation, as n increases the plant $G_{vd}(s)$ scales in frequency by a factor of $\Delta\omega_o$ corresponding to the variation of ω_o. Under this condition the following methods to scale controller parameters are proposed.

Method 1

Controller $G_c(s)$ can be scaled by means of the controller scaling theorem as in [14]: given $G_c(s)$ that stabilizes the plant $G_{vd}(s)$ with bandwidth ω_c and phase margin PM the controller $G_c(s/\Delta\omega_o)$ stabilizes the plant $G_{vd}(s/\Delta\omega_o)$ holding the same phase margin and reducing the bandwidth to $\omega_c \cdot \Delta\omega_o$. With the increase of output capacitance the new plant $G_{vd}(s/\Delta\omega_o)$ will results in a frequency scaled version of the original plant $G_{vd}(s)$ only if the ESR zero ω_{esr} is cancelled out by the controller high frequency pole ω_p. Under this assumption a controller $G_c(s)$ with zeros ω_{z1} and ω_{z2} placed near ω_o so that (5) is satisfied

$$\frac{\omega_{z1}}{\omega_o} = a_1, \quad \frac{\omega_{z2}}{\omega_o} = a_2, \qquad (5)$$

can be scaled using the controller scaling theorem in [14]. The scaled controller $G_c(s/\Delta\omega_o)$ will have zeros that still satisfy (5) for the new value of ω_o but bandwidth $\omega_c \cdot \Delta\omega_o$ (Fig. 3). This results in the new controller parameters being:

$$K_{p\_tuned} = K_p,$$

$$K_{i\_tuned} = K_i \Delta\omega_o = K_i / \sqrt{n},$$

$$K_{d\_tuned} = K_d / \Delta\omega_o = K_d \sqrt{n}$$

where $\Delta\omega_o = 1/\sqrt{n}$. Although the phase margin is preserved the bandwidth of the loop obtained with the scaled controller is reduced, thus reducing the benefit of adding additional output capacitance. As such Method 1 fails to meet the requirements as a suitable scaling method.

Method 2

Assuming that ω_c is far from ω_o, which is usually the case in POL applications, relation (5) ensures closed-loop stability because the contribution of the phase lag of the plant at the bandwidth ω_c is lower as n increases.

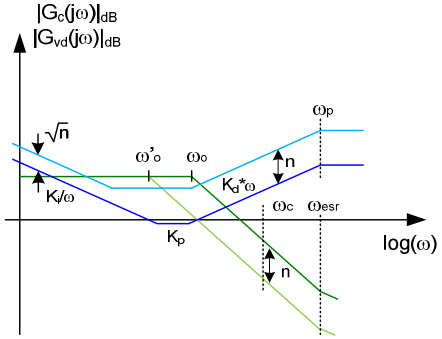

Fig. 5 Graphical representation of the asymptote shifting principle used in Method 3 to scale the original controller $G_c(s)$ (blue curve) designed to stabilize the plant $G_{vd}(s)$ (green curve) to accommodate a variation of ω_o (light green curve) due to an increase of n times of the bulk capacitance. The scaled compensator is represented by the cyan curve.

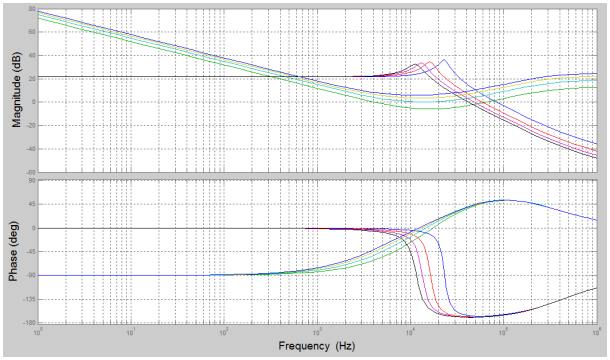

Fig. 6 Bode plot of plant $G_{vd}(s)$ and compensator $G_c(s)$ for $n = 1,2,3,4$ using Method 3. As n increases ω_o moves at lower frequencies and the zeros ω_{z1} , ω_{z2} of $G_c(s)$ moves to lower frequencies leading to a boost of the gain of the open loop at frequency greater of ω_o . Low frequency gain is scaled to accommodate the change of ω_o thus maintaining the original phase margin PM.

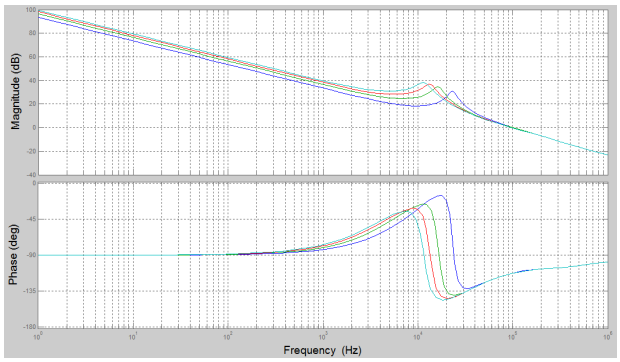

Fig. 7 Bode plot of the Open Loop for $n=1,2,3,4$. The controller $G_c(s)$ scaled as described in Method 3 preserves both phase margin and bandwidth of the original compensator.

This suggests that the open-loop gain may be adjusted to achieve the desired bandwidth while the location of controller zeros with respect to the new ω_o is maintained. From (4) the location of the zeros ω_{z1} and ω_{z2} is related to the parameters K_p' and K_d'. The bandwidth of the original controller is maintained when K_i of the scaled controller equals K_i of the original one and K_p, K_d are scaled to achieve bandwidth and zeros location constrains (5). Considering $n=1$ and assuming that the bandwidth ω_c is such that $\omega_o < \omega_c < \omega_{esr}$, at $\omega >> \omega_o$ the plant $G_{vd}(s)$ can be approximated as:

$$G_{vd}(j\omega)\big|_{\omega>>\omega_o} \cong 1/\left(\frac{j\omega}{\omega_o}\right)^2 \longrightarrow G_{vd}(\omega_c) \cong 1/\left(\frac{\omega_c}{\omega_o}\right)^2 \quad (6)$$

For $n>1$ the resonance frequency of the plant is $\omega'_o = \omega_o / \sqrt{n}$ and the gain of the plant at ω_c is $G_{vd}(\omega_c) \cong \omega_c / (\omega_c / \sqrt{n}) = G_{\omega_c} / n$. As shown in Fig. 4 the scaled compensator should boost the gain of the loop by a factor n at frequencies above ω_o, i.e. K_d should increases of n, while the location of PD zero ω_{z2} should be scaled of $\sqrt{n}$ to accommodate ω'_o. This results in the new

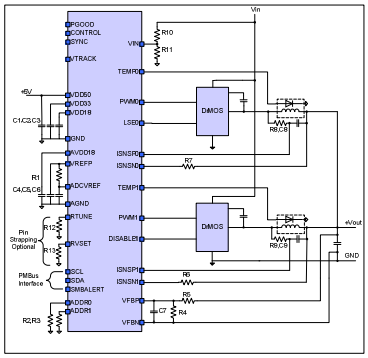

Fig. 8 Application schematic of the ZMDI ZSPM1363 Dual Phase digital controller used to evaluate the proposed scaling methods. Resistor value at the RTUNE™ pin can be trimmed to select different values of n to scale a preconfigured compensator upon a variation of the bulk capacitance.

controller parameters being $K_{p\_scaled} = K_p \cdot \sqrt{n}$, $K_{i\_scaled} = K_i$, $K_{d\_scaled} = K_d \cdot n$. The phase margin of the resulting controller increases due to a weaker influence of the LC output filter on the phase behavior at ω_c, as ω_o moves to lower frequencies. As a consequence the closed-loop output impedance of the scaled controller will exhibit a smaller peak at ω_c with respect to the original design resulting in an improvement of the voltage undershoot [15]. Conversely, because the integral parameter of the scaled controller is not affected by the scaling process the attenuation of the closed-loop impedance at low frequencies is the same as for the original design. This results in an increase of the settling time upon a load step transient. Although this may be acceptable in applications Method 2 does not meet the target of this paper, i.e. derive a controller that scales the closed-loop dynamics of the original design at every frequency.

Method 3: Proposed Method

As stated in [10] with two-parameters compensators, the bandwidth/phase margin constrains *uniquely* define the compensator frequency response and, hence, the desired system loop gain at *every frequency*. It is clear then that once K_{d_scaled} is fixed to achieve the bandwidth constraint both K_p and K_i of the original PI controller need to be scaled to preserve the original phase margin. As K_d increases by a factor n to maintain the bandwidth, K_p has to be increased by the same factor to maintain the location of ω_{z2} and therefore its phase contribution at ω_c. Differently from Method 2, here, K_i is increased by a factor $\sqrt{n}$ to shift the zero in ω_{z1} to follow ω_o, thus guaranteeing enough phase boost around ω'_o. Fig. 5 illustrates the compensator scaling principle. In summary, to achieve enough phase boost at ω'_o, the PI zero ω_{z1} has to shift together with ω_o while the zero in ω_{z2} maintains its original location to compensate for the phase variation at ω_c given by ω_o that has moved to lower frequencies. This results in a scaled compensator having parameters $K_{p\_scaled} = K_p \cdot n$, $K_{i\_scaled} = K_i \cdot \sqrt{n}$, $K_{d\_scaled} = K_d \cdot n$

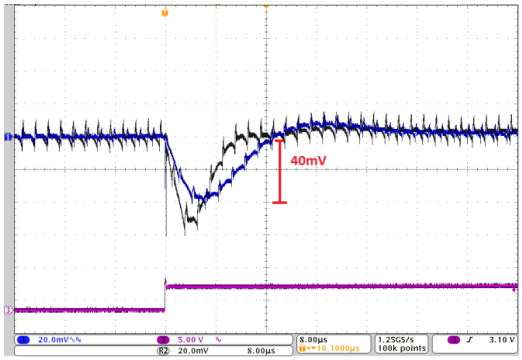

Fig. 9 Comparison between the transient responses of the reference design compensator for the case n=3 (black) and the case n=6 (blue) without compensator scaling. The increase of output capacitance penalizes the close loop dynamic.

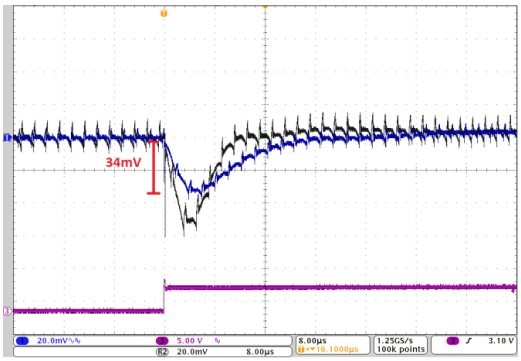

Fig. 10 Comparison between the transient responses of the reference design compensator for the case n=3 (black) and the compensator scaled with Method 1 for the case n=6 (blue).

Fig. 6 and Fig. 7 show the frequency response of the plant, the controller and the open-loop obtained by scaling the compensator as proposed in Method 3.

TABLE I: Summary of the scaling factors to be applied to controller proportional, integral and derivative parameters for the proposed compensator scaling methods.

	Method 1	**Method 2**	**Method 3**
K_p	1	$\sqrt{n}$	n
K_i	$1/\sqrt{n}$	1	$\sqrt{n}$
K_d	$\sqrt{n}$	n	n

IV. EXPERIMENTAL PLATFORM

Method 3 has been incorporated into a commercial POL controller, the ZSPM1363 from ZDMI. The controller could be set for various values of capacitance selecting an RTUNE™ trim resistor (accordingly to the scaling factor n) to evaluate the proposed compensator scaling method. Fig. 8 shows the application schematic of the ZSPM1363. For comparison, Methods 1 and 2 were also evaluated on the same platform.

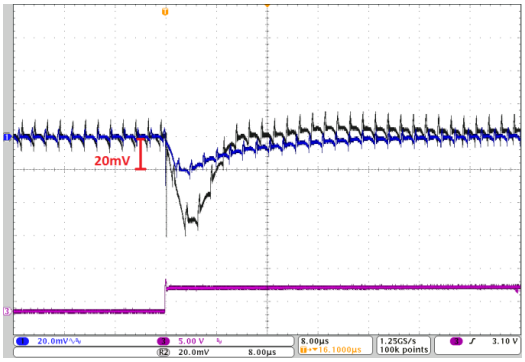

Fig. 11 Comparison between the transient responses of the reference design compensator for the case n=3 (black) and the compensator scaled with Method 2 for the case n=6 (blue). The increase of phase margin significantly slows down the settling time.

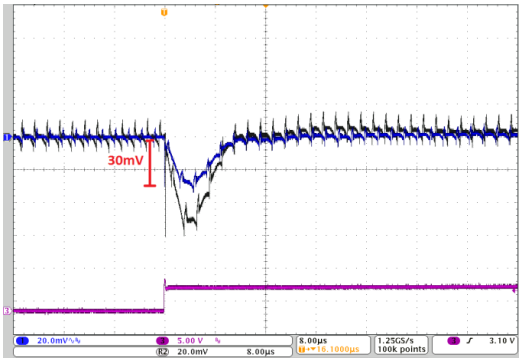

Fig. 12 Comparison between the transient responses of the reference design compensator for the case n=3 (black) and the compensator scaled with Method 3 for the case n=6 (blue). Bandwidth, phase margin and control loop dynamics are preserved compared to the reference design.

V. EXPERIMENTAL RESULTS

Experimental results have been collected for a single phase POL converter, as described in Section IV, having the following parameters: V_{in}=12V, V_{out}=1.2V, F_{sw}=500kHz, L=470nH, output capacitor C=100μF, ESR of output capacitor R_c=2.6$m\Omega$. A controller was designed for: bandwidth f_c=52.54kHz, phase margin PM=45.25°, scaling factor n=3. A reference transient response for a load step from $5A$ to $10A$ was taken. The controller was then scaled for the case n=6 using the three proposed methods. For comparison, the undershoot for a $5A$ load step was approximated as $\Delta V_{out\_pp} = \Delta I_{out} / (2\pi f_c \cdot n \cdot C)$ [11], yielding $\Delta V_{out\_pp} = 53mV$ and $\Delta V_{out\_pp} = 26.5mV$ for n=3 and n=6 respectively. Fig. 9 to Fig. 12 show comparisons between the transient performance of the original compensator (n=3) and the scaled compensators (n=6) using the three proposed methods. Starting from the case where additional capacitance is added without tuning the controller (Fig. 9), i.e. closed-loop dynamics deteriorates both in bandwidth and phase margin, Method 1 shows that closed-loop dynamic can be scaled in time, as explained, by scaling the bandwidth as well (Fig. 10). Method 2 leads to a slightly higher bandwidth compared to the reference design but also increases the phase margin. As

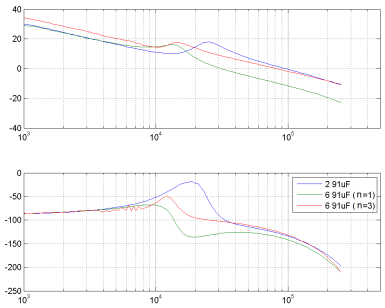

Fig. 13 Gain-Phase measurements of reference compensator design (blue), original compensator (green) and compensator scaled using Method 3 (red) upon increase of the output capacitance of 3 times. Bandwidth and phase margin are preserved.

explained in Section III the settling time of the scaled controller increases because the lack of attenuation of the scaled closed-loop output impedance in the low frequency range (Fig. 11). Method 3 (proposed method) preserves both bandwidth and phase margin, thus maintaining the dynamic performance of the closed-loop as capacitance varies (Fig. 12). TABLE II summarizes the results in terms of bandwidth f_c, phase margin PM, position ω_n of the closed-loop poles and the associated Q factor Q_n. It is interesting to notice that for the case of Method 3 closed-loop pole location is maintained with respect to the original design thus showing that frequency response of the original controller is scaled *at every frequency,* resulting in a load transient response that is actually a scaled version of the load transient response obtained for the original design. Finally, Fig. 13 shows the effectiveness of the proposed method (Method 3) in the frequency domain.

TABLE II: Comparison between obtained bandwidth f_c, phase margin PM and position of closed-loop zeros ω_n, as well as their associated Q factor Q_n with respect to the reference design.

	Reference design		**Method 1**	**Method 2**	**Method 3 (proposed)**
n	3	6	6	6	6
f_c [kHz]	52.54	31	37.28	58.87	52.5
PM [deg]	45.25	42.31	52.27	56.76	40.48
ω_n [rad/s]	$2.06*10^5$	$8.28*10^4$	$1.45*10^5$	$1.66*10^5$	$2.05*10^5$
Q_n	0.702	0.555	0.69	0.54	0.67

VI. CONCLUSIONS

In this paper three methods to scale a controller from an original design to accommodate variation of the power stage resonant frequency are presented and compared. In particular a new scaling method is proposed which is proven to maintain closed-loop dynamics of the original controller. It is shown that only *one single* tuning variable is required to preserve both bandwidth and phase margin of the original design which results in maintaining the original closed-loop poles location as well. Differently from most of the auto-tuning methods proposed so far controller parameters are tuned by acting on a controller proportional, integral and derivative asymptotes rather than controllers zeros directly. As Method 3 clearly shows, the zeros of the scaled controlled are not forced to be of the same type as the zeros of the original controller so that the required phase boost to maintain phase margin constraint is *always* achieved, resulting advantageous for our purposes. Finally, the proposed scaling methods are defined by simple scaling formulas leading to low computational cost tuning solutions that can also be applied to auto-tuning controllers, if desired, with the aim of shortening the controller tuning phase while enabling the tuned controller to match closed-loop dynamics requirements.

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