RENESAS Tool News

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Notes on Using the Real-Time OS --HI7000/4--for the SH-1-, SH-2-, SH2-DSP-, SH-2A-, and SH2A-FPU-Cored MCUs

Please take note of the following problems in using the real-time OS, HI7000/4, for the SH-1-, SH-2-, SH2-DSP-, SH-2A-, and SH2A-FPU-cored MCUs:

- With using HI7000/4 on the SH7250 series of MCUs
- With assigning the CPU's vector numbers 20-31 to an interrupt source in the SH-2A- or SH2A-FPU-cored MCU

1. Problem with Using HI7000/4 on the SH7250 Series of MCUs

1.1 Product and Versions Concerned

HI7000/4 V.2.00 Release 00 through V.2.02 Release 04
(the real-time OS for the SH-1-, SH-2-, SH2-DSP-, SH-2A- and SH2A-FPU-cored MCUs)

1.2 Description

If the following conditions are all satisfied, execution jumps to an incorrect address by the TRAPA #25 instruction executed when the direct interrupt handler described in (2) below is exited.
(1) The C_hivct section is placed at address 0.
(2) There is a direct interrupt handler which is declared by using “#pragma interrupt” with “tn=25”.

1.3 Workarounds

To avoid the problem, perform both of the following:
(1) Place any program or data at addresses other than 0x00000064 through 0x00000067 at linking. For example, place the C_hivct section at address 0x00000068 or later.
(2) At linking, create the file of a reset vector table as follows

```
    and place the C_RESETVEC section at address 0:
#include "kernel.h"
#pragma section _RESETVEC  /* Section name: C_RESETVEC */
extern void hi_cpuini(void);
const UW ResetVector[] = {
    (UW)hi_cpuini,   // Resets the PC.
    0xFFFA0000UL  // Resets the stack pointer.
}
```

1.4 Schedule of Fixing the Problems

The above problem have been fixed in HI7000/4 V.2.02 Release 05.
For details see Section 3 below.

2. With Assigning the CPU's Vector Numbers 20-31 to An Interrupt Source in the SH-2A- or SH2A-FPU-Cored MCU

2.1 Product and Versions Concerned

HI7000/4 V.2.00 Release 00 through V.2.02 Release 04
(the real-time OS for the SH-1-, SH-2-, SH2-DSP-, SH-2A- and SH2A-FPU-cored MCUs)

2.2 Description

(1) The CPU's vector numbers 25 and 26 cannot be defined to any interrupt handler.
(2) In HI7000/4 V.2.00 Release 00 through V.2.00 Release 02, the interrupt handler to which the CPU's Vector Numbers 20-24 and 27-31 are defined are neglected.
(3) In HI7000/4 V.2.01 Release 00 through V.2.02 Release 04, the CPU's Vector Numbers 20-24 and 27-31 cannot be defined to any normal interrupt handler using register banks.

2.3 Workarounds

No methods can be used to avoid this problem.

3. Schedule of Fixing the Problems

The above problems have been fixed in HI7000/4 V.2.02 Release 05.
This version is being published on February 20, 2009, on the Web site at:

http://www.renesas.com/hi7000_4_download

You can update your product to V.2.02 Release 05 free of charge. For how to update yours, see RENESAS TOOL NEWS Document No. 090216/tn3, "The Real-Time OS--HI7000/4--for the SH-1-, SH-2-, SH2-DSP-, SH-2A-,

and SH2A-FPU-Cored MCUs Revised to V.2.02 Release 05," on the Web page at:

http://tool-support.renesas.com/eng/toolnews/090216/tn3.htm

This Web page will be opened from February 20 on.

NOTICE:

Free-of-charge update of V.1 to V.2 is unavailable. If you are using HI7000/4 V.1, please purchase the latest product if necessary.
